

This document provides late-breaking information about device support in the 10.0 SP1 version of the Altera® Quartus® II software. For information about disk space and system requirements, refer to the **readme.txt** file in your **altera/<version number>/quartus** directory. For information about new features, EDA Tool version support, and existing and resolved software issues, refer to the *Quartus II Software Release Notes*.

This document contains the following sections:

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Device Support and Pin-Out Status

This section contains information about the status of support in the Quartus II software for the devices listed.

Full Device Support

The Quartus II software version 10.0 SP1 release does not add any new devices with Full Support.

Advance Device Support

Compilation, simulation, and timing analysis support is provided for the devices listed in [Table 1](#) that will be released in the near future. Although the Compiler generates pin-out information for these devices, the Compiler does not generate programming files for them in this release.

Table 1. Devices with Advance Support

Device Family	Devices	
Cyclone® IV GX	EP4CGX22	EP4CGX30
	EP4CGX50	EP4CGX75
	EP4CGX110	EP4CGX150
HardCopy® IV	HC4GX15	

Initial Information Device Support

Compilation, simulation, and timing analysis support is provided for the devices listed in [Table 2](#) that will be released in the near future. Programming files and pin-out information, however, are not generated for these devices in this release.

Table 2. Devices with Initial Information Support

Device Family	Devices	
Stratix®V	5SGXA3	5SGXA4
	5SGXA5	5SGXA7
	5SGXB5	5SGXB6
	5SGSB7	5SGSB8

Memory and Disk Space Recommendations

A full installation of the Altera Complete Design Suite requires approximately 8.2 GB of available disk space on the drive or partition where you are installing the Altera Complete Design Suite and approximately 30 MB of available space on the drive that contains your **TEMP** directory (Windows only).

The Quartus II Stand-Alone Programmer requires a minimum of 1 GB of RAM plus additional memory, based on the size and number of **.sof** files and the size and number of devices being configured.

Altera recommends that your system be configured to provide swap space (virtual memory) equal to the recommended physical RAM that is required to process your design.

[Table 3](#) lists the memory required to process designs targeted for Altera devices.

Table 3. Memory and Disk Space Recommendations

Device	Recommended Physical RAM	
	32-bit	64-bit
Arria®GX (EP1AGX20) Cyclone (EP1C3, EP1C4, EP1C6, EP1C12, EP1C20) Cyclone II (EP2C5, EP2C8, EP2C20) Cyclone III (EP3C5, EP3C10, EP3C16, EP3C25, EP3C40) Cyclone IV E (EP4CE6, EP4CE10, EP4CE15, EP4CE22, EP4CE30, EP4CE40) Cyclone IV GX (EP4CGX15, EP4CGX22, EP4CGX30) All MAX® series and MAX II device families Stratix (EP1S10, EP1S20) Stratix GX (EP1SGX10) Stratix II (EP2S15)	512 MB	512 MB
Cyclone III (EP3C55, EP3C80) Cyclone IV E (EP4CE55, EP4CE75)	768 MB	1.0 GB

Table 3. Memory and Disk Space Recommendations (Continued)

Device	Recommended Physical RAM	
	32-bit	64-bit
Arria GX (EP1AGX35, EP1AGX50, EP1AGX60) Arria II GX (EP2AGX45) Cyclone II (EP2C35, EP2C50) Cyclone IV E (EP4CE115) Cyclone IV GX (EP4CGX50, EP4CGX75) Stratix (EP1S25, EP1S30, EP1S40, EP1S60) Stratix GX (EP1SGX25, EP1SGX40) Stratix II (EP2S30) Stratix II GX (EP2SGX30, EP2SGX60) Stratix III (EP3SL50, EP3SE50, EP3SL70)	1.0 GB	1.5 GB
Arria GX (EP1AGX90) Arria II GX (EP2AGX65) Cyclone II (EP2C70) Cyclone III (EP3C120) Cyclone III LS (EP3CLS70, EP3CLS100) Cyclone IV GX (EP4CGX110, EP4CGX150) HardCopy II (HC210) Stratix (EP1S80) Stratix II (EP2S60, EP2S90) Stratix II GX (EP2SGX90) Stratix III (EP3SE80) Stratix IV (EP4SGX70)	1.5 GB	2.0 GB
Arria II GX (EP2AGX95, EP2AGX125, EP2AGX190) Cyclone III LS (EP3CLS150, EP3CLS200) Stratix II (EP2S130, EP2S180) Stratix II GX (EP2SGX130) HardCopy II (HC220, HC230, HC240) Stratix III (EP3SL110, EP3SE110, EP3SE150, EP3SL200) Stratix IV (EP4SGX110, EP4SGX230, EP4S40G2 and EP4S100G2)	3.0 GB	4.0 GB
Arria II GX (EP2AGX260) Stratix III (EP3SE260, EP3SL340) Stratix IV (EP4SGX290) Stratix V (5SGXA3)	4.0 GB	6.0 GB
Stratix IV (EP4SGX360, EP4S100G3, EP4S100G4) Stratix V (5SGXA4) HardCopy III (HC325) HardCopy IV (HC4E25)	(1)	8.0 GB

Table 3. Memory and Disk Space Recommendations (Continued)

Device	Recommended Physical RAM	
	32-bit	64-bit
HardCopy III (HC335) HardCopy IV (HC4GX15) Stratix IV (EP4SGX530, EP4SE530, EP4SE820, EP4S40G5, EP4S100G5) Stratix V (5SGXA5, 5SGXB5)	(1)	12.0 GB
HardCopy IV (HC4E35, HC4GX25) Stratix V (5SGXA7, 5SGXB6, 5SGSB7)	(1)	16.0 GB
HardCopy IV (HC4GX35) Stratix V (5SGSB8)	(1)	20.0 GB

(1) These devices cannot be compiled on a 32-bit system.

Timing and Power Models

Table 4 lists a summary of timing and power model status in the current version of the Quartus II software.

Table 4. Devices with Timing and Power Models

Device Family	Device	Timing Model Status	Power Model Status
Arria II GX	EP2AGX45	Final – 10.0	Final – 10.0
	EP2AGX65		
	EP2AGX95		
	EP2AGX125		
	EP2AGX190	Final – 10.0 SP1	
	EP2AGX260		
Cyclone III	EP3C5	Final – 8.0 SP1	Final – 8.1
	EP3C10	Final – 8.0 SP1	
	EP3C16	Final – 8.0 SP1	
	EP3C25	Final – 7.2 SP1	
	EP3C40	Final – 8.0	
	EP3C55	Final – 8.0	
	EP3C80	Final – 8.0	
	EP3C120	Final – 7.2 SP1	
Cyclone III LS	EPC3LS70	Final – 10.0	Final – 10.0 SP1
	EPC3LS100		
	EPC3LS150		
	EPC3LS200		
Cyclone IV E	(All 1.0V)	Final – 10.0 SP1	Final – 10.0 SP1
	(All 1.2V)	Final – 10.0	
Cyclone IV GX	(All)	Preliminary	Preliminary

Table 4. Devices with Timing and Power Models (Continued)

Device Family	Device	Timing Model Status	Power Model Status
HardCopy II	(All)	Correlated – 8.0	Correlated – 7.2
HardCopy III	(All)	Preliminary	Preliminary
HardCopy IV E	(All)	Preliminary	Preliminary
HardCopy IV GX	(All)	Preliminary	Preliminary
MAX IIZ	EPM240Z	Final – 9.0 SP1	Final – 9.0 SP1
	EPM570Z		
Stratix III	EP3SE50	Final – 9.0	Final – 9.0
	EP3SE80	Final – 8.1	
	EP3SE110	Final – 8.1	
	EP3SE260	Final – 9.0	
	EP3SL50	Final – 9.0	
	EP3SL70	Final – 9.0	
	EP3SL110	Final – 8.1	
	EP3SL150	Final – 8.1	
	EP3SL200	Final – 9.0	
	EP3SL340	Final – 8.1	
Stratix IV	EP4SE230	Final – 9.1 SP1	Final – 10.0
	EP4SGX180		
	EP4SGX230		
	EP4S40G2		
	EP4S100G2		
	EP4SE360	Final – 9.1 SP2	
	EP4SE530		
	EP4SGX290		
	EP4SGX360		
	EP4SGX530		
	EP4S40G5		
	EP4S100G3		
	EP4S100G4		
	EP4S100G5		
	EP4SGX70	Final – 10.0	Preliminary
	EP4SGX110		
	EP4SE820	Final – 10.0 SP1	
Stratix V	(All)	Preliminary	Preliminary

The current version of the Quartus II software also includes final timing and power models for the Arria GX, Cyclone, Cyclone II, MAX, MAX II, Stratix, Stratix II, Stratix GX, and Stratix II GX device families. Timing models for these device families became final in the Quartus II software versions 8.0 and earlier.

Stratix V Device Support

General Interest

Quartus II software version 10.0 SP1 provides initial information support for Stratix V devices. This support includes preliminary compilation, simulation, timing analysis, and power analysis support. Programming files and pin-out information are not generated in this release.

Given that the Quartus II software version 10.0 SP1 provides initial information for the Stratix V devices, not all features are provided in this initial release, as described in the following paragraphs.

- The Stratix V device resource counts are preliminary and subject to change.
- RLDRAM II and QDR II external memory interfaces are not supported for Stratix V devices in this release.
- The transceiver protocol PHY IP cores (XAUI PHY, PCI Express PHY, Interlaken PHY, Low Latency PHY, and Custom PHY) support Verilog language generation only; VHDL language generation is not supported in this release.
- The 10GBase-R PHY MegaCore is not supported for Stratix V devices in this release.

Known Issues

Following are known issues related to the release of Stratix V devices.

Transceiver Features

- The following PCI Express Compiler example designs have not yet been optimized for the Stratix V architecture, thus causing difficulty when closing timing for 250MHz variations: Gen1 x8 64 bit, Gen2 x4 64 bit, and Gen2 x8 128 bit.
- Some transceiver configurations that should fit in the selected device may result in Quartus II Compiler errors due to a failure to find a valid placement result. Manual transceiver I/O bank and other constraints may be used to resolve this issue. I/O bank definitions are preliminary in the Quartus II software version 10.0 SP1 and may change in a future release.

PLL and LVDS Features

- The altpll megafunction does not validate the phase shift and duty cycle settings with respect to the reference clock; illegal values may be undetected in this release.
- The altpll megafunction will cause a fitting error when Zero Delay Buffer compensation mode is used.
- The altvds megafunction settings may be incorrect due to a rounding error; in this case, the frequency and the derived clock settings will be incorrect.

I/O Features

- The association of I/O and power pins to I/O banks is preliminary and subject to change. The Fitter report's **I/O Banks Used** panel will not show voltages for banks. Banks missing VCCIO power will not show up in the list of banks.

- Non-transceiver I/O bank assignments are not supported.
- The Fitter might fail if different locally-routed signals are used to clock input registers and output registers of I/Os located in the same location; to resolve the issue, promote one of the affected signals to use the global or quadrant clock network or both.
- The association of VCCPD pins to multiple I/O banks imposes restrictions on VCCIO of the banks sharing the same VCCPD, but this restriction is not verified by the Fitter; explicit location assignments may be used to ensure a legal configuration.

Embedded Memory Features

- RAM memory megafunctions generated by the Memory Compiler® MegaWizard and using the ECC feature may cause warnings during compilation, indicating a port width mismatch on the port *eccstatus*. These warning messages can be safely ignored.
- The *altasm_parallel* megafunction is not supported in this release.
- The *altnmult_add* and *altnmult_accum* megafunctions do not support the Systolic feature for Stratix V devices in this release.

DSP Features

- The *altnmult_add* megafunction behavioral simulation model for Stratix V devices is provided in Verilog language only; no VHDL model is provided.
- Designs using the DSP block may have low performance because the DSP block input registers are bypassed during register packing. In some cases, this issue may be resolved by declaring the asynchronous clear when used by the DSP block as a global signal.
- Designs using the DSP block may also have low performance due to long interconnect delays; manual placement may be used to resolve this issue.
- Simulation of the DSP block may be incorrect for 36x36/18x18-complex dynamic mode when the output is registered.

Changes in Device Support

The following section is divided into device support changes according to whether the change is a notification, or whether the change has been fixed or not fixed. The section pertains to all device families other than Stratix V devices.

Change Notifications

This section provides notifications on devices.

Arria II GX speed grade voltage update

The maximum operating frequency of the Voltage-Controlled Oscillator (VCO) of the Phase Lock Loop (PLL) in Arria II GX devices with speed grades 3, 4, and 5 is updated from 1.6 GHz to 1.3 GHz.

Applies to: Arria II GX devices

Arria II GX new DLL range

The frequency range specification of the Delay Lock Loop (DLL) in Arria II GX devices is updated after further characterization.



For details and solutions, refer to the [Arria II GX Errata Sheet](#).

Applies to: Arria II GX devices

Cyclone III automotive grade devices removed

Support for Cyclone III automotive grade devices has been removed from the Quartus II software version 9.1 SP2. Altera recommends Cyclone IV E automotive grade devices for new designs.

Applies to: Cyclone III devices

No vertical migration for Engineering Sample Stratix IV 230 GX and E and 530 GX and E

Stratix IV GX and E 230 and GX and E 530 GX devices in Engineering Sample (ES) version are not allowed for vertical migration with the production devices due to the voltage changes. (Core voltage for ES devices is 0.95V, while core voltage for production devices is 0.9V.) To access vertical migration, use the corresponding production device in the design.

Applies to: Stratix IV devices

Device Support Not Fixed

This section provides details for device support that has not currently been fixed.

Stratix III DDR input functional failure

Stratix III DDR input registers fail to capture edge-aligned input data correctly while the TimeQuest Timing Analyzer shows positive slack when you use the corner clock pin and corner PLL.

The path from the corner clock pin to the corner PLL has incorrect delay and the patch updates the delay. Designs utilizing the affected path on the affected Stratix III parts will need to rerun the TimeQuest Timing Analyzer. If new timing violations occur, you must rerun the Fitter.

Applies to: Stratix III devices

Cyclone IV GX incorrect megafunction setting

All High-Speed Serial Interface (HSSI) PLLs should have the operation mode set to **no_compensation**, except for CPRI with PLL phase frequency detector (PFD) feedback turned on when the feedback is set to **normal**. MPLLs 6 and 7 do not support Compensation mode, but the altgx megafunction incorrectly sets the compensation mode to **normal** for CPRI with PFD turned off and duplex SDI design with reconfiguration turned on. The incorrect megafunction setting causes the placer to not use MPLL 6 or 7, which causes a no-fit.

For the design scenarios mentioned above, manually edit the generated altgx design file to modify the instance of the PLL operation mode to **no_compensation**.

Applies to: Cyclone IV GX devices

Cyclone IV GX incorrect simulation

For Cyclone IV GX devices, when simulating a design containing an altlvds megafunction, an incorrect result may occur when the **Enable bitslip control** option is turned on.

Applies to: Cyclone IV GX devices

Device Support Fixed

This section provides details for device support that has been fixed.

PCI Express Compiler cannot generate files for Gen1 protocol

The PCI Express Compiler v10.0 did not support IP and MegaWizard generation or regeneration of PCIe® Gen1 x4 or x8 designs targeting the Stratix IV and HardCopy IV device families.



For more information and solutions for this issue, refer to Knowledge Database solution [rd07012010_723](#).

This issue was fixed in the Quartus II software version 10.0.

Applies to: Stratix IV and HardCopy IV devices

Final timing model change

The timing model was changed in Stratix III and Stratix IV devices by removing an unused path in Half-Rate DDIO Input, which allows the Fitter to better optimize truly critical paths. User designs that closed timing do not need to perform any action.

Applies to: Stratix III and Stratix IV devices

Fixed timing simulation of Stratix IV SERDES_RX

A bug in timing simulation of Stratix IV SERDES_RX was fixed, and, as a result, the timing simulation of SERDES_RX does not capture the data bit correctly. This issue does not affect silicon behavior.

Applies to: Stratix IV devices

SERDES bit settings change

Revised and optimized SERDES bit settings according to final silicon characterization on Arria II GX parts.

Applies to: Arria II GX devices