

This document provides late-breaking information about device support in the Altera® Quartus® II software version 11.0. For information about disk space and system requirements, refer to the **readme.txt** file in your **altera/<version number>/quartus** directory. For information about new features, EDA Tool version support, and existing and resolved software issues, refer to the *Quartus II Software Release Notes*.

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Device Support and Pin-Out Status

This section contains information about the device support status in the Quartus II software version 11.0.

Full Device Support

Full compilation, simulation, timing analysis, and programming support is now available for the following new devices and device packages:

Table 1. Devices with Full Support

Device Family	Devices	
Cyclone® IV GX	EP4CGX30CF23	EP4CGX50
	EP4CGX75	
MAX® V	5M40ZE64	5M40ZM64
	5M80ZE64	5M80ZM64
	5M160ZE64	

Advance Device Support

Compilation, simulation, and timing analysis support is provided for the devices listed in [Table 2](#) that will be released in the near future. The Compiler generates pin-out information for these devices in this release, but does not generate programming files.

Table 2. Devices with Advance Support

Device Family	Devices	
Stratix® V	5SGXEA5	5SGXEA7
	5SGXMA5	5SGXMA7
	5SGXMA7ES	

Initial Information Device Support

Compilation, simulation, and timing analysis support is provided for the devices listed in [Table 3](#) that will be released in upcoming versions of the Quartus II software. Programming files and pin-out information are not generated for these devices in this release.

Table 3. Devices with Initial Information Support

Device Family	Devices	
Stratix V	5SGSED6	5SGSED8
	5SGSMD4	5SGSMD5
	5SGSMD6	5SGSMD8
	5SGXEA3	5SGXEA4
	5SGXEB5	5SGXEB6
	5SGXMA3	5SGXMA4
	5SGXMB5	5SGXMB6

Memory and Disk Space Recommendations

A full installation of the Altera software requires up to 10 GB of available disk space on the drive or partition where you are installing the Altera software.

The Quartus II Stand-Alone Programmer requires a minimum of 1 GB of RAM plus additional memory, based on the size and number of `.sof` files and the size and number of devices being configured.

Altera recommends that your system be configured to provide virtual memory equal to the recommended physical RAM that is required to process your design.

Table 4 lists the memory required to process designs targeted for Altera devices.

Table 4. Memory and Disk Recommendations

Family	Device	Recommended Physical RAM	
		32-bit	64-bit
Arria® GX	EP1AGX20	512 MB	512 MB
	EP1AGX35, EP1AGX50, EP1AGX60	1.0 GB	1.5 GB
	EP1AGX90	1.5 GB	2.0 GB
Arria II GX	EP2AGX45	1.0 GB	1.5 GB
	EP2AGX65	1.5 GB	2.0 GB
	EP2AGX95, EP2AGX125, EP2AGX190	3.0 GB	4.0 GB
	EP2AGX260	4.0 GB	6.0 GB
Arria II GZ	EP2AGZ225	3.0 GB	4.0 GB
	EP2AGZ300	4.0 GB	6.0 GB
	EP2AGZ350	N/A	8.0 GB
Cyclone	All	512 MB	512 MB
Cyclone II	EP2C5, EP2C8, EP2C20	512 MB	512 MB
	EP2C35, EP2C50	1.0 GB	1.5 GB
	EP2C70	1.5 GB	2.0 GB
Cyclone III	EP3C5, EP3C10, EP3C16, EP3C25, EP3C40	512 MB	512 MB
	EP3C55, EP3C80	768 MB	1.0 GB
	EP3C120	1.5 GB	2.0 GB
Cyclone III LS	EP3CLS70, EP3CLS100	1.5 GB	2.0 GB
	EP3CLS150, EP3CLS200	3.0 GB	4.0 GB
Cyclone IV E	EP4CE6, EP4CE10, EP4CE15, EP4CE22, EP4CE30, EP4CE40	512 MB	512 MB
	EP4CE55, EP4CE75	768 MB	1.0 GB
	EP4CE115	1.0 GB	1.5 GB
Cyclone IV GX	EP4CGX15, EP4CGX22, EP4CGX30	512 MB	512 MB
	EP4CGX50, EP4CGX75	1.0 GB	1.5 GB
	EP4CGX110, EP4CGX150	1.5 GB	2.0 GB
HardCopy® II	HC210	1.5 GB	2.0 GB
	HC220, HC230, HC240	3.0 GB	4.0 GB

Table 4. Memory and Disk Recommendations (Continued)

Family	Device	Recommended Physical RAM	
		32-bit	64-bit
HardCopy III	HC325	N/A	8.0 GB
	HC335	N/A	12.0 GB
HardCopy IV	HC4E25	N/A	8.0 GB
	HC4GX15	N/A	12.0 GB
	HC4E35, HC4GX25	N/A	16.0 GB
	HC4GX35	N/A	20.0 GB
MAX	All	512 MB	512 MB
MAX II	All	512 MB	512 MB
MAX V	All	512 MB	512 MB
Stratix	EP1S10, EP1S20	512 MB	512 MB
	EP1S25, EP1S30, EP1S40, EP1S60	1.0 GB	1.5 GB
	EP1S80	1.5 GB	2.0 GB
Stratix GX	EP1SGX10	512 MB	512 MB
	EP1SGX25, EP1SGX40	1.0 GB	1.5 GB
Stratix II	EP2S15	512 MB	512 MB
	EP2S30	1.0 GB	1.5 GB
	EP2S60, EP2S90	1.5 GB	2.0 GB
	EP2S130, EP2S180	3.0 GB	4.0 GB
Stratix II GX	EP2SGX30, EP2SGX60	1.0 GB	1.5 GB
	EP2SGX90	1.5 GB	2.0 GB
	EP2SGX130	3.0 GB	4.0 GB
Stratix III	EP3SL50, EP3SE50, EP3SL70	1.0 GB	1.5 GB
	EP3SE80	1.5 GB	2.0 GB
	EP3SL110, EP3SE110, EP3SE150, EP3SL200	3.0 GB	4.0 GB
	EP3SE260, EP3SL340	4.0 GB	6.0 GB
Stratix IV	EP4SGX70	1.5 GB	2.0 GB
	EP4SGX110, EP4SGX230, EP4S40G2, EP4S100G2	3.0 GB	4.0 GB
	EP4SGX290	4.0 GB	6.0 GB
	EP4SGX360, EP4S100G3, EP4S100G4	N/A	8.0 GB
	EP4SGX530, EP4SE530, EP4SE820, EP4S40G5, EP4S100G5	N/A	12.0 GB

Table 4. Memory and Disk Recommendations (Continued)

Family	Device	Recommended Physical RAM	
		32-bit	64-bit
Stratix V	5SGXA3	4.0 GB	6.0 GB
	5SGXA4	N/A	8.0 GB
	5SGXA5, 5SGXB5	N/A	12.0 GB
	5SGXA7, 5SGXB6, 5SGSB7	N/A	16.0 GB
	5SGSB8	N/A	20.0 GB

Timing and Power Models

Table 5 lists a summary of timing and power model status in the current version of the Quartus II software.

Table 5. Devices with Timing and Power Models

Device Family	Device	Timing Model Status	Power Model Status
Arria II GX	EP2AGX45	Final – 10.0	Final – 10.0
	EP2AGX65		
	EP2AGX95		
	EP2AGX125		
	EP2AGX190	Final – 10.0 SP1	
	EP2AGX260		
Arria II GZ	All	Final – 10.1	Final – 10.1
Cyclone III LS	EPC3LS70	Final – 10.0	Final – 10.0 SP1
	EPC3LS100		
	EPC3LS150		
	EPC3LS200		
Cyclone IV E	All 1.0V	Final – 10.0 SP1	Final – 10.0 SP1
	All 1.2V	Final – 10.0	
Cyclone IV GX	EP4CGX15	Final – 10.1	Final – 11.0
	EP4CGX22	Final – 11.0	
	EP4CGX30		(1)
	EP4CGX50	Final – 11.0	Preliminary
	EP4CGX75		
	EP4CGX110	Final – 10.1	Final – 11.0
	EP4CGX150		
HardCopy III	All	Preliminary	Preliminary
HardCopy IV E	All	Preliminary	Preliminary
HardCopy IV GX	All	Preliminary	Preliminary
MAX IIZ	EPM240Z	Final – 9.0 SP1	Final – 9.0 SP1
	EPM570Z		

Table 5. Devices with Timing and Power Models (Continued)

Device Family	Device	Timing Model Status	Power Model Status
MAX V	All	Final – 11.0	Final – 11.0
Stratix IV	EP4SE230	Final – 9.1 SP1	Final – 10.0
	EP4SGX180		
	EP4SGX230		
	EP4S40G2		
	EP4S100G2		
	EP4SE360	Final – 9.1 SP2	
	EP4SE530		
	EP4SGX290		
	EP4SGX360		
	EP4SGX530		
	EP4S40G5		
	EP4S100G3		
	EP4S100G4		
	EP4S100G5		
	EP4SGX70		
	EP4SGX110	Final – 10.0	
EP4SE820	Final – 10.0 SP1		
Stratix V	All	Preliminary	Preliminary
(1) EP4CGX30BF14 and EP4CGX30CF19 are final in 11.0. EP4CGX30CF23 is preliminary.			

The current version of the Quartus II software also includes final timing and power models for the Arria GX, Cyclone, Cyclone II, Cyclone III, HardCopy II, MAX, MAX II, MAX IIZ, Stratix, Stratix GX, Stratix II, Stratix II GX, and Stratix III device families. Timing models for these device families became final in the Quartus II software versions 9.0 and earlier.

Changes in Device Support

The following section is divided into device support changes according to whether the change is a notification, or whether the change has been fixed or not fixed.

Change Notifications

This section provides notifications for changes to devices.

Stratix IV pin file changes

In pin files that are generated by the Quartus II software version 11.0, you can observe the following changes as compared to the previously generated pin files. You can see these changes in Stratix IV EP4SGX290/360 FH29 devices and all GT devices. Certain pins that you could use in configuration mode only or for their JTAG functionality now show the corresponding functions in the pin file. Previously they appeared as the gnd* pin. You might see similar changes in the Pin Planner. Only the reported names changed. The underlying functionality and the placement remain the same.

Applies to: Stratix IV devices

Final timing model change for Cyclone IV E

The fast corner timing model was updated to reflect a smaller minimum pulse width. This timing model update results in a higher f_{MAX} limit when analyzing under the fast corner operating condition. This fix will remove the false warning “minimum pulse width violation” in timing reports. If your design passed timing checks in existing designs, no action is required. Designs that did not pass all timing checks before this update should employ the necessary timing closure techniques to ensure all timing checks pass.

Applies to: Cyclone IV E devices

MAX V pin name change

For the MAX V ordering code 5M160Z-M100C4, one of the pins in the package ddb_maxv2mbga100_pkg.ddb was incorrectly named, and has been correctly renamed.

Applies to: MAX V devices

Device Support Not Fixed

This section provides details for device support issues that have not yet been fixed.

Gate-level simulation flow for Stratix V designs

The generation of EDA simulation netlist files for post-synthesis or post-fit gate-level simulation is not supported in the Quartus II software version 11.0.

Applies to: Stratix V devices

Device Support Fixed

This section provides details for device support issues that have been fixed.

Final timing model change – Arria II GX LVPECL maximum data rate

The Arria II GX LVPECL maximum data rate is increased from 350 MHz to the LVDS data rate, which is a minimum of 500 MHz.

Applies to: Arria II GX devices



For more information, refer to the [Arria II Device Handbook](#).

Final timing model change – Arria II GX LVDS timing parameters

The Arria II GX sampling window for the LVDS SERDES is updated for speed grades 3 and 4 from 750 ps to 300 ps, for speed grade 5 from 750 ps to 350 ps, and for speed grade 6 from 750 ps to 400 ps. To see the improved RSKM value, re-run the TimeQuest Timing Analyzer.

The Arria II GX TCCS for the LVDS SERDES is updated for speed grades 3 and 4 from 100 ps to 150 ps, for speed grade 5 from 100 ps to 175ps, and for speed grade 6 from 100 ps to 200 ps. To see the updated TCCS number, re-run the TimeQuest Timing Analyzer.



For more information, refer to the [Arria II Device Handbook](#).