



# Quartus II Software Release Notes

January 2004

Quartus II version 4.0

This document provides late-breaking information about the following areas of this version of the Altera® Quartus® II software. For information about memory, disk space, and system requirements, refer to the **readme.txt** file in your **quartus** directory.

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## New Features & Enhancements

The Quartus II software version 4.0 includes the following new features and enhancements:

- **Memory Compiler Waveform Generation**—Produces waveform displays of memory structure operation based on memory parameterization and configuration selections. This feature of the MegaWizard Plug-In Manager makes it easier to understand the effects of different memory configuration settings.
- **RTL Viewer**—Provides a schematic representation of the design netlist that can be used to analyze a design's structure before further behavioral simulation, synthesis, and place-and-route steps are performed. The RTL Viewer allows designers to navigate a design's hierarchy and locate particular items of interest easily to aid in debugging and optimization. Selected items in the RTL Viewer can be directly traced back to source design files.
- **Compilation Revisions**—Allows designers to experiment using different compilation settings and assignments for a given design. A group of settings, assignments, and compilation results can be stored and processed separately as an individual design revision.
- **Physical Synthesis Support**—Adds physical synthesis optimization support for the Stratix II FPGA family.
- **Design Space Explorer Distributed Computing Support**—Design Space Explorer-automated design optimization script now supports distributed environments where multiple computers can run simultaneous compilations using different optimization settings.
- **SignalTap<sup>®</sup> II Advanced Triggering Feature**—Provides a graphical environment to implement complex user-defined trigger logic to compare bus states and individual signals to initiate SignalTap II embedded logic analyzer data capture. This feature gives FPGA designers unprecedented flexibility to isolate system design problems in-system and at system speeds.
- **Faster Compilation Times on Linux Platforms**—Improves compilation times by an average of 40% because the Quartus II software version 4.0 for Red Hat Linux versions 7.3 and 8.0 takes advantage of new software optimizations.
- **Easier Licensing**—Now the Quartus II software will automatically download from the web and install your already purchased node-locked license.
- **Faster Compilation Times for Many Designs**—The new Auto Fit feature shortens compilation times significantly for designs where the timing requirements are met easily.

## Project & Settings Files In This Release

The method that the Quartus II software version 4.0 uses to store assignments has changed substantially from the method used by the Quartus II software version 3.0 and earlier.

If you wish to work on a project you created using the Quartus II software version 3.0 or earlier, you should open and save the project in the GUI once, even if you are using the command-line executables to compile your project. Opening and saving your project in the GUI ensures that your setting and assignment files are converted properly.

When you open a project created in the Quartus II software version 3.0 or earlier, the following changes are made to your assignment and setting files:

- Your *<project>.quartus* file is converted to the new Quartus Project File (**.qpf**) format, and the original file is moved to the *\<project>\<project>.bak* directory.
- The contents of your Compiler Settings File (**.csf**), Entity Settings File(s) (**.esf**), Simulation Settings File (**.ssf**), Project Settings File (**.psf**), and Software Build Settings File (**.fsf**) are merged into the new Quartus Settings File (*<project>.qsf*), and the original files are moved to the *\<project>\<project>.bak* directory.
- Once the Quartus II software has converted your files and moved to originals to the backup directory, the files will not be used by the Quartus II software, so changes made to those files will be ignored.

# Device Support & Pin-Out Status

## Full Device Support

Full compilation, simulation, timing analysis, and programming support is now available for the following new devices and device packages:

### *Devices with Full Support*

Device Family	Devices	
Stratix GX	EP1SGX25F672 EP1SGX40F1020	EP1SGX25F1020

## Advance Device Support

Compilation, simulation, and timing analysis support is provided for the following devices that will be released in the near future. Although the Compiler generates pin-out information for these devices, it does not generate programming files for them in this release.

### *Devices with Advance Support*

Device Family	Devices
None	

## Initial Information Support

Compilation, simulation, and timing analysis support is provided for the following devices that will be released in the near future. Programming files and pin-out information, however, are not generated for these devices in this release.

### *Devices with Initial Information Support*

Device Family	Devices	
Stratix II	EP2S15 EP2S60 EP2S130	EP2S30 EP2S90 EP2S180

## Timing Models

This section contains a summary of timing model status in the current version of the Quartus II software.

### Preliminary Timing Models

The following table shows the devices with preliminary timing models in the current version of the Quartus II software:

#### *Devices with Preliminary Timing Models*

Device Family	Device
Stratix II	EP2S15
	EP2S30
	EP2S60
	EP2S90
	EP2S130
	EP2S180

### Final Timing Models

The following table lists the devices with final timing models that are available in the current version of the Quartus II software:

**Devices with Final Timing Models**

Device Family	Device	Timing Models Final in Quartus II Version Number
APEX™ II	EP2A15	2.1
	EP2A25	2.1
	EP2A40	2.1
	EP2A70	2.1
Cyclone	EP1C3	3.0 SP1
	EP1C4	4.0
	EP1C6	3.0
	EP1C12	3.0 SP1
	EP1C20	3.0
FLEX 10K	All	3.0
FLEX 10KA	All	3.0
Mercury™ <sup>(1)</sup>	EP1M120	2.1 SP1
MAX 3000 <sup>(1)</sup>	EPM3512A	2.1 SP1
MAX 7000 <sup>(1)</sup>	EPM7512B	2.1 SP1
MAX 7000S	All	3.0
Stratix	EP1S10	2.2 SP2
	EP1S20	2.2 SP2
	EP1S25	2.2 SP2
	EP1S30	2.2 SP2
	EP1S40	2.2 SP2
	EP1S60	3.0
	EP1S80	3.0
Stratix GX	EP1SGX10	4.0
	EP1SGX25	4.0
	EP1SGX40	4.0

(1) Timing models for devices in this device family not listed here became final in versions 2.1 and earlier.

The current version of the Quartus II software also includes final timing models for the ACEX® 1K, APEX 20K, APEX 20KE, APEX 20KC, Excalibur, FLEX 6000, and FLEX 10KE device families. Timing models for these device families became final in versions earlier than version 2.1.

## Changes to Default Settings in This Release

Setting Keyword	Default in 3.0	Default in 4.0
ACLK_CAT	"Off"	"ON"
ACLK_RULE_IMSZER_ADOMAIN	"Off"	"ON"
ACLK_RULE_NO_SZER_ACLK_DOMAIN	"Off"	"ON"
ACLK_RULE_SZER_BTW_ACLK_DOMAIN	"Off"	"ON"
ASSG_CAT	"Off"	"ON"
ASSG_RULE_MISSING_FMAX	"Off"	"ON"
ASSG_RULE_MISSING_TIMING	"Off"	"ON"
AUTO_RESTART_CONFIGURATION	"off"	"ON"
CLK_CAT	"Off"	"ON"
CLK_RULE_CLKNET_CLKSPINES	"Off"	"ON"
CLK_RULE_COMB_CLOCK	"Off"	"ON"
CLK_RULE_GATING_SCHEME	"Off"	"ON"
CLK_RULE_INPINS_CLKNET	"Off"	"ON"
CLK_RULE_INV_CLOCK	"Off"	"ON"
CLK_RULE_MIX_EDGES	"Off"	"ON"
DRC_REPORT_FANOUT_EXCEEDING	"Off"	"ON"
DRC_REPORT_TOP_FANOUT	"Off"	"ON"
HCPY_ALOAD_SIGNALS	"Off"	"ON"
NONSYNCHSTRUCT_RULE_ASYN_RAM	"Off"	"ON"
HCPY_CAT	"Off"	"ON"
HCPY_VREF_PINS	"Off"	"ON"
NONSYNCHSTRUCT_CAT	"Off"	"ON"
NONSYNCHSTRUCT_RULE_COMB_DRIVES_RAM_WE	"Off"	"ON"
NONSYNCHSTRUCT_RULE_COMBLOOP	"Off"	"ON"
NONSYNCHSTRUCT_RULE_DELAY_CHAIN	"Off"	"ON"
NONSYNCHSTRUCT_RULE_ILLEGAL_PULSE_GEN	"Off"	"ON"
NONSYNCHSTRUCT_RULE_LATCH_UNIDENTIFIED	"Off"	"ON"
NONSYNCHSTRUCT_RULE_MULTI_VIBRATOR	"Off"	"ON"
NONSYNCHSTRUCT_RULE_REG_LOOP	"Off"	"ON"
NONSYNCHSTRUCT_RULE_RIPPLE_CLK	"Off"	"ON"
NONSYNCHSTRUCT_RULE_SRLATCH	"Off"	"ON"
APEX20K_OPTIMIZATION_TECHNIQUE	"Speed"	"Balanced"
CYCLONE_OPTIMIZATION_TECHNIQUE	"Area"	"Balanced"
STRATIX_OPTIMIZATION_TECHNIQUE	"Speed"	"Balanced"
RECOMPILE_QUESTION	"Normal"	"Yes"
RESET_CAT	"Off"	"ON"
RESET_RULE_COMB_ASYNCH_RESET	"Off"	"ON"
RESET_RULE_IMSYNCH_ASYNCH_DOMAIN	"Off"	"ON"

<b>Setting Keyword</b>	<b>Default in 3.0</b>	<b>Default in 4.0</b>
RESET_RULE_IMSYNCH_EXRESET	"Off"	"ON"
RESET_RULE_INPINS_RESETNET	"Off"	"ON"
RESET_RULE_UNSYNCH_ASYNCH_DOMAIN	"Off"	"ON"
RESET_RULE_UNSYNCH_EXRESET	"Off"	"ON"
SIGNALRACE_CAT	"Off"	"ON"
SIGNALRACE_RULE_ASYNCHPIN_SYNCH_CLKPIN	"Off"	"ON"
TIMING_CAT	"Off"	"ON"
TIMING_RULE_COIN_CLKEDGE	"Off"	"ON"
TIMING_RULE_SHIFT_REG	"Off"	"ON"

## EDA Interface Information

The Quartus II software version 4.0 supports the following EDA tools.

### Supported EDA Tools

Synthesis Tools	Version	NativeLink <sup>®</sup> support
Mentor Graphics <sup>®</sup> LeonardoSpectrum-Altera	2002f	✓
Mentor Graphics <sup>®</sup> LeonardoSpectrum	2003b	✓
Synopsys Design Compiler	2002.02	
Mentor Graphics Precision RTL Synthesis	2003c	✓
Synplicity Synplify and Synplify Pro	7.5	✓
Aplus Design Technologies (ADT) PALACE <sup>™</sup>	2.3	✓
Verification Tools	Version	NativeLink support
Cadence NC-Verilog (Windows)	5.0 (s006)	✓
Cadence NC-Verilog (Solaris)	5.0 (s005)	
Cadence NC-VHDL (Windows)	5.0 (s006)	✓
Cadence NC-VHDL (Solaris)	5.0 (s005)	
Cadence Verilog-XL	3.3	
Model Technology <sup>™</sup> ModelSim <sup>®</sup>	5.7e	✓
Model Technology ModelSim-Altera	5.7e	✓
Mentor Graphics BLAST	1.2.2	
Synopsys PrimeTime	2003.03 SP1	✓
Synopsys Scirocco	2002.06	✓
Synopsys VSS	2000.05	
Synopsys VCS	7.0.1	
Mentor Graphics Tau	2.2	
Cadence Conformal LEC	4.2.0.a	

# Known Issues & Workarounds

## General Quartus II Software Issues

Issue	Workaround
<p>The Quartus II software no longer uses the registry to store non-user interface-related settings. Non-user interface-related settings are stored automatically in the <b>quartus2.ini</b> file when you open the Quartus II software user interface for the first time.</p>	<p>You must open the Quartus II software user interface at least once before using the command-line version of the software.</p>
<p>Versions of the Quartus II software earlier than version 3.0 cannot open Block Design Files (<b>.bdf</b>) created with the Quartus II software version 3.0 and later.</p>	<p>You can alter the BDF so that it can be opened in earlier versions, but location information will be lost.</p> <ol style="list-style-type: none"> <li>1. Open the BDF in any text editor (vi, emacs, notepad).</li> <li>2. Change the version from 1.3 to 1.2 in the header section.</li> <li>3. Remove all the lines with string "location," for example,           <pre>(annotation_block (location) (rect -336 -40 -248 -8)).</pre> </li> <li>4. Save the file.</li> </ol>
<p>Changes made to settings and/or assignments in the Assignment Editor, Floorplan Editor, or with Tcl commands in the Tcl Console window are saved to disk only when you choose <b>Save Project</b> (File menu). Choosing <b>Save</b> in the Assignment Editor, Floorplan Editor, or <b>Settings</b> dialog box saves the changes to memory only. They are not committed to disk until you choose <b>Save Project</b> (File menu), close the project, or exit from the Quartus II software. If you have turned off <b>Save changes to all files before starting a compilation, simulation, or software build</b> on the <b>Processing</b> page of the <b>Options</b> dialog box (Tools menu), changes you made may not be reflected in the latest compilation.</p>	<p>Turn on <b>Save changes to all files before starting a compilation, simulation, or software build</b> on the <b>Processing</b> page of the <b>Options</b> dialog box (Tools menu).</p> <p><i>or</i></p> <p>Choose <b>Save Project</b> (File menu) after making any changes to Settings or Assignments.</p>
<p>Not all speed grades of a given device share the same features.</p>	<p>Refer to the Altera device Handbook for further information.</p>

Issue	Workaround
<p>The default setting for the <b>Power-Up Don't Care</b> logic option has been changed to <b>On</b> in the Quartus II software version 2.1 Service Pack 1 and later.</p>	
<p>There is no distinction between output ports and bidirectional ports in AHDL Function Prototypes; instead, all ports listed after the RETURNS keyword are treated as output ports. As a result, if you specify a bidirectional port in a logic function's Function Prototype Statement and do not connect the port to a top-level bidirectional pin or to other logic in the design where you instantiate the logic function, an error can occur.</p>	<p>Connect the port to a top-level bidirectional pin or to other logic in the design.</p>
<p>Context-sensitive Help is not available for some items in the Quartus II software.</p>	<p>To locate Help on those items, choose <b>Index</b> (Help menu) and type the name of the item.</p>
<p>For APEX 20KE devices, the Quartus II software provides limited support for the following I/O standards that are not available with the <b>I/O Standard</b> logic option:</p> <ul style="list-style-type: none"> <li>• <b>LVPECL</b> is a differential I/O standard that is similar to the <b>LVDS</b> I/O standard. APEX 20KE devices can support LVPECL I/O pins by using the I/O pins in LVDS mode with an external resistor network.</li> <li>• <b>PCI-X</b> is an enhanced version of the <b>PCI</b> I/O standard that can support a higher average bandwidth. This standard has more stringent requirements than PCI.</li> </ul>	<p>To use the <b>LVPECL</b> I/O standard in APEX 20KE devices in the Quartus II software, set the <b>I/O Standard</b> logic option for the pins to <b>LVDS</b> and connect the pins to an appropriate external resistor network.</p> <p>The APEX 20KE I/O drivers meet the requirements for <b>PCI-X</b>. Turn on the <b>PCI I/O</b> logic option to support PCI-X requirements, including the overshoot clamp.</p>
<p>If you open a project that was created using an earlier version of the Quartus II software, you may receive a message that indicates that the database is incompatible and that results of the last compilation will be lost.</p>	<p>To maintain existing placement information and optionally routing information, back-annotate all of the project assignments in the earlier version. You may also need to generate a Quartus II Verilog Mapping file (<b>.vqm</b>) netlist to preserve the result of Physical Synthesis.</p>
<p>The Timing Analyzer does not recognize nonPLL clock signals when using any PLL megafunction.</p>	<p>Make clock settings assignments to all nonPLL clocks.</p>

Issue	Workaround
The Waveform Editor does not allow you to create a bus with nodes that are nonconsecutive members of a bus.	Create buses only with nodes that are consecutive members of a bus. Or, use the <b>Group</b> command (Edit menu) to create groups of arbitrary nodes.
If you are using the <code>altcam</code> , <code>altclklock</code> , <code>altlvds_rx</code> , or <code>altlvds_tx</code> megafunctions, the equations shown in the Equations Section of the Compilation Report are not complete.	To view the complete equations for any of these megafunctions, use the Equations window of the Last Compilation floorplan.
The Quartus II software does not support file names with more than one extension. For example, you cannot use the file name <b>file.eda.edif</b> .	Use file names with only one extension.
If you install the Quartus II software for PCs on a UNIX server that exports shares with the Samba software version 1.9.18p10, you may experience problems accessing project files also on the network.	Altera recommends using version 1.9.16p11 or 2.0 of the Samba software.
If you make assignments to reserve pins as a group or with group notation ( <code>debug[7..0]</code> ), the Quartus II software does not correctly generate simulation output files, and you receive a warning message saying “Unsupported data type in the top-level module.”	Reserve the pins using single name notation (for example, <code>debug7</code> , <code>debug6</code> , and so on).
If you are using the <b>HSTL Class II</b> I/O standard with an APEX II device, additional information is required.	Contact the Altera Customer Applications department at <a href="mailto:apexii@altera.com">apexii@altera.com</a> for information about Service Packs and device pin-outs.
Do not change the file permissions (such as changing “read-only” to “read and write”) of Quartus II settings and configurations files ( <b>.qpf</b> , and <b>.qsf</b> ), while a Quartus II project is open.	Close the Quartus II project before making changes to the file permissions.
The order of ports for the <b>ARM<sup>®</sup>-based Excalibur MegaWizard<sup>®</sup> Plug In</b> -generated symbol for the stripe changed in version 2.0 of the Quartus II software. If you re-run the <b>MegaWizard Plug-In Manager</b> (Tools menu) for a design created in a version of the Quartus II software earlier than version 2.0, you will receive port connection errors when you compile the design.	To avoid receiving these errors, adjust the port connections in the BDF after updating the symbol.

Issue	Workaround
Node names containing numbers greater than 2 <sup>31</sup> -1 (2147483647) will cause an Internal Error in the Quartus II software.	Do not use node names containing large numbers.
Occasionally the Programmer does not allow you to use a MAX 7000AE Programmer Output File (.pof) with a MAX 7000AE device. This error sometimes occurs after a compatible MAX 7000B device is used with the MAX 7000AE POF.	Do not switch between compatible MAX 7000B and MAX 7000AE devices when a MAX 7000AE POF is loaded, or reload the MAX 7000AE POF.
The Quartus II software versions 2.1 and later no longer support the Quartus Settings File (.qsf) variable MIGRATION_DEVICES.	To specify migration device names in the QSF, use the DEVICE_MIGRATION_LIST variable. For example: DEVICE_MIGRATION_LIST = "DEVICE_A, DEVICE_B, DEVICE_C" ;
Routing back-annotation may fail if the back-annotated locations do not match the location assignments in the QSF or if the location assignments are missing. This problem can occur if you change devices, or if you remove some location assignments by using the <b>Assignment Editor</b> (Assignments menu) or by manually editing the QSF.	If you experience a “no fit” or an Internal Error while using routing back-annotation, delete the Routing Constraints File (.rcf) and back-annotate the design again after a successful compilation.
After register duplication has occurred, the duplicated register has a unique name in the form <original name>~<suffix>. The new register name may not properly inherit timing assignments made with wild cards.	Make sure that duplicated register names are included in your wild card match when making timing assignments.
You may receive an “invalid command name” error when you run an existing Tcl script that uses the Tk toolkit for its user interface. Beginning with the Quartus II software version 2.2, the Quartus II software no longer initializes the Tk toolkit automatically when starting any process.	Add the Tcl command “init_tk” to the beginning of any Tcl script that uses the Tk toolkit.
The <b>lpm_fifo MegaWizard Plug-In</b> has been removed from the Quartus II software version 2.2 and later. The lpm_fifo megafunction is still included for backward compatibility with older designs.	Altera recommends that you use the <b>"memory compiler/FIFO" MegaWizard Plug-In</b> for all new designs requiring FIFO functions.

Issue	Workaround
<p>If you receive an error message saying “System resources low...” or if the user interface is slow in responding and there is a lot of disk activity when you are not compiling a design, your system may be running out of free memory.</p>	<p>You can recover system memory by clearing messages from the Messages window. To clear messages from the Messages window, right-click anywhere in the Messages window and choose <b>Clear Messages from Window</b> (right button pop-up menu). Additional memory can be recovered by closing the Floorplan Editor.</p>
<p>Occasionally, the Quartus II software may crash or hang with no error message immediately upon opening a project.</p>	<p>Delete the Quartus Workspace File (<b>.qws</b>) <i>&lt;project name&gt;.qws</i> from the project directory. If the problem persists, delete the <i>\&lt;project directory&gt;\db</i> directory.</p>
<p>When you are setting phase shift and duty cycle values for clock signals using the <code>altpll</code> megafunction, some combinations of settings may result in values that cannot be synthesized exactly. Under certain circumstances, the Quartus II software attempts to synthesize the phase shift parameter before the duty cycle parameter.</p>	<p>You should first select values for the parameter (phase shift or duty cycle) that is most important for your design.</p>
<p>During compilation or simulation, the Quartus II software may “hang” and not proceed to the next module if a menu or modal dialog box is open at the time the current module finishes its execution.</p>	<p>Close any open menus or modal dialog boxes before the compilation or simulation reaches the next stage.</p>
<p>Running individual Quartus II software executables (<b>quartus_map</b>, <b>quartus_fit</b>, and so on) from within the Quartus II Tcl Console may cause the Quartus II software to crash.</p>	<p>You should run individual executables either from within the Quartus II scripting shell (<b>quartus_sh</b>) or directly at a command prompt.</p>
<p>If you have chosen migration devices in the <b>Compatible Migration Devices</b> dialog box, which is available from the <b>Device</b> page in the <b>Settings</b> dialog box (Assignments menu), the Timing Closure Floorplan and the Last Compilation Floorplan will display only the pins and PLLs that are common to all the selected devices. However, the Chip Editor will display all the pins and PLLs available for the device specified for compilation.</p>	

Issue	Workaround
<p>Turning <b>Physical Synthesis</b> on in the <b>Physical Synthesis Optimizations</b> page under <b>Fitter Settings</b> in the <b>Settings</b> dialog box on average will cause compilation time to double and peak memory usage to increase by approximately 20%. For large designs, the Progress Bar for the Fitter may appear to be stuck in the 50-70% range while the elapsed time continues to increase. Provided that compilation time has not increased over 10X, this is normal and the compilation should be allowed to finish. In rare cases, the compilation time may increase by more than 10X. In these cases, it is appropriate to apply the workaround if you cannot tolerate such a long compilation time.</p>	<p>If compilation time is excessive with <b>Physical Synthesis</b> turned on, you can either remove or convert LogicLock™ regions to soft before recompiling, or you can turn off <b>Physical Synthesis</b>.</p>
<p>The time shown in the Status window may not agree with the processing times reported in the Compilation Report. This difference is due to differences in how the times are calculated during processing.</p>	
<p>The following Tcl simulator commands are no longer supported by the Quartus II software version 4.0 and later:</p> <ul style="list-style-type: none"> <li>• dbg</li> <li>• get_time</li> <li>• get_value</li> <li>• force_value</li> <li>• release_value</li> <li>• read_memory</li> <li>• write_memory</li> <li>• run</li> <li>• print</li> <li>• get_memory_width</li> <li>• get_memory_depth</li> <li>• testbench_mode</li> </ul>	<p>There are new versions of most of these commands. Refer to the Tcl online help for more details. To view Tcl online help type the following command at a command prompt:  <code>quartus_sh --qhelp &lt;Enter&gt;</code></p>
<p>Occasionally you may receive an error message saying "Can't contact license server &lt;port@server&gt;..." even though you know the license server is connected and running.</p>	<p>Add an explicit port number to the SERVER line of the license file on the server in question. For example 1700@athena.</p>

Issue	Workaround
If you type a name in the entity column of the Assignment Editor that differs from an existing name only by case, the Assignment Editor's "auto-completion" feature always uses the existing name.	Type the new entity name in another application, such as a text editor, copy it to the clipboard, and paste the name from the clipboard into the Assignment Editor.
When you instantiate a new RAM or ROM memory with the <b>MegaWizard Plug-In Manager</b> , the outputs of the memory will be registered using the same clock as the inputs, by default. This is a change of behavior in that prior to the Quartus II software version 4.0, the outputs were not registered by default.	This is a change of behavior that affects only new instantiations of RAM or ROM memory. Existing memories are not affected.
If you close the RTL Viewer window while the RTL Viewer is processing a netlist (such as immediately after Analysis & Elaboration), the Quartus II software may crash.	Do not close the RTL Viewer window while it is processing a netlist.
Do not choose the <b>List paths</b> or <b>Locate</b> commands (right-button pop up menu) from the Timing Analyzer sections of the Compilation Report while a task such as compilation is running. nmj	Wait until compilation is finished before using the <b>List paths</b> or <b>Locate</b> commands from the Report window.
Opening either the Timing Closure floorplan or the Last Compilation floorplan while a compilation is running can cause the Quartus II software to crash with an internal error.	Wait until compilation is finished before opening either floorplan.
The Quartus II software may crash or display incorrect results if you open the Timing Closure floorplan and the Last Compilation floorplan at the same time.	Open only one floorplan at a time.

## Platform-Specific Issues

### PC Only

Issue	Workaround
<p>Under certain circumstances, the Quartus II installation program may crash or you may receive an error message immediately upon launching the installation program.</p>	<p>Reinstall the <b>stdole32.tlb</b> file from the original Windows distribution disks. To reinstall the file, type the appropriate command at a command prompt. (Note: the command must be typed on one line.)</p> <p><b>Windows NT:</b> &lt;CD-ROM drive letter&gt;:\i386\expand.exe stdole32.tl_ %SystemRoot%\System32\stdole32.tlb &lt;Enter&gt;</p> <p><b>Windows 2000:</b> &lt;CD-ROM drive letter&gt;:\i386\expand.exe stdole32.tl_ %SystemRoot%\System32\stdole32.tlb &lt;Enter&gt;</p> <p><b>Windows XP:</b> &lt;CD-ROM drive letter&gt;:\i386\expand.exe stdole32.tl_ %SystemRoot%\System32\stdole32.tlb &lt;Enter&gt;</p>
<p>If the full, hierarchical name of an instance exceeds 247 characters, it may not be displayed properly in the Quartus II user interface. This problem occurs most often with EDIF netlist files generated by other EDA synthesis tools.</p>	<p>Limit the full, hierarchical instance name to fewer than 247 characters if possible.</p>
<p>Path names longer than 229 characters can cause an internal error in the Quartus II software.</p>	<p>Make sure that all path names do not exceed 229 characters.</p>
<p>If you are running the Quartus II software from a network server, the Quartus II software will not run properly on the client computer if you share the <b>\quartus\bin</b> directory.</p>	<p>You must share the <b>quartus</b> directory, not the <b>\quartus\bin</b> directory.</p>

Issue	Workaround
Under some circumstances, the Quartus II software crashes when using the <b>X</b> button to close the Print Preview window if a project is open.	Use the <b>Close</b> button to close the Print Preview window if you have a project open.
The Quartus II software is not compatible with the MATLAB web server.	Turn off the MATLAB web server in the <b>Services Control Panel</b> (Start menu) before running the Quartus II software.
Under some circumstances, the Quartus II splash screen appears and the Quartus II icon appears in the Taskbar, but the graphical user interface does not appear.	The registry settings controlling the position of the Quartus II windows may have become corrupted. Type the following command at a command prompt: <code>quartus -reset_desktop &lt;Enter&gt;</code>
If you install the stand-alone Quartus II Programmer and the Quartus II software, and then uninstall either one, the Programmer may report "JTAG Server -- internal error code 82 occurred" when you click the <b>Add Hardware</b> button in the <b>Hardware Setup</b> dialog box (Edit menu). This error occurs because uninstalling the software has disabled the JTAG Server service.	Manually restart the JTAG Server service by locating the <b>jtagserver.exe</b> program and at a command prompt for that directory, type <code>jtagserver --install &lt;Enter&gt;</code>
Under certain circumstances, when you are running the Quartus II software on non-English language versions of the Windows 2000 or Windows XP operating system, the <b>Mode</b> list in the Programmer does not operate correctly.	To change programming mode, click the <b>Mode</b> list, and then type a character to select the corresponding mode. J JTAG mode I In-Socket programming mode P Passive Serial programming mode A Active Serial programming mode
Under certain circumstances the InstallShield program may fail and display "Error 5006 (0x8007003)" during initialization.	Check for an invalid <b>My Documents</b> folder and correct the shortcut to My Documents that appears on the desktop.
If you choose to uninstall a previous version of the Quartus II software during installation, and there is a "locked" file or directory, the installation program will not reboot the computer as is necessary to successfully complete the installation.	Exit from the installer and reboot the computer manually after the removal of the previous version is complete, before completing the installation of the new version.

**Solaris, HP-UX & Linux**

Issue	Workaround
The Quartus II Help is not available if you have set either the MWNO_RIT or the MWDONT_XINITTHREAD environment variables before running the Quartus II software.	Remove the variables from your environment and allow the Quartus II software to set these variables automatically, if needed.
If you are using the Exceed X server software for Windows while running the Quartus II software, the font size may be larger than the line height. This problem occurs most often if you installed the Exceed software while running at a screen resolution greater than 1024 × 768.	Reinstall the Exceed software while running at a screen resolution of 1024 × 768. You can then switch back to your normal, higher resolution setting.
Under some circumstances, there may be editor windows listed in the Window menu that you cannot see.	To display the hidden windows, choose <b>Cascade</b> (Window menu).
You cannot launch the AXD Debugger software from within the Quartus II software.	Launch the AXD Debugger software from outside the Quartus II software.
Under some circumstances, the Internet connectivity features of the Quartus II software are not functional.	Specify the full path to your web browser software on the <b>Internet Connectivity</b> page of the <b>Options</b> dialog box (Tools menu). If you access the Internet through a proxy server, you must also specify the address of the proxy server and its port number.
If you cannot access the Quartus II online Help in the user interface, you can access it by typing <code>hh quartus.chm &lt;Return&gt;</code> at a command prompt.	
When the LogicLock Regions window is floating, you cannot drag and drop node names to it from the Node Finder.	Dock the LogicLock Regions window before dragging node names to it from the Node Finder.
If you are accessing the Quartus II software through one of the following versions of the Hummingbird Exceed software (6.2, 7.0, 7.1, or 8.0) and have any Microsoft Office application or Internet Explorer open, the Quartus II user interface may start very slowly.	Contact Hummingbird Software at <b>www.hummingbird.com</b> for a patch for the Exceed software.

Issue	Workaround
If you are running the Quartus II software version 4.0 on a Linux or Solaris workstation, even though <b>Reopen current project and files at startup</b> is turned on, the last project is not reopened when you restart the software.	Use the <b>File/Project 1, 2, 3, ...</b> command (File menu) to reopen your last project.

**Solaris Only**

Issue	Workaround
The <b>ARM-based Excalibur MegaWizard Plug-In</b> , which is available from the <b>MegaWizard Plug-In Manager</b> requires the Java Runtime Environment (JRE) version 1.3, which has already been installed on your computer. On Solaris workstations, however, you may need to install extra patches to the operating system in order for JRE 1.3 to function properly.	Check the web site <a href="http://java.sun.com/j2se/1.3/install-solaris-patches.html">java.sun.com/j2se/1.3/install-solaris-patches.html</a> for information about any patches that might be needed.
If you are running the FLEXlm license server software on a Solaris server, the <b>alterad</b> daemon may fail to start and you may receive the following message: "Vendor daemon can't talk to lmgrd"	Use the following script to start the <b>lmgrd</b> daemon: <pre>#!/bin/sh ulimit -n 1024 ulimit -H -n 1024 lmgrd \$*</pre>
If you double-click or click and hold on drop-down list boxes in the Property Resource Editor the Quartus II software may crash.	

**HP-UX Only**

Issue	Workaround
You receive error messages indicating that you do not have required permissions to perform the requested operation while using Network Information Services (NIS).	Add a plus-sign (+) followed by a carriage return on a line by itself as the last line in both of the following files: <b>/etc/passwd</b> and <b>/etc/group</b> .
Programming EPC16 configuration devices has been disabled on HP-UX workstations.	
Compiling any design can cause the following warning message to be displayed during Analysis & Synthesis: "Warning: Illegal assignment keyword -- ignoring assignment"	No action is required, the message is spurious and can be ignored safely.

**Linux Only**

Issue	Workaround
<p>If the MasterBlaster™ download cable is not listed in the <b>Available hardware items</b> list in the <b>Hardware Settings</b> tab of the <b>Hardware Setup</b> dialog box, but it is connected properly, you may not have read/write permission for the serial (<code>dev/ttySx</code>) port to which the MasterBlaster cable is connected.</p>	<p>Have a system administrator assign read/write permission for the appropriate port. This change can be accomplished by adding you to the “uucp” group, or by giving read/write permission for the serial port to everyone, using the following command:  <code>chmod o+rw /dev/ttySx</code>                      where <i>x</i> is the serial port affected.</p>
<p>If you are using the ReflectionX X-server software as your display on a Linux workstation, the Quartus II software may hang and a white box may appear.</p>	<p>Set the <code>QUARTUS_MWWM</code> environment variable to <code>allwm</code> and then start the Quartus II software without the splash screen by typing the following commands at a command prompt:  <code>setenv QUARTUS_MWWM allwm &lt;Enter&gt;</code>  <code>quartus -no_splash &lt;Enter&gt;</code></p>
<p>Running a Tcl script from within the Tcl Console while a process (compilation, simulation, software build) is running in the background can cause the Quartus II software to crash with an internal error.</p>	<p>Run Tcl scripts only when compilation, simulation, or software build processes are not running.</p>
<p>If you double-click or click and hold on drop-down list boxes in the Resource Property Editor the Quartus II software may crash.</p>	
<p>When running the Quartus II software under the Red Hat Linux 8.0 operating system, the <b>LogicLock Regions Properties</b> dialog box may not be shown completely.</p>	
<p>When running the Quartus II software under the Red Hat Linux 8.0 operating system, the <b>Insert Symbol</b> dialog box and the MegaWizard Plug-In Manager window cannot be closed using the Window Close (X) button in the top right corner.</p>	<p>Right-click on the title bar of the dialog box or window and choose <b>Close</b> (right-button pop-up menu).</p>
<p>Under certain circumstances, the Quartus II software may not start properly.</p>	<p>Ensure that the <code>/etc/hosts</code> file has an entry for the hostname of the machine on which you are running. For example, if the workstation is named “orange,” there should be an entry in <code>/etc/hosts</code> with the IP address of the “orange” workstation as shown below:  <code>&lt;IP address of orange&gt; orange</code></p>

Issue	Workaround
If you are using either KDE or Gnome as your window manager on Linux 7.2 or 7.3, you may experience "trails" left on the screen when you select and drag objects in the Quartus II Block Editor.	
If you are running the Quartus II software version 4.0 using VNC software, the Quartus II software may terminate unexpectedly whenever you open any file or browse any directory from within the Quartus II software.	Make sure your VNC server software is version 3.3.4 or later.
If you are running the Quartus II software under Red Hat Linux 7.3, you may experience substantial degradation of compilation times if your design files are located on a separate server from the Quartus II software.	Make sure that the operating system kernel is upgraded to the latest available. If you are using a NetApps server, refer to the following URL for more information: <a href="http://www.netapp.com/tech_library/3183.html">http://www.netapp.com/tech_library/3183.html</a>
The Quartus II software will crash with a core dump when you open the online help if the .mw directory in your home directory does not exist.	Start and then exit from, the Quartus II software at least once before opening the online Help.

## Device Family Issues

### Mercury

Issue	Workaround
If your Quartus II software version 1.0 or 1.1 design for a Mercury device uses the altlvds_tx or altlvds_rx megafunction, and you archived the design, you may have functional problems in your design, including inverted signals.	Delete the altlvds_tx or altlvds_rx megafunction from the design and replace it with the version included with the current version of the Quartus II software before compiling your design in the Quartus II software version 2.1 or later.

### APEX 20K

Issue	Workaround
To use the EP20K400GC655 device in your design, please contact the Altera Customer Applications Department.	

**Excalibur**

Issue	Workaround
<p>You may receive the message “System Build Descriptor File missing parameter programming_clock_frequency” for System Build Descriptor Files (.sbd) generated in the Quartus II software version 2.0 and earlier, after selecting the <b>Boot from Serial</b> option in the <b>ARM-based Excalibur MegaWizard Plug-In</b>.</p>	<p>Rerun the <b>ARM-based Excalibur MegaWizard Plug-In</b> in the current version of the Quartus II software to regenerate the SBD File and correct the error.</p>
<p>If you are using the Stripe-to-PLD Bridge in Excalibur EPXA10 Devices, your design may not function due to the Stripe-to-PLD Bridge lockup errata if either of the following options is turned on in the Quartus II software:  <b>Remove Redundant Logic Cells</b>  <b>Perform WYSIWYG Primitive Resynthesis</b>                      Please refer to the EPXA10 Device Errata Sheet for details on the device errata.</p>	<p>To avoid bridge lock-up, ensure that the <b>Remove Redundant Logic Cells</b> option is turned off for the project.                      If the <b>Perform WYSIWYG Primitive Resynthesis</b> option is turned on for your project, you may receive warnings that the stripe signals were not routed correctly. To eliminate the warnings, re-run the <b>MegaWizard Plug-In Manager</b> in the Quartus II software version 2.2 or later. This procedure will create an additional settings file (<b>alt_exc_stripe.esf</b>) to ensure that the required logic elements are implemented.</p>

Issue	Workaround
<p>Designs targeting Excalibur devices that use Boot-from-Flash mode may not operate when downloaded to the target board if the Quartus II Software Builder or SOPC Builder Excalibur-build script was used to generate the flash programming file.</p>	<p>The Excalibur boot loader in the Quartus II software version 3.0 does not function correctly if the Quartus II Software Builder is used to generate the flash programming file. This is because the compression option that is used with the <b>makeprogfile</b> utility during the software build process does not work with this version of the bootloader. To work around this issue, do not use the Software Builder to generate a programming file, but instead use the <b>makeprogfile</b> utility at the command line with the <b>-nc</b> (no compression) option. If you are using the SOPC Builder Excalibur-build script, you must edit the script located in the <b>\&lt;XA dev kit instalationl directory&gt;\bin</b> folder. Modify line 1034 of this script to remove the <b>-nc</b> option. For example, line 1034 should be changed as shown in this example.</p> <pre>\$command = "makeprogfile -nc -b \${fileBase}_bootdata.o \$SBD \$SBI \${fileBase}.hex";</pre> <p>You must recompile your software project for this change to take effect.</p>
<p>If you are developing new designs with the XA MegaWizard, you should manually import the file settings from the <b>&lt;block_name&gt;.esf</b> file into the Quartus Settings File (<b>.qsf</b>) using the <b>Import Assignments</b> command (Assignments menu). This ensures that the Quartus II software does not remove certain cells and uses the inverting input on the stripe interface, which does not work.</p>	

**Cyclone, Stratix & Stratix GX**

Issue	Workaround
Using the Resource Property Editor to invert the clock signal of a logic cell that has a clock enable signal when other logic cells in the same LAB share both the clock and clock enable signals will pass the netlist checks run by choosing the <b>Check and Save All Netlist Changes</b> command (Edit menu) but may cause the Quartus II software to crash with an internal error in the Assembler.	Invert the clock signal on all logic cells with common clock and clock enable signals. Inverting only one clock signal in the LAB requires that you change your source.
Under certain circumstances, a LogicLock region in the design appears after compilation as a 1 x 1 block in the lower left corner of the device floorplan.	This problem can occur when both the <b>Automatically route signal probe signals</b> option on the <b>Signal Probe</b> page and the <b>Use Smart Compilation</b> option on the <b>Compilation Process</b> page in the <b>Settings</b> dialog box (Assignments menu) are turned on. To prevent this problem from occurring in the future, perform the following steps: Turn off the <b>Smart Compilation</b> option. <i>or</i> 1. Turn on the <b>Preserve fewer node names</b> option. 2. Turn off the <b>Automatically route signal probe signals</b> option. 3. Recompile your design. 4. Create the desired LogicLock regions.
When you use a Routing Constraints File (.rcf) to control fitting after performing Routing Back-Annotation, your timing analysis results may change slightly due to parasitic and other effects. Any change will be very small.	
If you use the SignalProbe™ feature to observe the signals at an output pin, by routing them to another output pin, the SignalProbe output pin signal will be shown as Unknown (X) in the Quartus II Simulator.	The signal will be correct in actual operation, the error appears only in the Quartus II Simulator.

Issue	Workaround
<p>In the <b>SignalProbe Source to Output Delays</b> table of the Timing Analyzer Report, the following right-button menu commands are not available although they are available in other similar Timing Analyzer Report tables:</p> <ul style="list-style-type: none"> <li>• <b>List Paths</b></li> <li>• <b>Locate in Chip Editor</b></li> <li>• <b>Locate in Timing Closure Floorplan</b></li> <li>• <b>Locate in Last Compilation Floorplan</b></li> </ul>	<p>You can use other Timing Analyzer Report tables to list and locate the affected paths.</p>

**Stratix and Stratix GX**

Issue	Workaround
<p>If you use the <code>altdio_bidir</code> or <code>alt_dqs</code> megafunction and connect any data port directly to VCC or GND, the Quartus II software version 3.0 SP1 and later will insert an additional logic element in the circuit path.</p>	
<p>The behavior of the 0-degree phase shift setting of the <code>DLL_PHASE_SHIFT</code> parameter of the <code>altdqs</code> megafunction or the <b>DQS Phase Shift</b> logic option with the <code>altdio_bidir</code> megafunction has changed in the Quartus II software version 3.0 SP2. The previous behavior produced an uncharacterized delay that cannot be specified to fall within the specified 500 ps delay difference.</p>	<p>If your design uses this setting and does not work correctly after installing the Quartus II software version 3.0 SP2, you should contact the Altera Applications department for further information.</p>

**Stratix**

Issue	Workaround
<p>Versions of the Quartus II software earlier than version 3.0 SP1 did not correctly implement the fast PLL normal mode compensation delay in EP1S40 devices. The Quartus II software will not warn of this condition when compiling designs created with the Quartus II software earlier than version 2.2.</p>	<p>The Quartus II software version 3.0 SP1 implements the feature correctly. If your design was created with the Quartus II software version earlier than 3.0 SP1, you should recompile your design to obtain the correct results. If your design requires using the previous results, you can specify the following values for the <code>clk&lt;n&gt;_phase_shift</code> parameter for each clock port you are using in the <code>altpll</code> megafunction:                      Center PLL (PLLs 1, 2, 3, 4) : -1990 ps                      Corner PLLs (PLLs 7, 8, 9, 10) : -420 ps</p>
<p>Versions of the Quartus II software earlier than version 2.2 did not correctly implement the following functions in DSP blocks in Stratix devices:</p> <ul style="list-style-type: none"> <li>• Mixed-sign multiplications of 19 bits and greater</li> <li>• Dynamic-sign multiplications of 19 bits and greater</li> <li>• Signed multiplications greater than 36 bits</li> </ul>	<p>Designs that implement DSP functions must be recompiled in the Quartus II software version 2.2 or later. The current version of Quartus II software implements the design correctly, but uses more resources and has reduced performance from earlier versions.</p>
<p>Designs compiled for Stratix EP1S40ES devices must be recompiled for the EP1S40 device before programming.</p>	
<p>Stratix PLL simulation models have been enhanced to handle jitter on the input clock. This enhancement has the unintended side effect that functional simulations for LVDS designs using cascaded PLLs may be incorrect by one clock cycle.</p>	<p>Altera recommends that you perform Timing Simulation to display the correct behavior in the Quartus II Simulator or in other EDA Simulators.</p>

**Changes to Stratix PLL Timing:**

<b>Enhanced PLL Maximum VCO Frequency (MHz)</b>			
<b>Speed Grade</b>	<b>-5</b>	<b>-6</b>	<b>-7</b>
Quartus II Ver. 2.2	1000	1000	1000
Stratix Datasheet Ver. 3.0	800	800	800
Quartus II Ver. 2.2 SP1	800	800	600

<b>Fast PLL Maximum VCO Frequency (MHz)</b>			
<b>Speed Grade</b>	<b>-5</b>	<b>-6</b>	<b>-7</b>
Quartus II Ver. 2.2	1000	1000	1000
Stratix Datasheet Ver. 3.0	840	840	840
Quartus II Ver. 2.2 SP1	1000	1000	700

**For Enhanced PLLs (EPLLs):**

The Quartus II software version 2.2 SP1 and later will enforce the 300–800 MHz maximum VCO frequency range as specified in the Stratix device family data sheet for -5 and -6 speed grades. The PLL VCO frequency range for the -7 speed grade is 300–600 MHz.

**For Fast PLLs (FPLLs):**

The Quartus II software version 2.2 SP1 and later will continue to support the 300–1000 MHz PLL VCO frequency range when the FPLL is used as a general purpose PLL. The higher PLL VCO frequency range enables more flexibility in choosing multiplication and division factors in the Quartus II software. When the FPLL is used in Source Synchronous mode, the PLL VCO frequency range is unchanged from the data sheet specification of 300–840 MHz.

**Stratix GX**

<b>Issue</b>	<b>Workaround</b>
The Quartus II software version 3.0 Service Pack 1 also supports PowerGauge™ simulation-based power estimation for the Stratix GX device family. The power estimation is calculated based upon the number of channels used per transceiver block, the toggle rate of the output and the data transfer rate.	

Issue	Workaround
<p>In the Quartus II software version 3.0 and earlier, unused Stratix GX dedicated GXB reference clock pins were marked GND+ in the Quartus II-generated Pin-Out file (.pin) and Compilation Report. No recommendations were made for connecting unused GXB Receiver and Transmitter pins.</p> <p>In the Quartus II software version 4.0, Altera recommends that unused GXB Receiver, Transmitter, and dedicated reference clock positive pins be connected to VCC (1.5V) through a 10 KOhm resistor, while unused GXB Receiver, Transmitter and dedicated reference clock negative pins are connected to GXB_GND through a 10 KOhm resistor.</p>	
<p>Under certain circumstances, you may receive the following error message when compiling designs targeting Stratix GX devices:</p> <pre>"Internal Error: Sub-system: ASM, File: asm_cdr.cpp, Line: 840, Illegal Clock Placement. Problem between Quad PLL and the Quad Clock Pad. PLL has Reset connected."</pre>	<ul style="list-style-type: none"> <li>• Remove the TX PLL areset connection from the GXB block.</li> </ul> <p>or:</p> <ul style="list-style-type: none"> <li>• Do not use the dedicated refclk pad in the GXB Quad to provide the reference clock to the TX PLL or to the receiver.</li> </ul> <p>or:</p> <ul style="list-style-type: none"> <li>• Ensure that the clock signal placed on the refclk pad in the GXB Quad does not have a TX PLL with its TX PLL areset port connected.</li> </ul>
<p>Under certain circumstances, you may receive the following error message when compiling designs targeting Stratix GX devices:</p> <pre>"Internal Error: Sub-system: ASM, File: asm_cdr.cpp, Line: 839, llegal Clock Placement. Problem between Quad PLL and the Quad Clock Pad. PLL has Enable connected."</pre>	<ul style="list-style-type: none"> <li>• Remove the TX PLL enable connection from the GXB block.</li> </ul> <p>or:</p> <ul style="list-style-type: none"> <li>• Do not use the dedicated refclk pad in the GXB Quad to provide the reference clock to the TX PLL or to the receiver.</li> </ul> <p>or:</p> <ul style="list-style-type: none"> <li>• Ensure that the clock signal placed on the refclk pad in the GXB Quad does not have a TX PLL with its TX PLL enable port connected</li> </ul>

Issue	Workaround
<p>Under certain circumstances, you may receive the following error message when compiling designs targeting Stratix GX devices:</p> <pre>"Internal Error: Sub-system: ASM, File: asm_cdr.cpp, Line: 863, Illegal Clock Placement. Problem between RX Channel Resets and the Quad Clock Pad. All RX's in Quad have Resets connected."</pre>	<ul style="list-style-type: none"> <li>• Remove one or more of the RX analogreset connections from the GXB block</li> </ul> <p><i>or:</i></p> <ul style="list-style-type: none"> <li>• Do not use the dedicated refclk pad in the GXB Quad to provide the reference clock to the TX PLL or the Receiver.</li> </ul> <p><i>or:</i></p> <ul style="list-style-type: none"> <li>• Ensure that the clock signal placed on the refclk pad in the GXB Quad does not have Receivers with all of their rxanalog reset ports connected</li> </ul>

**Stratix II**

Issue	Workaround
<p>Back-annotating some designs targeted to a Stratix II device with the <b>Demote cell assignments to</b> option set to <b>LABs</b> may prevent the design from fitting.</p>	<p>Back-annotate the design with <b>Demote cell assignments to</b> turned off.</p>
<p>When the Stratix II DSP block is used with its accumulator, the maximum frequency is reported to be 289 MHz. The correct maximum frequency is 363 MHz. This error is caused by incorrectly calculating the delay on the feedback path to the accumulator. This issue does not affect families other than Stratix II and will be fixed in the Quartus II software version 4.0 Service Pack 1. If your design uses a Multiply-Accumulate (MAC) block that is on your critical path, your performance will improve after installation of the service pack.</p>	<p>Make <b>Cut Timing Path</b> assignments between all DSP output nodes, and the maximum reported frequency should return to 363 MHz.</p>
<p>If you are compiling a design for a Stratix II device that was originally targeted to a Stratix device, you may receive the following error message from the <b>quartus_map</b> executable if the design uses PLLs that have external clock outputs:</p> <pre data-bbox="251 1255 795 1499">"Info: Messages issued during the elaboration of &lt;design entity&gt; Error: PLL pll uses extclk[2] output clock port, which cannot be remapped to clk port because target device does not have enough available clk ports."</pre>	<p>Enhanced PLLs on Stratix II devices have fewer output taps than Enhanced PLLs on Stratix devices. Therefore, you must reduce the number of taps on that PLL. If two taps have exactly the same configuration including their enables, you can merge them into a single tap. You must re instantiate the PLL in your source code with the <b>MegaWizard Plug-In Manager</b>, and recompile the design.</p>

## Cyclone

Issue	Workaround
Altera recommends that the frequency of the external clock output of the PLLs be limited to 312 MHz.	
The Cyclone EP1C3T100 device does not support the <b>LVDS</b> I/O standard on any pins.	Use the Cyclone EP1C3T144 device instead. It supports the <b>LVDS</b> I/O standard.
The operating frequency range of the PLL has been changed. In the Quartus II software version 3.0 and earlier, the range was 300 MHz to 800 MHz. In version 3.0 Service Pack 1 and later, that range changed to 500 MHz to 1000 MHz because of concerns about jitter at frequencies below 500 MHz. Because of this change, the minimum input frequency is now 15.625 MHz (previously 15 MHz) and the minimum output frequency is also 15.625 MHz (previously 9.38 MHz).	Recompile your design after installing the current version of the Quartus software.
The PLL lock circuit does not function correctly for PFD (Phase Frequency Detector) frequencies below 200 MHz when the temperature is below -20°C.	If operation at temperatures below -20°C is required, choose a higher input frequency and clock division (N) factor such that the PFD input frequency is higher than 200 MHz.

## Design Flow Issues

### Verification

Issue	Workaround
If you select <b>SignalTap II: pre-synthesis</b> or <b>SignalTap II: post-fitting</b> in the <b>Filter</b> list of the Node Finder and select a bus to add to the STP File, the Quartus II software may expand the bus into individual nodes that may be removed during synthesis, resulting in an error.	Delete the nodes and recompile the project. You can select individual nodes in the Node Finder and group them in the SignalTap II window using the <b>Group</b> command (Edit menu).

**Integrated Synthesis (VHDL and Verilog HDL)**

Issue	Workaround
The Quartus II software version 4.0 may give the message “Error: Duplicate entity <name> found in file <filename1> colliding with the one found in file <filename2>,” for a project that compiled successfully with Quartus II 2.2 or earlier.	The Quartus II software version 2.2 and earlier versions gave a warning when they encountered a duplicate definition of a VHDL or Verilog HDL entity and ignored the duplicate. The Quartus II software version 4.0 gives an error message when it finds two or more definitions of a VHDL or Verilog HDL entity in the same project. To avoid this error in the future, remove the duplicate entity or entities.
The Quartus II software version 4.0 may give the message “Error: unsupported choice with meta-value ‘X’” (or ‘-’) for a project that compiled successfully with the Quartus II software version 2.2 or earlier. This occurs in a case statement that uses the metavalues ‘X’ or ‘-’.	Previous versions of the Quartus II software ignored a case item with a metavalue and printed a warning message. However, this can cause simulation-synthesis mismatches and this design style can also be synthesized differently with other synthesis tools. To match the behavior of the Quartus II software version 2.2, delete the case item that contains the metavalue. If this is not the behavior you want, modify your design to avoid the use of ‘X’ in the case statement.

**Verilog HDL Integrated Synthesis**

Issue	Workaround
Verilog-2001 mode is enabled by default. This mode can cause some issues with Verilog-1995 designs, most commonly due to new reserved words in Verilog-2001 such as <code>config</code> .	Do not use Verilog-2001 reserved words as identifiers or select <b>Verilog-1995</b> on the <b>Verilog HDL</b> input page under <b>HDL Input Settings</b> of the <b>Settings</b> dialog box (Assignments menu).
Verilog HDL escaped names that look like vectors can cause problems in the Quartus II software. For example, if you have a single-bit component port named <code>\my_vector_port[3:0]</code> , the Quartus II software versions 2.1 and later will treat it as an array port.	You should avoid using escaped port names in the Quartus II software version 2.1 and later.

Issue	Workaround
<p>The Quartus II software version 4.0 gives the message “Error: illegal Procedural Assignment to nonregister data type &lt;name&gt;,” or “Error: illegal continuous assignment to non-net data type &lt;name&gt;,” for a project that compiled successfully with the Quartus II software version 2.2 or earlier.</p>	<p>The Quartus II software version 4.0 enforces the distinction between <code>reg</code> data types and <code>wire</code> data types, as required in the Verilog HDL standard. The Quartus II software version 2.2 and earlier did not enforce this distinction. To avoid receiving this error in the future, declare the variable as a <code>wire</code> when you use a continuous assignment, and as a <code>reg</code> when you use a procedural assignment.</p>
<p>Some designs that compiled successfully in the Quartus II software version 3.0 may fail with the error message "Value cannot be assigned to input &lt;name&gt;."</p>	<p>The Quartus II software version 4.0 does not allow an assignment to an input. Change the port to be of type output.</p>
<p>Some designs that compiled successfully in the Quartus II software version 3.0 may fail with the error message "Index Z cannot be outside range (x to y) of array &lt;name&gt;."</p>	<p>The Quartus II software version 4.0 does not allow out-of-bounds array accesses. The Quartus II software version 3.0 would return "don't care". You must rewrite your design to keep array accesses within the valid range of the array.</p>

**VHDL Integrated Synthesis**

Issue	Workaround
<p>Recursive VHDL entities are not supported by the Quartus II software versions 2.1 and later.</p>	
<p>A VHDL design that compiles successfully in the Quartus II software version 3.0 or earlier may fail when compiled with the Quartus II software version 4.0. The error messages will be similar to this example:                  "Error: VHDL error at &lt;location&gt;: object &lt;some_name&gt; is used but not declared."                  The entity with the problem will contain a use clause similar to the following example:                  use &lt;user_library&gt;.all;</p>	<p>The Quartus II software version 3.0 imports the declarations in the &lt;user_library&gt; and in the <b>work</b> library when it processes the use clause. This sometimes causes declarations to be imported more than once, which leads to VHDL compilation errors. The Quartus II software version 4.0 does not look in the <b>work</b> library when it encounters this use clause. To fix your design, you can explicitly add a use clause to look in the <b>work</b> library (use <code>work.all</code>); or you can import the specific declarations that you need rather than the entire <b>work</b> namespace.</p>

<p>If a syntax error occurs at the end of a Verilog HDL or VHDL design file, sometimes the Quartus II software will give this generic error:          Verilog HDL syntax error near end of file  <i>or</i>          VHDL syntax error: experienced unexpected end_of_file -- delimiter or keyword may be missing          It will not give a file name or line number for the error.</p>	<p>This error occurs most often when you have a missing keyword, for example a missing "endmodule" statement at the end of a Verilog HDL file or a missing "END ;" at the end of a VHDL file. You can check the syntax of each individual file with the <b>Analyze Current File</b> command (Processing menu) to identify the file that is causing the problem.</p>
<p>The Quartus II software version 4.0 incorrectly synthesizes some VHDL state machines that assign tri-state ('Z') values to a state machine output.</p>	<p>Change your design so that you do not directly assign tri-state values to the state machine outputs. You can introduce temporary signals to store the tri-state enable signal and any driving value for the actual output, and add a separate process statement to create the tri-state values.</p>
<p>Using the default component declaration for the <code>altsyncram</code> megafunction provided with the Quartus II libraries for VHDL may not work correctly.</p>	<p>Use the MegaWizard Plug-In Manager to instantiate the megafunction.</p>

**Chip Editor, Change Manager, and Resource Property Editor Issues**

Issue	Workaround
<p>If the Netlist Explorer is open and you choose <b>Check and save all netlist changes</b> (right button pop-up menu), the Quartus II software will crash with an internal error the next time you open the Netlist Explorer.</p>	<p>Close the Netlist Explorer before running the <b>Check and save all netlist changes</b> command.</p>
<p>If the Assembler is run after changes are made in the Resource Property Editor but before performing <b>Check and save all netlist changes</b>, the Change Manager will erroneously report the status of the changes as Committed. The changes will not be implemented because they were not explicitly saved.</p>	<p>Either run <b>Check and save all netlist changes</b> before running the Assembler, or close and reopen the project.</p>

## SOPC Builder Issues

Issue	Workaround
If the Quartus II software is installed in a directory having space characters in its name, the SOPC Builder software will not run.	Install the Quartus II software in a directory that does not have space characters in the path.
When adding an Excalibur Stripe component in conjunction with Avalon peripherals, you may encounter SOPC Builder errors indicating too many masters are present.	If the master-connection patch-panel is not visible, choose <b>Show Master Connections</b> (View menu). Then click on the master/slave intersection indicated by the error message. This will remove the connection. Click again to restore the connection and the error will not reappear.
Designs targeting Excalibur devices that use Boot From Flash mode may not operate when downloaded to the target board if the Quartus II Software Builder or SOPC Builder Excalibur-build script was used to generate the flash programming file.	<p>The Excalibur boot loader in the Quartus II software version 3.0 does not function correctly if the Quartus II Software Builder is used to generate the flash programming file. This is because the compression option that is used with the <b>makeprogfile</b> utility during the software build process does not work with this version of the bootloader. To work around this issue, do not use the Software Builder to generate a programming file, but instead use the <b>makeprogfile</b> utility at the command line with the <b>-nc</b> (no compression) option. If you are using the SOPC Builder Excalibur-build script, you must edit the script located in the <b>\&lt;XA dev kit install directory&gt;\bin</b> folder. Modify line 1034 of this script to remove the <b>-nc</b> option. For example, line 1034 should be changed as shown in this example.</p> <pre>\$command = "makeprogfile -nc -b \${fileBase}_bootdata.o \$SBD \$SBI \${fileBase}.hex";</pre> <p>You must recompile your software project for this change to take effect.</p>
The SOPC Builder and Nios Software Development Kit shell may "hang" and become unresponsive when run while the Frisk antivirus software is running.	Turn off the Dynamic Virus Checking feature of the Frisk software before running SOPC Builder or the Nios SDK shell.

## SOPC Builder Compatibility

### ***Nios version 3.1 and later***

You can use your existing Nios components and they will be recognized automatically by the SOPC Builder integrated into the Quartus II version 4.0 software.

### ***Nios version 2.2 / SOPC Builder 2.7***

Your Nios components are not compatible with the SOPC Builder integrated with the Quartus II version 3.0 software. You will receive upgraded Nios components as part of a new Nios Development Kit. You can run your earlier version of SOPC Builder by following these steps:

1. If Altera SOPC Builder 2.7 is not shown in the **MegaWizard Plug-In Manager**, reinstall the SOPC Builder version 2.7 software, or copy the **sopc\_builder\_2\_7\_wizard.lst** file into your **\quartus\libraries\megafunctions** directory.
2. When you open a system that uses the Nios version 2.2 embedded processor, you will be given the choice of using the Altera SOPC Builder or the Altera SOPC Builder 2.7. Choose the 2.7 version. If you choose the version without a number (version 3.0) your components will be disabled.

## EDA Integration Issues

Issue	Workaround
<p>The current version of the Quartus II software allows you to select the Synplicity Amplify software as a physical optimization tool. However, this setting is for ATOPS mode, which is currently not supported by the Amplify software.</p>	<p>Contact Synplicity for the support schedule for the Amplify software ATOPS mode.</p>
<p>The directory containing the ARM-based Excalibur stripe models changed in the Quartus II software version 2.0. This change may cause compilation scripts that were created for earlier versions of the Quartus II software to fail.</p>	<p>Edit your compilation scripts so that the models and simulation wrapper files are located in the following directory:  <code>\quartus\eda\sim_lib\excalibur\stripe_model_&lt;operating system&gt;\ModelGen\models\epxa&lt;I   4   10&gt;\r0\&lt;simulator_language&gt;</code></p>
<p>There is not an option in the installation program to install the EDA tool interface for the Cadence Concept software, even though the software is supported by the Quartus II software version 2.2 and later.</p>	<p>Select Cadence Verilog-XL in the installation to install the <b>cadence.tcl</b> interface script in your <code>\&lt;Quartus II installation&gt;\eda\cadence</code> directory.</p>
<p>The Cadence NC-VHDL version 3.4 software requires the s013 patch, which contains a more stable version of the NC-VHDL software.</p>	<p>Install the s013 patch, available from Cadence, for the NC-VHDL software before simulating designs.</p>
<p>The Quartus II software generates Verilog Output Files (.vo) and VHDL Output Files (.vho) with the name of the current Quartus II project as the file name.</p>	<p>To simulate the subentity of a design with EDA simulation tools, rename the Verilog or VHDL Output File with the name of the subentity to be simulated.</p>
<p>Support has been added for generation of IBIS Output Files (.ibs) for EPCS1 and EPCS4 Serial Configuration Devices.</p>	<p>The IBIS file will be generated in the <code>\&lt;project name&gt;\board\ibis</code> directory after compilation when the design is targeted to a Cyclone device and Active Serial configuration scheme using EPCS1 or EPCS4 devices is chosen.</p>
<p>When simulating designs targeted to Stratix GX devices in the Synopsys VCS software version 7.0.1 you may receive an error saying "Assertion failed "0" at line 669 in file alias.c"</p>	<p>Simulate your design using the Synopsys VCS software version 7.0 or use the <code>+newpli</code> directive in the version 7.0.1 software</p>

<b>Issue</b>	<b>Workaround</b>
A Synplicity VQM project that compiles successfully in the Quartus II software version 3.0 or earlier may fail when compiled with the Quartus II software version 4.0 with errors "Port A_IN does not exist in primitive <PRIM> of instance <inst_name>" and "Port A_OUT does not exist in primitive <PRIM> of instance <inst_name>"	This error can occur if your Quartus II project specifies that the Synplicity-generated VQM is a Verilog HDL file. Change the file type of the VQM to Verilog Quartus Mapping File in the <b>Properties</b> dialog box of the <b>Files</b> page of the <b>Settings</b> dialog box (Assignment menu)
NativeLink support does not work with versions of Precision RTL Synthesis Software earlier than version 2003b) due to a change in Precision's project API.	

## Simulation Model Changes

### altera\_mf Models

#### RAM Models

Model	Change
altsyncram	<ul style="list-style-type: none"> <li>Added support for Stratix II devices</li> <li>Output 'X' when byte-enable is de-asserted. The corresponding data bytes are not written into the memory array.</li> <li>Aligned the behavior during initialization               <ul style="list-style-type: none"> <li>All addresses are initialized to zeros</li> <li>If set to ROM, the output register and output port should always be initialized to zeros</li> </ul> </li> </ul>
scfifo	<ul style="list-style-type: none"> <li>Fixed read pointer wrap around problem when <code>lpm_showahead</code> is ON.</li> </ul>
alt3pram	<ul style="list-style-type: none"> <li>Added support for Stratix, Stratix GX and Cyclone device families.</li> </ul>

#### DSP Models

Model	Change
altmult_add	<ul style="list-style-type: none"> <li>Added support for Stratix II.</li> </ul>
altmult_accum	<ul style="list-style-type: none"> <li>Added support for Stratix II.</li> </ul>

#### I/O Models

Model	Change
altpll	<ul style="list-style-type: none"> <li>Added support for Stratix II.</li> <li>Updated Stratix PLL "lock" to "unlock" time. This enables the PLL to release lock after a maximum two <code>refclk</code> periods when input clock stops.</li> <li>Added support for new output ports <code>enable0</code> and <code>enable1</code> to supply load enable signals for LVDS.</li> <li>Added support to enable downstream PLL output clock (in a cascaded PLL chain) always in phase with its input clock.</li> </ul>
altlvds_tx	<ul style="list-style-type: none"> <li>Added support for Stratix II.</li> <li>Fixed "index out of bound" problem during data serialization after PLL is reset.</li> </ul>

Model	Change
altlvds_rx	<ul style="list-style-type: none"> <li>Added support for Stratix II.</li> <li>Under Stratix II, rx_data_align port will be treated as rx_channel_data_align port with additional latency added for each data alignment signal.</li> <li>Under Stratix, serial input data must be input right after (1) the receiver has locked, and (2) needs to be on the 3<sup>rd</sup> PLL fast clock cycle after the rising edge of PLL slow clock (rx_outclock).</li> <li>Updated Stratix GX DPA connection to get the output registers always clocked by rx_coreclk instead of PLL's slow clock when rx_coreclk is used (USE_CORECLOCK_INPUT=ON) and output is registered (REGISTERED_OUTPUT=ON).</li> <li>Use load enable signal from PLL to load input data on the first slow clock cycle after the PLL is locked. This reduces one additional clock cycle needed to get the data right.</li> </ul>
altdio_out	<ul style="list-style-type: none"> <li>Able to output dataout_h or dataout_l when clocken is deasserted.</li> </ul>

## 220Model

Model	Change
lpm_mux	<ul style="list-style-type: none"> <li>Added in checks to output 'X' if the input port SEL value is out of range.</li> </ul>
lpm_compare	<ul style="list-style-type: none"> <li>Added support for data more than 32bits.</li> </ul>
lpm_add_sub	<ul style="list-style-type: none"> <li>Added support for data more than 32bits.</li> </ul>

## Latest Known Quartus II Software Issues

For known software issues after publication of this version of the Quartus II Software Release Notes, please look for information in the **Quartus II Latest Known Issues** section of the Altera Support Knowledge Database at the following URL:

**[http://answers.altera.com/altera/index.jsp?/Topics/Support Solutions/Known Issues/Software/Quartus II](http://answers.altera.com/altera/index.jsp?/Topics/Support/Solutions/Known%20Issues/Software/Quartus%20II)**

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