



Quartus II Software Release Notes

December 2004

Quartus II version 4.2

This document provides late-breaking information about the following areas of this version of the Altera® Quartus® II software. For information about memory, disk space, and system requirements, refer to the **readme.txt** file in your `\altera\quartus<version number>` directory.

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New Features & Enhancements

The Quartus II software version 4.2 includes the following new features and enhancements:

- PowerPlay Power Analyzer — enables designers to accurately analyze and optimize both dynamic and static power.
- Physical synthesis performance enhancement — Physical synthesis has been augmented to increase f_{MAX} even further. In addition, the compilation time overhead of physical synthesis has been decreased.
- Pin-out support for members of Cyclone™ II device family.
- Full device support for Stratix® II EP2S130 devices.
- Full device support for EPCS64 configuration devices.
- Incremental synthesis — allows you to synthesize an isolated portion of your design to which you made design changes. Resynthesizing only the changed portions of your design reduces synthesis time and run-time memory use.
- In-System Memory Content Editor — now allows you to select specific memory address ranges of data and the ability to quickly replace your selections with new standard or custom values.
- Soft LVDS Megafunction — Simplifies implementing LVDS communication with Cyclone II and Cyclone devices.
- SignalTap® II Logic Analyzer — new commands in the Advanced Trigger Condition Editor allow you to more easily manipulate items and conditions.
- Early timing estimate — you can obtain an estimate of your design's timing performance before completing the fitting process.
- Platform migration — project and design files created on one platform or in one directory can now be moved to another platform or directory.
- Revisions — enhancements to the Revisions feature now allow you to see and compare settings and results across multiple revisions.
- New Timing Analysis and Fitting Features — New features analyze and control clock skew, allow the designer to model clock jitter, and enable better analysis and optimization of control signals.

Project & Settings Files In This Release

The method that the Quartus II software version 4.0 and later uses to store assignments has changed substantially from the method used by the Quartus II software version 3.0 and earlier.

If you wish to work on a project you created using the Quartus II software version 3.0 or earlier, you should open and save the project in the GUI once, even if you are using the command-line executables to compile your project. Opening and saving your project in the GUI ensures that your setting and assignment files are converted properly.

When you open a project created in the Quartus II software version 3.0 or earlier, the following changes are made to your assignment and setting files:

- Your *<project>.quartus* file is converted to the new Quartus Project File (**.qpf**) format, and the original file is moved to the *\<project>\<project>.bak* directory.
- The contents of your Compiler Settings File (**.csf**), Entity Settings File(s) (**.esf**), Simulation Settings File (**.ssf**), Project Settings File (**.psf**), and Software Build Settings File (**.fsf**) are merged into the new Quartus Settings File (*<project>.qsf*), and the original files are moved to the *\<project>\<project>.bak* directory.
- Once the Quartus II software has converted your files and moved the originals to the backup directory, the original files will not be used by the Quartus II software, so subsequent changes made to those files will be ignored.

Device Support & Pin-Out Status

This section contains information about the status of support in the Quartus II software for the listed devices.

Full Device Support

Full compilation, simulation, timing analysis, and programming support is now available for the following new devices and device packages:

Devices with Full Support

Device Family	Devices	
Stratix II	EP2S60F484ES	EP2S60F672ES
	EP2S60F1020ES	

Advance Device Support

Compilation, simulation, and timing analysis support is provided for the following devices that will be released in the near future. Although the Compiler generates pin-out information for these devices, it does not generate programming files for them in this release.

Devices with Advance Support

Device Family	Devices	
Cyclone II	EP2C5	EP2C8
	EP2C20	EP2C35
	EP2C50	EP2C70
Stratix II	EP2S90F780C4	EP2S130F780C4
	EP2S90F780C5	EP2S130F780C5

Initial Information Support

Compilation, simulation, and timing analysis support is provided for the following devices that will be released in the near future. Programming files and pin-out information, however, are not generated for these devices in this release.

Devices with Initial Information Support

Device Family	Devices
None	

Devices Not Shown in this Version

The following devices are not shown in this version of the Quartus II software. Existing designs using these devices are still supported, but these devices are not recommended for new designs. Contact Altera Applications for more information.

Devices No Longer Shown in the Quartus II Software

Device Family	Devices	
Mercury™	EP1M120F484I6	EP1M350F780I6
APEX™ 20K	EP20K30EQC208-1	EP20K30EQC208-1X
	EP20K30EQC208-2	EP20K30EQC208-2X
	EP20K30EQC208-3	EP20K60EBC356-1
	EP20K60EBC356-1X	EP20K60EBC356-2
	EP20K60EBC356-2X	EP20K60EBC356-3
	EP20K60EFI144-2X	EP20K60EFI324-2
	EP20K60EFI324-2X	EP20K60EQI208-2X
	EP20K100EQI240-2X	EP20K100EBI356-2X
	EP20K200CQ208C7	EP20K200CF484I8
	EP20K200CQ208C9	EP20K200CQ208C8
	EP20K200EBI652-2	EP20K200EBI356-2X
	EP20K200EQI240-2X	EP20K200EBI672-2X

Device Family	Devices	
	EP20K300EQI240-2X	EP20K400CF672I8
	EP20K400CB652I8	EP20K600CF33C7
	EP20K600CB652I8	EP20K600CF33C9
	EP20K600CF33C8	EP20K600CF672I8
	EP20K1000CF33I8	
APEX™ II	EP2A15F672I8	EP2A25B724I8
	EP2A25F672I8	EP2A40B724I8
	EP2A40F1020I8	EP2A70F724C7
	EP2A70F724C8	EP2A70F724C9
	EP2A70F1508C7	EP2A70F1508C8
	EP2A70F1508C9	
FLEX 10K®	EPF10K10AFC256-1	EPF10K10AFC256-2
	EPF10K10AFC256-3	EPF10K10AQI208-3
	EPF10K30ABI356-3	EPF10K50SFI484-2
	EPF10K50SQC240-2X	EPF10K50STC144-1
	EPF10K50STC144-1X	EPF10K50STC144-2
	EPF10K50STC144-3	EPF10K50VQI240-2
	EPF10K100ABI600-2	EPF10K100EFC484-2X
	EPF10K100EQC240-2X	EPF10K130EBC356-2X
	EPF10K120EBC600-1	EPF10K120EBC600-1X
	EPF10K120EBC600-2	EPF10K120EBC600-2X
	EPF10K120EBC600-3	EPF10K130EFC484-2X
	EPF10K130EFC672-1	EPF10K130EFC672-1X
	EPF10K130EFC672-2	EPF10K130EFC672-2X
	EPF10K130EFC672-3	EPF10K130EQC240-2X
	EPF10K200SBC356-1	EPF10K200SBC356-1X
	EPF10K200SBC356-2	EPF10K200SBC356-2X
	EPF10K200SBC356-3	EPF10K200SBC600-2X
	EPF10K200SFC484-2X	EPF10K200SFC672-2X
	EPF10K200SRC240-2X	
	FLEX® 6000	EPF6016AQI208-2
EPF6016ATI144-2		EPF6024ABI256-2
EPF6024AFI256-2		EPF6024AQI208-3
MAX® 7000	EPM7032BLC44-3	EPM7032BLC44-5
	EPM7032BLC44-7	EPM7032BUC49-3
	EPM7032BUC49-5	EPM7032BUC49-7
	EPM7064SLI84-7	EPM7128EFC256-7
	EPM7128EFC256-10	EPM7128ELC84-5
	EPM7128ELC84-7	EPM7128ELC84-10
	EPM7128BFC100-4	EPM7128BFC100-7
EPM7128BFC100-10	EPM7128BFC256-4	

Device Family	Devices	
	EPM7128BFC256-7	EPM7128BFC256-10
	EPM7128BFI256-7	EPM7256BQC208-5
	EPM7256BQC208-7	EPM7256BQC208-10
	EPM7256BQI208-7	EPM7256BUC169-5
	EPM7256BUC169-10	EPM7512AEBI256-10
	EPM7512BBC256-5	EPM7512BBC256-7
	EPM7512BBC256-10	EPM7512BFI256-10
Excalibur™	EPXA1F484I2	EPXA1F672I2

Timing Models

This section contains a summary of timing model status in the current version of the Quartus II software.

Preliminary Timing Models

The following table shows the devices with preliminary timing models in the current version of the Quartus II software:

Devices with Preliminary Timing Models

Device Family	Device
Stratix II	EP2S15*
	EP2S30*
	EP2S60*
	EP2S90*
	EP2S130*
	EP2S180*
Cyclone II	EP2C5*
	EP2C8*
	EP2C20*
	EP2C35*
	EP2C50*
	EP2C70*
MAX II	EPM240
	EPM570
	EPM1270
	EPM2210

* These devices had significant changes to their timing models in this release of the Quartus II software. You should run the Timing Analyzer on your design to see any effects of these changes.

Final Timing Models

The following table lists the devices with final timing models that are available in the current version of the Quartus II software:

Devices with Final Timing Models

Device Family	Device	Timing Models Final in Quartus II Version Number
APEX II	EP2A15	2.1
	EP2A25	2.1
	EP2A40	2.1
	EP2A70	2.1
Cyclone	EP1C3	3.0 SP1
	EP1C4	4.0
	EP1C6	3.0
	EP1C12	3.0 SP1
	EP1C20	3.0
FLEX 10K	All	3.0
FLEX 10KA	All	3.0
Mercury ⁽¹⁾	EP1M120	2.1 SP1
MAX 3000 ⁽¹⁾	EPM3512A	2.1 SP1
MAX 7000 ⁽¹⁾	EPM7512B	2.1 SP1
MAX 7000S	All	3.0
Stratix ⁽²⁾	EP1S10	4.1
	EP1S20	4.1
	EP1S25	4.1
	EP1S30	4.1
	EP1S40	4.1
	EP1S60	4.1
	EP1S80	4.1
Stratix GX ⁽²⁾	EP1SGX10	4.1
	EP1SGX25	4.1
	EP1SGX40	4.1

(1) Timing models for devices in this device family not listed here became final in versions 2.1 and earlier.

(2) The timing models for devices in this family were updated in version 4.1 of the Quartus II software.

The current version of the Quartus II software also includes final timing models for the ACEX[®] 1K, APEX 20K, APEX 20KE, APEX 20KC, Excalibur, FLEX 6000, and FLEX 10KE device families. Timing models for these device families became final in versions earlier than version 2.1.

EDA Interface Information

The Quartus II software version 4.2 supports the following EDA tools.

Supported EDA Tools

Synthesis Tools	Version	NativeLink® support
Mentor Graphics® LeonardoSpectrum	2004b	✓
Synopsys Design Compiler	2004.09	
Synopsys Design Compiler FPGA	2004.12	
Synopsys FPGA Compiler II	3.8	✓
Mentor Graphics Precision RTL Synthesis	2004c	✓
Synplicity Synplify and Synplify Pro	8.0	✓
Magma Design Automation PALACE™	2.4	✓
Verification Tools	Version	NativeLink support
Cadence NC-Verilog (Windows)	5.1-s017	✓
Cadence NC-Verilog (UNIX)	5.1-s017	
Cadence NC-VHDL (Windows)	5.1-s017	✓
Cadence NC-VHDL (UNIX)	5.1-s017	
Cadence Verilog-XL (Windows)	3.3	
Cadence Verilog-XL (UNIX)	5.1-s017	
Mentor Graphics ModelSim®	5.8e	✓
Mentor Graphics ModelSim-Altera	5.8e	✓
Synopsys PrimeTime	2004.06	✓
Synopsys VSS	2002.06	
Synopsys VCS / VCS - MX	7.1.1 L1	
Synopsys Formality	2004.12	
Mentor Graphics Tau	SDD 2004	
Cadence Incisive Conformal	4.3.5.a	

Changes to Software Behavior

This section documents instances in which the behavior and default settings of this release of the Quartus II software have been changed from earlier releases of the software.

Changes to Default Settings in This Release

This section lists the variable names for Quartus II settings that have different default values in the Quartus II software version 4.2 from the previous version. The default values and a list of the changed values are stored in the */<Quartus II Installation directory>/bin/assignments_default.qdf* file.

Setting Keyword	Default in 4.1	Default in 4.2
<code>do_min_analysis</code>	ON	OFF

Changes to Software Behavior

Items listed in the following table represent cases in which the behavior of the current release of the Quartus II software is different from a previous version.

Description	Workaround
For MAX 7000S family devices, the Quartus II software version 4.2 reports unused I/O pins as RESERVED by default, or as RESERVED_INPUT if the setting Reserve all unused pins as inputs, tri-stated is selected. Previous versions report unused I/O pins as GND* , which is incorrect for MAX 7000S family devices.	To generate a correct pin-out file, recompile any MAX 7000S designs that were created in earlier versions of the Quartus II software.
The Quartus II software version 4.2 and later prohibits the placement of the IOE registers within the same LAB row as a SERDES RX or TX channel. IOE registers must be placed at least one LAB row away from an RX or TX channel. The Quartus II software version 4.1 SP2 and earlier does not prohibit the use of IOE registers in the same LAB row as a receiver (RX) or transmitter (TX) channel that utilizes the SERDES block.	Recompile any Stratix II design that was created in an earlier version of the Quartus II software with the current version. The setup time of the register (t_{SU}) will increase if the IOE register is moved to the PLD core. It is up to the designer to ensure that all setup times are met. Contact Altera Applications for more details.

Description	Workaround
The Tcl Console Window is disabled while a compilation or simulation flow is in progress. This behavior is necessary to prevent inadvertent changes to settings files during compilation.	Wait until compilation or simulation is complete before trying to execute a Tcl command in the Tcl Console.
The pll megafunction has been removed from the Quartus II software version 4.2. This megafunction implemented a digital PLL in logic cells, and was maintained for backward compatibility only.	If wish to still use the pll megafunction rather than the altpll or altclklock megafunctions, you must copy the pll.inc and pll.tdf files from the /<Path to Quartus II installation>/mega directory of a previous version and place them in the same directory of the current version.
The PLLs in Stratix, Stratix II, and Stratix GX device families no longer support delay shift (time delay elements).	Altera recommends using the phase shift feature of the altpll megafunction to implement time shifts.
The Quartus II software version 4.2 no longer supports the -entity option for the LL_IMPORT_FILE assignment.	You must make the LL_IMPORT_FILE assignment for each instance of the entity to which you want to make the assignment.
<p>In the Quartus II software version 4.2, the RAM atom simulation models have changed in the following ways:</p> <ol style="list-style-type: none"> 1. In the Quartus II software version 4.1 and earlier, all ports on the RAM atom had fixed widths (data port width=144,address port width=16, etc.). Starting in version 4.2, the widths of all ports are parameterized. 2. The default port width in the simulation model is 1 (i.e., if an input is not used, it is assumed that the width of that input is 1). 3. Instead of using parameters such as MEM1,...,MEM9 to hold initialization data for RAM, two parameters called "MEM_INIT0 and MEM_INIT1" are used. The MEM_INIT0 parameter holds lower bytes of initialization data in increasing order of address up to a maximum of 2048 bits. The MEM_INIT1 parameter holds the remaining upper bytes. 	You must recompile your project in the Quartus II software version 4.2 or later to generate new Verilog Output (.vo) or VHDL Output (.vho) files for the simulation tool. If your design runs at a clock speed of greater than 500 MHz, you must set the simulation resolution to picoseconds (ps).
The Quartus II software no longer uses the registry to store non-user interface-related settings. Non-user interface-related settings are stored automatically in the quartus2.ini file when you open the Quartus II software user interface for the first time.	You must open the Quartus II software user interface at least once before using the command-line version of the software.

Description	Workaround
<p>The following Tcl simulator commands are no longer supported by the Quartus II software version 4.0 and later:</p> <ul style="list-style-type: none"> • dbg • get_time • get_value • force_value • release_value • read_memory • write_memory • run • print • get_memory_width • get_memory_depth • testbench_mode 	<p>There are new versions of most of these commands in the ::quartus::simulator package, which is available in the quartus_sim.exe module. Refer to the Quartus II Command-Line and Tcl API Help for more details. To view Tcl online Help type the following command at a command prompt:</p> <pre>quartus_sh --qhelp <Enter></pre>
<p>When you instantiate a new RAM or ROM function with the MegaWizard Plug-In Manager, the outputs of the memory function will be registered using the same clock as the inputs, by default. This is a change of behavior in that the Quartus II software versions earlier than version 4.0, the outputs were not registered by default.</p>	<p>This is a change of behavior that affects only new instantiations of RAM or ROM function. Existing memory functions are not affected.</p>
<p>In the Quartus II software version 3.0 and earlier, LogicLock™ assignments are stored in lowercase. In version 4.0 and later, designs written in case-sensitive languages may require that LogicLock assignments be in mixed case. Due to the difference in case-sensitivity between versions, LogicLock assignments made in the Quartus II software version 3.0 and earlier may not be usable in the Quartus II software version 4.0 and later.</p>	<p>Do not use upper case or mixed case in your HDL design files.</p>
<p>When you are using formal verification tools with a design that contains LogicLock regions that was compiled with the Quartus II software version 3.0 or earlier, under certain circumstances when you open the design in the Quartus II software version 4.0 and later, the LogicLock regions will not be handled properly.</p>	<p>Redefine the LogicLock regions in the Quartus II software version 4.0 or later to eliminate the errors.</p>

Description	Workaround
<p>Changes made to settings and/or assignments in the Assignment Editor, Floorplan Editor, or with Tcl commands in the Tcl Console window are saved to disk only when you choose Save Project (File menu). Choosing Save in the Assignment Editor, Floorplan Editor, or Settings dialog box saves the changes to memory only. They are not committed to disk until you choose Save Project (File menu), close the project, or exit from the Quartus II software. If you have turned off Save changes to all files before starting a compilation, simulation, or software build on the Processing page of the Options dialog box (Tools menu), changes you made may not be reflected in the latest compilation.</p>	<p>Turn on Save changes to all files before starting a compilation, simulation, or software build on the Processing page of the Options dialog box (Tools menu).</p> <p><i>or</i></p> <p>Choose Save Project (File menu) after making any changes to settings or assignments.</p>
<p>In the Quartus II software version 4.0 SP1 and later, the labeling of unused GXB_TX and GXB_RX pins has changed.</p>	<p>Pins previously labeled GXB_VCC+ are now labeled GXB_VCC*. Pins previously labeled GXB_GND+ are now labeled GXB_GND*.</p>
<p>The behavior of the Quartus II Fitter has been modified to minimize compilation time when there are no timing constraints applied to the design. This change in behavior results in an average of 40% faster compilation times and an average of 15% slower f_{MAX} performance. This change to the Fitter behavior applies only when the Auto Fit option is chosen for Fitter Effort on the Fitter Settings page of the Settings dialog box (Assignments menu), and affects only Stratix, Stratix GX, Stratix II, Cyclone, and Cyclone II device families.</p>	<p>To return to the same behavior as earlier versions of the Quartus II software, choose Standard Fit under Fitter Effort on the Fitter Settings page of the Settings dialog box (Assignments menu), or apply appropriate timing constraints.</p>

Description	Workaround
<p>The following megafunctions have clear box simulation models that contain assignments that are not stored in the Quartus Settings File (.qsf) and are not written out to a Verilog Quartus Mapping File (.vqm):</p> <pre> altdqs altdq altddio_bidir altddio_out altddio_input altlvds_rx altlvds_tx altufm_i2c dcfifo </pre>	<p>Do not save your atom netlist file as a VQM if you are using these megafunctions.</p>
<p>The following megafunctions now use clear box models instead of the generic model libraries:</p> <pre> altmemmult altufm altdq altdqs altremoteupdate altpll_reconfig altclkctrl </pre>	<p>When you are simulating a design that uses one of these megafunctions, you must use the family-specific atom model library (such as stratix_atoms.v) instead of the generic altera_mf.v (or .vhd) library.</p>

Known Issues & Workarounds

General Quartus II Software Issues

Issue	Workaround
The Assignment Editor may respond very slowly when the design files are located on a remote machine, and you have not performed Analysis & Elaboration on the design files.	Run Analysis & Elaboration on the design before using the Assignment Editor.
Changing the number of registers in the routing for a SignalProbe™ pin, and then recompiling the design sometimes results in a message similar to the following example: Warning: Following 1 pins have nothing, GND, or VCC driving datain port	Perform the following steps: 1. Turn off the SignalProbe assignment you want to change. 2. Recompile the design. 3. Turn on the SignalProbe assignment and change the number of registers. 4. Start a SignalProbe compilation.
During a SignalProbe compilation, you might receive warning message(s) similar to the example shown below: Routing constraints for signal <some_signal> seem to be causing unresolvable routing congestion. The constraints for the signal were removed.	The Compiler issues these warning when it is unable to retain the routing constraints from a previous compilation because those routing resources were needed by the SignalProbe signal routing.
If you modify a resource (node or connection) used by a SignalProbe pin using the Resource Property Editor and then perform another SignalProbe compilation, the compilation will fail and the Quartus II software may crash with an Internal Error.	Do not use the Chip Editor features (Resource Property Editor, Chip Editor, or Engineering Change Manager) to modify properties of SignalProbe pins.
Not all speed grades of a given device share the same features.	Refer to the Altera device handbook or data sheet for further information.

Issue	Workaround
There is no distinction between output ports and bidirectional ports in AHDL Function Prototypes; instead, all ports listed after the RETURNS keyword are treated as output ports. As a result, if you specify a bidirectional port in a logic function's Function Prototype Statement and do not connect the port to a top-level bidirectional pin or to other logic in the design where you instantiate the logic function, an error can occur.	Connect the port to a top-level bidirectional pin or to other logic in the design.
Context-sensitive Help is not available for some items in the Quartus II software.	To locate Help on those items, choose Index (Help menu) and type the name of the item.
The Timing Analyzer does not recognize non-PLL clock signals when using any PLL megafunction.	Make clock settings assignments to all non-PLL clocks.
The Waveform Editor does not allow you to create a bus with nodes that are nonconsecutive members of a bus.	Create buses only with nodes that are consecutive members of a bus. Or, use the Group command (Edit menu) to create groups of arbitrary nodes.
If you are using the <code>altcam</code> , <code>altclklock</code> , <code>altlvds_rx</code> , or <code>altlvds_tx</code> megafunctions, the equations shown in the Equations Section of the Compilation Report are not complete.	To view the complete equations for any of these megafunctions, use the Equations window of the Timing Closure floorplan.
The Quartus II software does not support design file names with more than one extension. For example, you cannot use the file name file.eda.edif .	Use design file names with only one extension.
If you install the Quartus II software for PCs on a UNIX server that exports shares with the Samba software version 1.9.18p10, you may experience problems accessing project files that are also on the network.	Altera recommends using version 1.9.16p11 or 2.0 of the Samba software.
If you make assignments to reserve pins as a group or with group notation (<code>debug [7..0]</code>), the Quartus II software does not correctly generate simulation output files, and you receive a warning message saying "Unsupported data type in the top-level module."	Reserve the pins using single-name notation (for example, <code>debug [7]</code> , <code>debug [6]</code> , and so on).

Issue	Workaround
Do not change the file permissions (such as changing “read-only” to “read and write”) of Quartus II settings and configurations files (.qpf, and .qsf,) while a Quartus II project is open.	Close the Quartus II project before making changes to the file permissions.
Node names containing numbers greater than 2 ³¹ -1 (2147483647) will cause an Internal Error in the Quartus II software.	Do not use node names containing large numbers.
Occasionally the Programmer does not allow you to use a MAX 7000AE Programmer Output File (.pof) with a MAX 7000AE device. This error sometimes occurs after a compatible MAX 7000B device is used with the MAX 7000AE POF.	Do not switch between compatible MAX 7000B and MAX 7000AE devices when a MAX 7000AE POF is loaded, or reload the MAX 7000AE POF.
Routing back-annotation may fail if the back-annotated locations do not match the location assignments in the QSF or if the location assignments are missing. This problem can occur if you change devices, or if you remove some location assignments by using the Assignment Editor (Assignments menu) or by manually editing the QSF.	If you experience a “no fit” or an Internal Error while using routing back-annotation, delete the Routing Constraints File (.rcf) and back-annotate the design again after a successful compilation.
If you receive an error message saying “System resources low...” or if the user interface is slow in responding and there is a lot of disk activity when you are not compiling a design, your system may be running out of free memory.	You can recover system memory by clearing messages from the Messages window. To clear messages from the Messages window, right-click anywhere in the Messages window and choose Clear Messages from Window (right button pop-up menu). Additional memory can be recovered by closing the Floorplan Editor.
Occasionally, the Quartus II software may crash or hang with no error message immediately upon opening a project.	Delete the Quartus Workspace File (.qws) <project name>.qws from the project directory. If the problem persists, delete the \<project directory>\db directory.
When you are setting phase shift and duty cycle values for clock signals using the altp11 megafunction, some combinations of settings may result in values that cannot be synthesized exactly. Under certain circumstances, the Quartus II software attempts to synthesize the phase shift parameter before the duty cycle parameter.	You should first select values for the parameter (phase shift or duty cycle) that is most important for your design.

Issue	Workaround
<p>During compilation or simulation, the Quartus II software may “hang” and not proceed to the next module if a menu or modal dialog box is open at the time the current module finishes running.</p>	<p>Close any open menus or modal dialog boxes before the compilation or simulation reaches the next stage.</p>
<p>Running individual Quartus II software executables (quartus_map, quartus_fit, and so on) from within the Quartus II Tcl Console may cause the Quartus II software to crash.</p>	<p>You should run individual executables either from within the Quartus II scripting shell (quartus_sh) or directly at a command prompt.</p>
<p>If you have chosen migration devices in the Compatible Migration Devices dialog box, which is available from the Device page in the Settings dialog box (Assignments menu), the Timing Closure Floorplan will display only the pins and PLLs that are common to all the selected devices. However, the Chip Editor will display all the pins and PLLs available for the device specified for compilation.</p>	
<p>Turning Physical Synthesis on in the Physical Synthesis Optimizations page under Fitter Settings in the Settings dialog box on average will cause compilation time to double and peak memory usage to increase by approximately 20%. For large designs, the Progress Bar for the Fitter may appear to be stuck in the 50-70% range while the elapsed time continues to increase. Provided that compilation time has not increased over 10X, this is normal and the compilation should be allowed to finish. In rare cases, the compilation time may increase by more than 10X. In these cases, it is appropriate to apply the workaround if you cannot tolerate such a long compilation time.</p>	<p>If compilation time is excessive with Physical Synthesis turned on, you can either remove or convert LogicLock regions to soft before recompiling, or you can turn off Physical Synthesis.</p>
<p>The time shown in the Status window may not agree with the processing times reported in the Compilation Report. This difference is due to differences in how the times are calculated during processing.</p>	

Issue	Workaround
If you type a name in the entity column of the Assignment Editor that differs from an existing name only by case, the Assignment Editor's "auto-completion" feature always uses the existing name.	Type the new entity name in another application, such as a text editor, copy it to the clipboard, and paste the name from the clipboard into the Assignment Editor.
Altera recommends that you do not use node or entity names that differ only by case if you are using the Quartus II Simulator or Waveform Editor.	
Under certain circumstances, a design that uses Virtual Pin assignments may fail to fit after back-annotation. This situation occurs because the clock signals chosen automatically for the first compilation do not match those chosen for the second compilation.	Manually assign your clock signals, using Virtual Pin Clock assignments before the first compilation, or use Advanced Back-Annotation to explicitly write out the virtual clock assignments before the second compilation.
If you use the <code>dcfifo</code> or <code>scfifo</code> megafunctions in an AHDL design, you may receive an error message similar to "The parameter LPM_WIDTHU has been set to an invalid value..."	Either remove the LPM_WIDTHU parameter arguments from your AHDL <code>dcfifo</code> or <code>scfifo</code> megafunction instantiation, or explicitly set the LPM_WIDTHU parameter to <code>ceil(log2(LPM_NUMWORDS))</code> .
If you use the MegaWizard Plug-In Manager to create files for your design, the Quartus II software might not "remember" your settings for device, etc.	The Quartus II software does not write your settings to the Quartus Settings File (.qsf) until you close the MegaWizard Plug-In Manager . You must save your settings with the Save Project command (File menu).
Do not open, change permissions, or delete the <code><project directory>/db</code> directory or any file therein while any Quartus II executable is running.	
If you are using the IP Toolbench and add a user library, the Quartus II software may add a backslash (\) to the end of the library file name. The Quartus II user interface ignores this trailing backslash.	
Support for nondecimal radix numbers (such as hexadecimal) used as constants in the <code>lpm_constant</code> , <code>lpm_compare</code> , and <code>lpm_add_sub</code> megafunctions is limited to values that can be represented by 31 bits or fewer.	For values that require more than 31 bits, use decimal radix only.

Issue	Workaround
In situations where the Quartus II software merges multiple ROMs into a single RAM block when using LogicLock regions in an APEX II design, a new Memory Initialization File (.mif) will be created and should be used for subsequent compilations. If you need to change the ROM data, you must change it in the new MIF.	

Issue	Workaround
<p>Under certain circumstances, back-annotation of routing in unreserved LogicLock regions can cause unsatisfiable routing constraints for signals going to clock and clock-enable ports of LABs. This can occur when other portions of the design are not back-annotated, and the Fitter populates empty LCELLs in the back-annotated LogicLock region during subsequent compilations.</p> <p>For example, assume that on the initial compilation, LogicLock region L contains register A, which uses the CLK1 and ENA1 ports of a LAB. When the design is recompiled, the Fitter may place register B, which is not part of region L, and uses the SLOAD input, in the same LAB as register A (assuming that the LAB has sufficient empty space to accommodate it).</p> <p>The LAB control signal generation block does not allow use of both ENA1 and SLOAD in the same LAB; therefore, register A must use the CLK0 and ENA0 ports, rather than CLK1 and ENA1. To avoid a no-route situation, the Fitter will ignore the routing constraints for the clock and enable signals, and re-route the signals using the appropriate control signal multiplexing for the CLK0 and ENA0 ports of the LAB. The Fitter picks the most appropriate routing and, in the majority of cases, the circuit's timing is not adversely affected. When the Fitter is forced to ignore routing constraints, info messages of the form "Info: Can't route signal <name> to atom <name>" are displayed to inform the user; the appearance of such messages is not a cause for alarm.</p>	<p>This situation can be avoided entirely by marking all LogicLock regions as Reserved, thereby preventing the Fitter from placing new items in a region. The tradeoff, of course, is that should a Reserved LogicLock region be under-utilized, the Fitter will be unable to place other logic items in the unused portion of the region.</p>

Platform-Specific Issues

PC Only

Issue	Workaround
You cannot access the web-based PowerPlay Early Power Estimator on the Altera web site if you have installed Windows XP SP2 because the service pack blocks the active content.	Refer to the Altera Knowledge Database on the Altera web site for more information on enabling your browser to access the PowerPlay Early Power Estimator spreadsheets.
Some dialog box title bar text is not displayed correctly when the Quartus II software is installed on a computer running the Chinese version of Windows XP.	Change the font in the Active Title Bar section of the Windows Appearance Control Panel.
If you do not have Administrator privileges when you install the Quartus II software, certain features of the software, particularly the online help, will not work properly.	Altera recommends that you have Administrator privileges when installing the Quartus II software.
Under certain circumstances, the Quartus II installation program may crash or you may receive an error message immediately upon launching the installation program.	<p>Reinstall the stdole32.tlb file from the original Windows distribution disks. To reinstall the file, type the appropriate command at a command prompt. (Note: the command must be typed on one line.)</p> <p>Windows NT: <CD-ROM drive letter>:\i386\expand.exe stdole32.tl_ %SystemRoot%\System32\stdole32.tlb <Enter></p> <p>Windows 2000: <CD-ROM drive letter>:\i386\expand.exe stdole32.tl_ %SystemRoot%\System32\stdole32.tlb <Enter></p> <p>Windows XP: <CD-ROM drive letter>:\i386\expand.exe stdole32.tl_ %SystemRoot%\System32\stdole32.tlb <Enter></p>

Issue	Workaround
If the full, hierarchical name of an instance exceeds 247 characters, it may not be displayed properly in the Quartus II user interface. This problem occurs most often with EDIF netlist files generated by other EDA synthesis tools.	Limit the full, hierarchical instance name to fewer than 247 characters if possible.
Due to a limit of the Windows operating system, path names longer than 229 characters can cause an internal error in the Quartus II software.	Make sure that all path names do not exceed 229 characters. This limitation applies to UNIX and Linux installations also.
If you are running the Quartus II software from a network server, the Quartus II software will not run properly on the client computer if you share the <code>\quartus\bin</code> directory.	You must share the <code>\quartus</code> directory, not the <code>\quartus\bin</code> directory.
The Quartus II software is not compatible with the MATLAB web server.	Turn off the MATLAB web server in the Services Control Panel (Start menu) before running the Quartus II software.
Under some circumstances, the Quartus II splash screen appears and the Quartus II icon appears in the Taskbar, but the graphical user interface does not appear. Under other circumstances, the user interface appears but windows and/or toolbars do not appear correctly.	The registry settings controlling the position of the Quartus II windows may have become corrupted. If the user interface appears, click the Reset All button on the Toolbars page of the Customize dialog box (Tools menu), or, if the user interface does not appear, type the following command at a command prompt: <code>quartus -reset_desktop <Enter></code>
If you install the stand-alone Quartus II Programmer and the Quartus II software, and then uninstall either one, the Programmer may report "JTAG Server -- internal error code 82 occurred" when you click the Add Hardware button in the Hardware Setup dialog box (Edit menu). This error occurs because uninstalling the software has disabled the JTAG Server service.	Manually restart the JTAG Server service by locating the <code>jtagserver.exe</code> program and at a command prompt for that directory, type <code>jtagserver --install <Enter></code>
If you choose to uninstall a previous version of the Quartus II software during installation, and there is a "locked" file or directory, the installation program will not reboot the computer as is necessary to successfully complete the installation.	Exit from the installer and reboot the computer manually after the removal of the previous version is complete, before completing the installation of the new version.

Issue	Workaround
The Quartus II software version 4.2 does not allow a parallel port T-Guard (dongle) to be used on the same parallel port as a ByteBlaster II download cable.	Use another download cable, such as a USB-Blaster or MasterBlaster to configure your device, or use separate parallel ports for the T-Guard and the download cable. The Quartus II programmer is not a licensed feature, so you can remove the T-Guard to program your device, but you must replace it to use any other Quartus II software features.
If you are running the Quartus II software on Windows with a country setting that uses the comma (,) as the decimal point, instead of the period (.), you may encounter unexpected results when performing arithmetic functions in the Tcl Console window.	
During installation of the Quartus II software, when you insert the ModelSim-Altera CD-ROM, an Explorer window may appear.	Close the Explorer window before proceeding with the installation.

Solaris, HP-UX & Linux

Issue	Workaround
On certain Solaris 8 and Linux systems, the text in the Assignment Editor, and other dialog boxes, may not be readable because of the text size.	Delete or move the ~/.mw directory and restart the Quartus II software.
If the operating system crashes, and the file system in \$TMP is rebuilt automatically, the data in the \$TMP/Mw_<user ID> file is corrupted, the Quartus II software may fail to start correctly.	Delete the \$TMP/Mw_<user ID> file and restart the Quartus II software.
If you are using the Exceed X server software for Windows while running the Quartus II software, the font size may be larger than the line height. This problem occurs most often if you installed the Exceed software while running at a screen resolution greater than 1024 × 768.	Reinstall the Exceed software while running at a screen resolution of 1024 × 768. You can then switch back to your normal, higher resolution setting.
Under some circumstances, there may be editor windows listed in the Window menu that you cannot see.	To display the hidden windows, choose Cascade (Window menu).
You cannot launch the AXD Debugger software from within the Quartus II software.	Launch the AXD Debugger software from outside the Quartus II software.

Issue	Workaround
Under some circumstances, the Internet connectivity features of the Quartus II software are not functional.	Specify the full path to your web browser software on the Internet Connectivity page of the Options dialog box (Tools menu). If you access the Internet through a proxy server, you must also specify the address of the proxy server and its port number.
If you cannot access the Quartus II online Help in the user interface, you can access it by typing <code>hh quartus.chm <Return></code> at a command prompt.	
If you are accessing the Quartus II software through one of the following versions of the Hummingbird Exceed software (6.2, 7.0, 7.1, or 8.0) and have any Microsoft Office application or Internet Explorer open, the Quartus II user interface may start very slowly.	Contact Hummingbird Software at www.hummingbird.com for a patch for the Exceed software.
If you are running the Quartus II software version 4.0 and later on a Linux or Solaris workstation, even though Reopen current project and files at startup is turned on, the last project is not reopened when you restart the software.	Use the Recent Projects command (File menu) to reopen your last project.
The stand-alone Quartus II Programmer and SignalTap programs are not available on Solaris, Linux, and HP-UX workstations.	
If you double-click or click and hold on drop-down list boxes in the Resource Property Editor, the Quartus II software may crash.	
When you are changing values in the Resource Property Editor, you must press the Return key to apply the changed values.	

Solaris Only

Issue	Workaround
Creating an instance of the SignalTap II embedded analyzer with the MegaWizard Plug-In Manager causes the MegaWizard Plug-In Manager to crash with an error similar to the example shown below: “Can't create the custom megafunction variation files.”	Create the SignalTap II Logic Analyzer instance using the Quartus II GUI with the SignalTap II Logic Analyzer command (Tools menu).
The ARM-based Excalibur MegaWizard Plug-In , which is available from the MegaWizard Plug-In Manager , requires the Java Runtime Environment (JRE), which has already been installed on your computer. On Solaris workstations, however, you may need to install extra patches to the operating system in order for the JRE to function properly.	Check the web site http://sunsolve.sun.com/pub-cgi/show.pl?target=patches/J2SE for information about any patches that might be needed.
On certain Solaris 8 systems, the position and size of the Help window are not maintained when the Quartus II software is closed and then started again.	Install Solaris OS patch 109147-12 or higher to regain the normal Help functionality.

HP-UX Only

Issue	Workaround
You receive error messages indicating that you do not have required permissions to perform the requested operation while using Network Information Services (NIS).	Add a plus-sign (+) followed by a carriage return on a line by itself as the last line in both of the following files: /etc/passwd and /etc/group .
Programming EPC16 configuration devices is disabled on HP-UX workstations.	

Linux Only

Issue	Workaround
If the MasterBlaster™ download cable is not listed in the Available hardware items list in the Hardware Settings tab of the Hardware Setup dialog box, but it is connected properly, you may not have read/write permission for the serial (<code>dev/ttySx</code>) port to which the MasterBlaster cable is connected.	Have a system administrator assign read/write permission for the appropriate port. This change can be accomplished by adding you to the “uucp” group, or by giving read/write permission for the serial port to everyone, using the following command: <code>chmod o+rw /dev/ttySx</code> where <i>x</i> is the serial port affected.

Issue	Workaround
If you are using the ReflectionX X-server software as your display on a Linux workstation, the Quartus II software may hang and a white box may appear.	Set the <code>QUARTUS_MWWM</code> environment variable to <code>allwm</code> and then start the Quartus II software without the splash screen by typing the following commands at a command prompt: <pre>setenv QUARTUS_MWWM allwm <Return> quartus -no_splash <Return></pre>
If you double-click or click and hold on drop-down list boxes in the Resource Property Editor, the Quartus II software may crash.	
Under certain circumstances, the Quartus II software may not start properly.	On a system with a static IP address, ensure that the <code>/etc/hosts</code> file has an entry for the hostname of the machine on which you are running. For example, if the workstation is named “orange,” there should be an entry in <code>/etc/hosts</code> with the IP address of the “orange” workstation as shown below: <pre><IP address of orange> orange</pre> In addition, the network configuration (hostname, DHCP hostname, DNS search path, and domain names) must be correct or the Quartus II software will abort on startup.
If you are running the Quartus II software version 4.0 and later using VNC software, the Quartus II software may terminate unexpectedly whenever you open any file or browse any directory from within the Quartus II software.	Make sure your VNC server software is version 3.3.4 or later.
If you are running the Quartus II software under Red Hat Linux 7.3, you may experience substantial degradation of compilation times if your design files are located on a separate server from the Quartus II software.	Make sure that the operating system kernel is upgraded to the latest available. If you are using a NetApps server, refer to the following document for more information: www.netapp.com/tech_library/ftp/3183.pdf
If you select a node in the Timing Closure Floorplan, and select Locate in the Resource Property Editor (right button pop-up menu), and then select Goto Source Node (right button pop-up menu), the Quartus II software will not display the entire, hierarchical node name.	

Device Family Issues

Excalibur

Issue	Workaround
<p>You may receive the message “System Build Descriptor File missing parameter programming clock frequency” for System Build Descriptor Files (.sbd) generated in the Quartus II software version 2.0 and earlier, after selecting the Boot from Serial option in the ARM-based Excalibur MegaWizard Plug-In.</p>	<p>Rerun the ARM-based Excalibur MegaWizard Plug-In in the current version of the Quartus II software to regenerate the SBD File and correct the error.</p>
<p>If you are using the Stripe-to-PLD Bridge in Excalibur EPXA10 Devices, your design may not function due to the Stripe-to-PLD Bridge lockup errata if either of the following options is turned on in the Quartus II software:</p> <ul style="list-style-type: none"> Remove Redundant Logic Cells Perform WYSIWYG Primitive Resynthesis <p>Please refer to the EPXA10 Device Errata Sheet for details on the device errata.</p>	<p>To avoid bridge lockup, ensure that the Remove Redundant Logic Cells option is turned off for the project.</p> <p>If the Perform WYSIWYG Primitive Resynthesis option is turned on for your project, you may receive warnings that the stripe signals were not routed correctly. To eliminate the warnings, re-run the MegaWizard Plug-In Manager in the Quartus II software version 2.2 or later. This procedure will create an additional settings file (alt_exc_stripe.esf) to ensure that the required logic elements are implemented.</p>

Issue	Workaround
<p>Designs targeting Excalibur devices that use Boot-from-Flash mode may not operate when downloaded to the target board if the Quartus II Software Builder or SOPC Builder Excalibur-build script was used to generate the flash programming file.</p>	<p>The Excalibur boot loader in the Quartus II software version 3.0 does not function correctly if the Quartus II Software Builder is used to generate the flash programming file. This is because the compression option that is used with the makeprogfile utility during the software build process does not work with this version of the bootloader. To work around this issue, do not use the Software Builder to generate a programming file, but instead use the makeprogfile utility at the command line with the -nc (no compression) option. If you are using the SOPC Builder Excalibur-build script, you must edit the script located in the <i><XA dev kit instalationl directory>\bin</i> folder. Modify line 1034 of this script to remove the -nc option. For example, line 1034 should be changed as shown in this example.</p> <pre>\$command = "makeprogfile -nc -b \${fileBase}_bootdata.o \$SBD \$SBI \${fileBase}.hex";</pre> <p>You must recompile your software project for this change to take effect.</p>
<p>If you are developing new designs with the XA MegaWizard, you should manually import the file settings from the <i><block_name>.esf</i> file into the Quartus Settings File (.qsf) using the Import Assignments command (Assignments menu). This ensures that the Quartus II software does not remove certain cells and uses the inverting input on the stripe interface, which does not work.</p>	

Cyclone, Stratix & Stratix GX

Issue	Workaround
<p>When you use a Routing Constraints File (.rcf) to control fitting after performing Routing Back-Annotation, your timing analysis results may change slightly due to parasitic and other effects. Any change will be very small.</p>	
<p>If you use the SignalProbe™ feature to observe the signals at an output pin, by routing them to another output pin, the SignalProbe output pin signal will be shown as Unknown (X) in the Quartus II Simulator.</p>	<p>The signal will be correct in actual operation, the error appears only in the Quartus II Simulator.</p>
<p>In the SignalProbe Source to Output Delays table of the Timing Analyzer Report, the following right-button menu commands are not available although they are available in other similar Timing Analyzer Report tables:</p> <ul style="list-style-type: none"> • List Paths • Locate in Chip Editor • Locate in Timing Closure Floorplan 	<p>You can use other Timing Analyzer Report tables to list and locate the affected paths.</p>

Stratix and Stratix GX

Issue	Workaround
<p>If you use the altddio_bidir or alt_dqs megafunction and connect any data port directly to VCC or GND, the Quartus II software version 3.0 SP1 and later will insert an additional logic element in the circuit path.</p>	
<p>The behavior of the 0-degree phase shift setting of the DLL_PHASE_SHIFT parameter of the altdqs megafunction or the DQS Phase Shift logic option with the altddio_bidir megafunction has changed in the Quartus II software version 3.0 SP2. The previous behavior produced an uncharacterized delay that cannot be specified to fall within the specified 500 ps delay difference.</p>	<p>If your design uses this setting and does not work correctly after installing the Quartus II software version 3.0 SP2 or later, you should contact the Altera Applications department for further information.</p>

Stratix

Issue	Workaround
Designs compiled for Stratix EP1S40ES devices must be recompiled for the EP1S40 device before programming.	
Stratix PLL simulation models have been enhanced to handle jitter on the input clock. This enhancement has the unintended side effect that functional simulations for LVDS designs using cascaded PLLs may be incorrect by one clock cycle.	Altera recommends that you perform Timing Simulation to display the correct behavior in the Quartus II Simulator or in other EDA Simulators.

Stratix GX

Issue	Workaround
When using the <code>altlvds_tx</code> or <code>altlvds_rx</code> megafunction to set up a PLL with a Stratix II device, the default setting for all clocks, including core clocks and SERDES clocks, will be -180 degrees (with respect to the data rate frequency) compared to the input clock, which is required for legal SERDES operations. The <code>altlvds_tx</code> or <code>altlvds_rx</code> megafunction will automatically add this phase offset.	

Stratix II

Issue	Workaround
<p>Quartus II 4.2 software supports programming file generation for EP2S60 ES devices, but only for designs where the M-RAM memory is not used.</p>	<p>Programming file support for Stratix II designs using M-RAM memory will be provided in a Service Pack release. For more information about programming file support for Stratix II devices, please contact Altera Applications</p>
<p>The following Stratix II devices, EP2S90F780C4, EP2S90F780C5, EP2S130F780C4, EP2S130F780C5, are released in the Quartus II software version 4.2. The pin-outs for those devices are preliminary and will change. When compiled in the Quartus II software version 4.2 without a migration device selected, the Quartus II software will give the following message: "Compilation Report contains advanced information. Specifications for the device are subject to change. Contact Altera for information on availability. No pin-out will be generated" but will generate the pin-out in the report file. This pin-out will change in future releases of the Quartus II software.</p>	
<p>The Quartus II software may crash with an internal error if you have used one of the following combinations of I/O standard and On-Chip Termination value:</p> <p>1.8 V and 25 Ohm 1.5 V and 50 Ohm 1.8 V SSTL Class II and 25 Ohm 1.8 V HSTL Class II and 25 Ohm 1.5 V HSTL Class I and 50 Ohm</p>	<p>Manually assign pins with these combinations to Top or Bottom Edge in the Assignment Editor.</p>
<p>The Quartus II software may crash with an Internal Error if you try to assign a SignalProbe pin to a register that has been packed into an I/O element with the Auto Register Packing option.</p>	<p>Do not assign SignalProbe pins to packed registers.</p>

Issue	Workaround
<p>The Cell Delay box in the Resource Property Editor shows cell delays of only one of the ALMs in a Stratix II device (the other three are not shown).</p>	<p>You must select the individual node in the Resource Property Editor for which you want to see the cell delays.</p>
<p>Timing violations can occur on transfers from core registers to the LVDS SERDES transmit block on Stratix II devices for certain LVDS megafunction modes when appropriate timing constraints are not set.</p>	<p>When using the <code>altlvds_tx</code> megafunction for Stratix II devices, you have the choice of which clock registers the inputs of the TX instantiation (<code>tx_inclock</code> or <code>tx_coreclock</code>, where <code>tx_inclock</code> is the default). You also have the choice to turn on the Use shared PLL(s) for receiver and transmitter option, which is set to on by default. If you select the <code>tx_inclock</code> to clock the inputs to the LVDS megafunction, and the <code>tx_inclock</code> signal is not generated by the same PLL that clocks the high-speed SERDES registers, the timing requirements for this circuitry can be very complex. In particular, this case requires that you make multicyle assignments in order for timing to be correctly analyzed. These multicyle constraints are a function of the PLL clock offset, and other parameters. In the absence of user-entered multicyle constraints, the Quartus II software analyzes timing conservatively for this case, which may result in timing violations.</p> <p>The simplest way to avoid this issue is to ensure that the same PLL output feeds all the clocks in the LVDS TX block. In that case the Quartus II software automatically determines and applies the correct multicyle timing constraints, and no timing violations occur. Alternatively, you can set appropriate multicyle timing constraints for the transfer from the core registers to the LVDS TX block.</p>
<p>Back-annotating some designs targeted to a Stratix II device with the Demote cell assignments to option set to LABs may prevent the design from fitting.</p>	<p>Back-annotate the design with Demote cell assignments to turned off.</p>

Issue	Workaround
<p>If you are compiling a design for a Stratix II device that was originally targeted to a Stratix device, you may receive the following error message from the quartus_map executable if the design uses PLLs that have external clock outputs:</p> <pre> Info: Messages issued during the elaboration of <design_entity> Error: PLL pll uses extclk[2] output clock port, which cannot be remapped to clk port because target device does not have enough available clk ports." </pre>	<p>Enhanced PLLs on Stratix II devices have fewer output taps than Enhanced PLLs on Stratix devices. Therefore, you must reduce the number of taps on that PLL. If two taps have exactly the same configuration including their enables, you can merge them into a single tap. You must re instantiate the PLL in your source code with the MegaWizard Plug-In Manager, and recompile the design.</p>

Cyclone

Issue	Workaround
<p>Altera recommends that the frequency of the external clock output of the PLLs be limited to 312 MHz.</p>	
<p>The Cyclone EP1C3T100 device does not support the LVDS I/O standard on any pins.</p>	<p>Use the Cyclone EP1C3T144 device instead. It supports the LVDS I/O standard.</p>
<p>The operating frequency range of the Cyclone PLL has been changed. In the Quartus II software version 3.0 and earlier, the range was 300 MHz to 800 MHz. In version 3.0 Service Pack 1 and later, that range changed to 500 MHz to 1000 MHz because of concerns about jitter at frequencies below 500 MHz. Because of this change, the minimum input frequency is now 15.625 MHz (previously 15 MHz) and the minimum output frequency is also 15.625 MHz (previously 9.38 MHz).</p>	<p>Recompile your design after installing the current version of the Quartus II software.</p>
<p>The PLL lock circuit does not function correctly for PFD (Phase Frequency Detector) frequencies below 200 MHz when the temperature is below -20°C.</p>	<p>If operation at temperatures below -20°C is required, choose a higher input frequency and clock division (N) factor such that the PFD input frequency is higher than 200 MHz.</p>

Cyclone II

Issue	Workaround
Back-annotating some designs targeted to a Cyclone II device with the Demote cell assignments to option set to LABs may prevent the design from fitting.	Back-annotate the design with Demote cell assignments to turned off.

HardCopy Stratix

Issue	Workaround
When you run the HardCopy® Files wizard, you may receive messages similar to that shown in the example below: “Warning: Can't find required Hierarchy Database File (.hdb).”	The messages are erroneous and can be ignored safely. No action is required.
The pin table shown in the Quartus II online Help for the HC1S40F780 HardCopy Stratix device incorrectly shows pins U12 and U18 as user I/O.	These pins are factory test pins and should be connected to GND. Select the EP1S40_HardCopy_Prototype when compiling for this device.
When targeting HardCopy Stratix devices, the Quartus II software discards floating LogicLock regions of size [1,1] (including Auto-size regions with default dimensions) and may generate an internal error when processing LogicLock regions containing RAM.	Ensure that floating regions are of size greater than [1,1] and use location assignments for RAMs instead.

Design Flow Issues

Verification

Issue	Workaround
The simulation models for the LVDS_TX module in altera_mf are incorrect in the Quartus II software version 4.2.	Install the Quartus II software version 4.2 Service Pack 1 when it becomes available.
If you are using IP Toolbench to generate simulation models for Altera IP Megacore functions, you will get an error if the Stratix device family is not installed.	Install the Stratix device family.
Incremental routing may fail for nodes assigned to the SignalTap Logic Analyzer if you have turned on any of the Physical Synthesis Fitter optimizations, such as Perform physical synthesis for combinational logic or Perform register duplication or Perform register retiming .	
If you instantiate multiple VHDL instances of the SignalTap Logic Analyzer with the MegaWizard Plug-In Manager , you may receive error messages at compilation similar to this example: “Error: VHDL error at sld_signaltap.vhd (<number>): formal parameter <name> must have actual or default value.”	Choose another language, such as Verilog HDL.

Integrated Synthesis (VHDL and Verilog HDL)

Issue	Workaround
The Quartus II software version 4.0 and later may give the message “Error: Duplicate entity <name> found in file <filename1> colliding with the one found in file <filename2>,” for a project that compiled successfully with Quartus II 2.2 or earlier.	The Quartus II software gives an error message when it finds two or more entities with the same name. To avoid this error in the future, remove the duplicate entity or entities. If you cannot remove the duplicate entity, you can direct the Quartus II software to ignore the duplication by adding set_global_assignment -name IGNORE_DUPLICATE_DESIGN_ENTITY ON to your QSF file. Altera recommends that you avoid using this workaround if possible.

Verilog HDL Integrated Synthesis

Issue	Workaround
Verilog-2001 mode is enabled by default. This mode can cause some issues with Verilog-1995 designs, most commonly due to new reserved words in Verilog-2001 such as <code>config</code> .	Do not use Verilog-2001 reserved words as identifiers or select Verilog-1995 on the Verilog HDL input page under HDL Input Settings of the Settings dialog box (Assignments menu).
Verilog HDL escaped names that look like vectors can cause problems in the Quartus II software. For example, if you have a single-bit component port named <code>\my_vector_port [3:0]</code> , the Quartus II software versions 2.1 and later will treat it as an array port.	You should avoid using escaped port names in the Quartus II software version 2.1 and later.
Some designs that compiled successfully in the Quartus II software version 3.0 may fail with the error message “Index Z cannot be outside range (x to y) of array <name>.”	The Quartus II software version 4.0 and later does not allow out-of-bounds array accesses. The Quartus II software version 3.0 would return “don't care.” You must rewrite your design to keep array accesses within the valid range of the array.

SOPC Builder Issues

Issue	Workaround
When creating a component with the SOPC Builder Component Editor, you must not choose a component name that exactly matches the HDL file name or the top-level module name. If the names are the same, SOPC Builder will generate an error during system generation. This problem will be fixed in a future version of SOPC Builder.	Using the SOPC Builder component editor, rename the component to a different name. In the SOPC Builder table of active components, add the newly-named component to your system, and delete the old component.
If the Quartus II software is installed in a directory having space characters in its name, the SOPC Builder software will not run.	Install the Quartus II software in a directory that does not have space characters in the path.
When adding an Excalibur Stripe component in conjunction with Avalon peripherals, you may encounter SOPC Builder errors indicating too many masters are present.	If the master-connection patch-panel is not visible, choose Show Master Connections (View menu). Then click on the master/slave intersection indicated by the error message. This will remove the connection. Click again to restore the connection and the error will not reappear.

Issue	Workaround
<p>Designs targeting Excalibur devices that use Boot From Flash mode may not operate when downloaded to the target board if the Quartus II Software Builder or SOPC Builder Excalibur-build script was used to generate the flash programming file.</p>	<p>The Excalibur boot loader in the Quartus II software version 3.0 and later does not function correctly if the Quartus II Software Builder is used to generate the flash programming file. This is because the compression option that is used with the makeprogfile utility during the software build process does not work with this version of the boot loader. To work around this issue, do not use the Software Builder to generate a programming file, but instead use the makeprogfile utility at the command line with the <code>-nc</code> (no compression) option. If you are using the SOPC Builder Excalibur-build script, you must edit the script located in the <code>\<XA dev kit install directory>\bin</code> folder. Modify line 1034 of this script to remove the <code>-nc</code> option. For example, line 1034 should be changed as shown in this example.</p> <pre>\$command = "makeprogfile -nc -b \${fileBase}_bootdata.o \$SBD \$SBI \${fileBase}.hex";</pre> <p>You must recompile your software project for this change to take effect.</p>
<p>The SOPC Builder and Nios Software Development Kit shell may “hang” and become unresponsive when run while the Frisk antivirus software is running.</p>	<p>Turn off the Dynamic Virus Checking feature of the Frisk software before running SOPC Builder or the Nios SDK shell.</p>

SOPC Builder Compatibility

Nios version 3.1 and later

You can use your existing Nios components and they will be recognized automatically by the SOPC Builder integrated into the Quartus II version 4.2 software.

Nios version 2.2 / SOPC Builder 2.7

Your Nios components are not compatible with the SOPC Builder integrated with the Quartus II version 4.2 software. You will receive upgraded Nios components as part of a new Nios Development Kit. You can run your earlier version of SOPC Builder by following these steps:

1. If Altera SOPC Builder 2.7 is not shown in the **MegaWizard Plug-In Manager**, reinstall the SOPC Builder version 2.7 software, or copy the **sopc_builder_2_7_wizard.lst** file into your **\quartus\libraries\megafunctions** directory.
2. When you open a system that uses the Nios version 2.2 embedded processor, you will be given the choice of using the Altera SOPC Builder or the Altera SOPC Builder 2.7. Choose the 2.7 version. If you choose the version without a number your components will be disabled.

EDA Integration Issues

Issue	Workaround
The current version of the Quartus II software allows you to select the Synplicity Amplify software as a physical optimization tool. However, this setting is for an automated mode called ATOPS, which is currently not supported by the Amplify software.	Contact Synplicity for the support schedule for the Amplify software ATOPS mode.
Support has been added for generation of IBIS Output Files (.ibs) for EPCS1 and EPCS4 Serial Configuration Devices.	The IBIS file will be generated in the \<project name>\board\ibis directory after compilation when the design is targeted to a Cyclone device and Active Serial configuration scheme using EPCS1 or EPCS4 devices is chosen.

Issue	Workaround
A Synplicity VQM project that compiles successfully in the Quartus II software version 3.0 or earlier may fail when compiled with the Quartus II software version 4.0 and later with errors “Port A_IN does not exist in primitive <PRIM> of instance <inst_name>” and “Port A_OUT does not exist in primitive <PRIM> of instance <inst_name>”	This error can occur if your Quartus II project specifies that the Synplicity-generated VQM is a Verilog HDL file. Change the file type of the VQM to Verilog Quartus Mapping File in the Properties dialog box of the Files page of the Settings dialog box (Assignment menu)
NativeLink support does not work with versions of Precision RTL Synthesis Software earlier than version 2003b due to a change in Precision's project interface.	

Simulation Model Changes

altera_mf Models

Memory Models

Model	Change
altsyncram	<ul style="list-style-type: none"> • Performance improvements <ul style="list-style-type: none"> ○ Optimize address conversion calculation for port B when width_a is equal to width_b. ○ Set the byteenable mask register in separate combinational logic block.
dcfifo	<ul style="list-style-type: none"> • Added low latency FIFO support for Stratix GX, Hardcopy Stratix, and Cyclone device families.

DSP Models

Model	Change
altmult_add	<ul style="list-style-type: none"> • Added new parameters to recognize the port connectivity for ports addnsub1, addnsub3, signa, and signb in order to support Formal Verification. • Pipelined output port will be cleared when the aclr signal is asserted high.
altaccumulate	<ul style="list-style-type: none"> • The cout port will not be cleared when aclr is asserted high.
altsquare	<ul style="list-style-type: none"> • New model support. Used by <code>lpm_mult</code> only when the option is chosen.

I/O Models

Model	Change
altpll	<ul style="list-style-type: none"> Added new parameters to control the connectivity of <code>port_clkena*</code>, <code>port_extclkena*</code>, <code>port_extclk*</code>, <code>port_clkbad*</code>, <code>port_activeclock</code>, and <code>port_clkloss</code> ports. Default value for parameters <code>vco_multiply_by</code> and <code>vco_divide_by</code> changed to value 0 for correct Stratix II fast PLL clock output. Rename package name <code>pllpack</code> to <code>MF_pllpack</code> to avoid name collision and cause incorrect simulation output when <code>altera_mf.vhd</code> is simulated with the atom VHDL file.
altlvds_tx	<ul style="list-style-type: none"> Added support for Cyclone and Cyclone II device families.
altlvds_rx	<ul style="list-style-type: none"> Added support for Cyclone and Cyclone II device families. The RX model for Cyclone and Cyclone II is not working in this release.

220 Models

Model	Change
lpm_mult	Added support to accept constant input data through new parameters <code>INPUT_A_FIXED_VALUE</code> and <code>INPUT_B_FIXED_VALUE</code>
lpm_ff	<ul style="list-style-type: none"> <code>aclr</code> has a higher priority over <code>aset</code> when both are asserted Output will be <code>x</code> if <code>aclr</code> is set to <code>x</code>

Notes:

The ModelSim software version 5.8 gives the following warning when **altera_mf** or **220models** megafunction models are compiled with the -87 option:

```
*** Warning (vcom-1148) Condition in IF GENERATE must be static
```

You can safely ignore this warning because under the 1987 rules, the constant is not considered to be static because of the initialization from the function call.

RAM Megafunction models only support HEX format for all other EDA simulators. Manually convert MIF format to HEX first in the Quartus II software.

Latest Known Quartus II Software Issues

For known software issues after publication of this version of the Quartus II Software Release Notes, please look for information in the **Quartus II Latest Known Issues** section of the Altera Support Knowledge Database at the following URL:

[http://answers.altera.com/altera/index.jsp?/Topics/Support Solutions/Known Issues/Software/Quartus II](http://answers.altera.com/altera/index.jsp?/Topics/Support/Solutions/Known%20Issues/Software/Quartus%20II)

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