



# Quartus II Software Release Notes

November 2005

Quartus II version 5.0 Service Pack 2

This document provides late-breaking information about the following areas of this version of the Altera® Quartus® II software. For information about memory, disk space, and system requirements, refer to the **readme.txt** file in your `\altera\quartus<version number>` directory.

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## New Features & Enhancements

The Quartus II software version 5.0 Service Pack 2 includes the following new features and enhancements:

- Adds full programming support Cyclone™ II EP2C5, EP2C8, and EP2C50 devices.
- Incorporates software fixes for Cyclone II M4K memory issue and Stratix II M4K memory issue. For further information about these issues refer to the Cyclone II Errata Sheet and the Stratix II Errata Sheet, both of which are available on the Literature pages of the Altera web site.
- Incorporates software fix for Stratix, Stratix GX, and Cyclone Error Detection CRC issue.

## Project & Settings Files In This Release

The method that the Quartus II software version 4.0 and later uses to store assignments is substantially different from the method used by the Quartus II software version 3.0 and earlier.

If you wish to work on a project you created using the Quartus II software version 3.0 or earlier, you should open and save the project in the GUI once, even if you are using the command-line executables to compile your project. Opening and saving your project in the GUI ensures that your setting and assignment files are converted properly.

When you open a project created in the Quartus II software version 3.0 or earlier, the following changes are made to your assignment and setting files:

- Your *<project>.quartus* file is converted to the new Quartus Project File (**.qpf**) format, and the original file is moved to the *\<project>\<project>.bak* directory.
- The contents of your Compiler Settings File (**.csf**), Entity Settings File(s) (**.esf**), Simulation Settings File (**.ssf**), Project Settings File (**.psf**), and Software Build Settings File (**.fsf**) are merged into the new Quartus Settings File (*<project>.qsf*), and the original files are moved to the *\<project>\<project>.bak* directory.
- Once the Quartus II software has converted your files and moved the originals to the backup directory, the original files will not be used by the Quartus II software, so subsequent changes made to those files will be ignored.

# Device Support & Pin-Out Status

This section contains information about the status of support in the Quartus II software for the listed devices.

## Full Device Support

Full compilation, simulation, timing analysis, and programming support is now available for the following new devices and device packages:

### *Devices with Full Support*

Device Family	Devices	
Cyclone™ II	EP2C5T144	EP2C5Q208
	EP2C5F256	EP2C8T144
	EP2C8Q208	EP2C8F256
	EP2C5-F484	EP2C50F672

## Advance Device Support

Compilation, simulation, and timing analysis support is provided for the following devices that will be released in the near future. Although the Compiler generates pin-out information for these devices, it does not generate programming files for them in this release.

### ***Devices with Advance Support***

Device Family	Devices
None	

## Initial Information Support

Compilation, simulation, and timing analysis support is provided for the following devices that will be released in the near future. Programming files and pin-out information, however, are not generated for these devices in this release.

### ***Devices with Initial Information Support***

Device Family	Devices
None	

## Timing Models

This section contains a summary of timing model status in the current version of the Quartus II software.

### Preliminary Timing Models

The following table shows the devices with preliminary timing models in the current version of the Quartus II software:

#### ***Devices with Preliminary Timing Models***

Device Family	Device
Stratix II	EP2S180
Cyclone II	EP2C5*
	EP2C8*
	EP2C20*
	EP2C35*
	EP2C50*
	EP2C70*
MAX II	EPM240
	EPM570
	EPM1270
	EPM2210

\* These devices had significant changes to their timing models in the version 4.2 release of the Quartus II software. You should run the Timing Analyzer on your design to see any effects of these changes.

### Final Timing Models

The following table lists the devices with final timing models that are available in the current version of the Quartus II software:

**Devices with Final Timing Models**

Device Family	Device	Timing Models Final in Quartus II Version Number
APEX™ II	EP2A15	2.1
	EP2A25	2.1
	EP2A40	2.1
	EP2A70	2.1
Cyclone	EP1C3	3.0 SP1
	EP1C4	4.0
	EP1C6	3.0
	EP1C12	3.0 SP1
	EP1C20	3.0
FLEX 10K®	All	3.0
FLEX 10KA	All	3.0
Mercury™ <sup>(1)</sup>	EP1M120	2.1 SP1
MAX 3000 <sup>(1)</sup>	EPM3512A	2.1 SP1
MAX 7000 <sup>(1)</sup>	EPM7512B	2.1 SP1
MAX 7000S	All	3.0
MAX II	EPM240	5.0
	EPM1270	5.0
Stratix	EP1S10	4.1
	EP1S20	4.1
	EP1S25	4.1
	EP1S30	4.1
	EP1S40	4.1
	EP1S60	4.1
	EP1S80	4.1
Stratix II <sup>(2)</sup>	EP2S15	5.0 SP1
	EP2S30	5.0
	EP2S60	5.0
	EP2S90	5.0 SP1
	EP2S130 <sup>(3)</sup>	5.0 SP1
Stratix GX	EP1SGX10	4.1
	EP1SGX25	4.1
	EP1SGX40	4.1

(1) Timing models for devices in this device family not listed here became final in versions 2.1 and earlier.

(2) The timing models for Stratix II devices are updated in the Quartus II version 5.0 SP2 software. The change affects the performance of the M4K memory blocks. Additional changes in Quartus II version 5.1 affect I/O timing performance as discussed below. Altera recommends that you rerun timing analysis on affected Stratix II designs using the

new software. For additional details on the Stratix II timing model changes, please contact Altera Technical Services at <http://mysupport.altera.com>.

(3) The logic element timing models for the EP2S130 in the C3 speed grade have been updated in Quartus II version 5.1.

The current version of the Quartus II software also includes final timing models for the ACEX<sup>®</sup> 1K, APEX 20K, APEX 20KE, APEX 20KC, Excalibur<sup>™</sup>, FLEX<sup>®</sup> 6000, and FLEX 10KE device families. Timing models for these device families became final in versions earlier than version 2.1.

### **M4K Memory Block Changes**

- Performance reduced for dual-port dual-clock mode and packed single-port mode
- $f_{MAX}$  reduced by 14% in affected modes compared to v5.0 SP1 model
- Unregistered output delay ( $t_{CO}$ ) increased per speed grade compared to v5.0 SP1 model
  - C3 speed grade slows down by 280ps
  - C4 speed grade slows down by 322ps
  - C5 speed grade slows down by 306ps

### **Other Stratix II Timing Model Changes**

The Stratix II timing models in Quartus II version 5.1 software contain some corrections that are not provided in the Quartus II 5.0 SP2 software. These corrections affect the output delay capacitive load de-rating factors for LVTTTL, LVCMOS, HSTL, and SSTL I/O standards, output delays for SSTL outputs when On-chip Termination (OCT) is used, and cell delays for EP2S130 and EP2S180 in C3 speed grade. For more information on these corrections, please contact Altera Technical Services at <http://mysupport.altera.com>.

## EDA Interface Information

The Quartus II software version 5.0 supports the following EDA tools.

### Supported EDA Tools

Synthesis Tools	Version	NativeLink® support
Mentor Graphics® LeonardoSpectrum	2004b Update 1	✓
Synopsys Design Compiler	2004.09	
Synopsys Design Compiler FPGA	2005.03	
Synopsys FPGA Compiler II	3.8	✓
Mentor Graphics Precision RTL Synthesis	2004c Update 1	✓
Synplicity Synplify and Synplify Pro	8.1	✓
Magma Design Automation PALACE™	2.4	✓
Verification Tools	Version	NativeLink support
Cadence NC-Verilog (Windows)	5.4p001	✓
Cadence NC-Verilog (UNIX)	5.4s004	
Cadence NC-VHDL (Windows)	5.4p001	✓
Cadence NC-VHDL (UNIX)	5.4s004	
Cadence Verilog-XL (Windows)	3.3	
Cadence Verilog-XL (UNIX)	5.4	
Mentor Graphics ModelSim®	6.0c	✓
Mentor Graphics ModelSim-Altera	6.0c	✓
Mentor Graphics Tau	ISD 2004 SPac2	
Synopsys PrimeTime	2004.12	✓
Synopsys VCS / VCS MX	7.2	✓
Synopsys VSS	2002.06	
Synopsys Formality	2005.03	
Cadence Encounter Conformal	5.1	

## Changes to Software Behavior

This section documents instances in which the behavior and default settings of this release of the Quartus II software have been changed from earlier releases of the software.

## Changes to Default Settings in This Release

This section lists the variable names for Quartus II settings that have different default values in the Quartus II software version 5.0 from the previous version. The default values and a list of the changed values are stored in the \<Quartus II Installation directory>\bin\assignments\_default.qdf file.

Setting Keyword	Default in 4.2	Default in 5.0
SIMULATION_WITH_GLITCH_FILTERING	OFF	ON
SMART_RECOMPILE	ON	OFF

## Changes to Software Behavior

Items listed in the following table represent cases in which the behavior of the current release of the Quartus II software is different from a previous version.

Description	Workaround
The Quartus II software version 5.0 now supports Comma-Separated Value files (.csv) for using the PowerPlay Early Power Estimation spreadsheet with Stratix II and Cyclone II devices.	
You cannot use the Quartus II stand-alone Programmer to erase devices when you are using JAM files (.jam) or Jam Byte Code files (.jbc).	
Some designs that compiled without error in the Quartus II software version 4.2 and earlier may cause an error similar to the following example to be displayed, when compiled in the Quartus II software 5.0: Error: Fast PLL DPA-mode channels span rows 2 to 28, but location assignment of LVDS DPA-mode SERDES driven by PLL altlvds_rx:altlvds_rx_component  lvds_rx_9p31:auto_generated pll is not within 25 from driving fast PLL	Remove your pin assignments and recompile the design with the Quartus II software version 5.0.
The Quartus II software version 5.0 corrects a previous problem in which the Cyclone and Cyclone II CRC configuration oscillator was shown to run at 100 MHz rather than the 80 MHz rate correctly shown in the device family handbooks.	
In the Quartus II software version 5.0 and later, you can assign the <b>Allow XOR Gate Usage</b> logic option to individual nodes and entities. In previous versions, you could apply this logic option only to the entire design (that is, it was a global logic option).	

Description	Workaround
In the Quartus II software version 5.0 and later, if your Quartus II Settings File (.qsf) contains an error, you cannot compile the project until the error has been corrected. In previous versions, a warning message was displayed and compilation continued.	
In the Quartus II software version 5.0 and later, the <code>\altera\qdesigns&lt;version number&gt;\ll_makefile</code> directory has been replaced by the <code>\altera\qdesigns&lt;version number&gt;\logiclock_makefile</code> directory.	
The <code>altgxb</code> megafunction has been updated in the Quartus II software version 5.0. Any Stratix GX project that used the <code>altgxb</code> megafunction and was archived with the <b>Include functions from system libraries</b> option turned on will not compile correctly.	You must delete the <code>altgxb.tdf</code> file that is included in the project archive, and recompile your design.
The Quartus II software version 5.0 does not support Advanced NativeLink integration with the Synopsys VCS MX software.	
For all Stratix GX devices, a change has been made to the PLL settings in the gigabit transceiver blocks, which results in a reduction of total jitter for a specific data rate range. If your design has a data rate in the range of 1.01 Gbps to 1.25 Gbps, recompiling your design in the Quartus II software version 5.0 will result in a reduction in Transmit Total Jitter by ~35%.	
In the Quartus II software version 4.2 SP1 and later for UNIX and Linux workstations, the <b>Copy</b> command is disabled when the RTL Viewer, Technology Viewer, and certain Report window panes are open.	

Description	Workaround
<p>SOPC Builder systems using an Avalon Tri-State Bridge may fail to compile after upgrading to the Quartus II software version 4.2 and later due to an address width mismatch.</p>	<p>In the Quartus II software versions 4.1 and earlier, SOPC Builder created an extra most-significant-address bit for registered slave peripherals (also called native peripherals) connected to an Avalon Tri-State Bridge. If this bridge has only native slave devices connected to it, then some designers may have connected this extra address bit in their design to a peripheral. This extra address bit no longer exists if the embedded system is regenerated using the Quartus II software version 4.2 and later. If a design uses the extra address bit and the Quartus II software is upgraded to version 4.2 and later, a compilation error will occur due to the most significant address bit not being connected. This issue can be corrected without the need to modify software or hardware interconnects. If the peripheral affected by this issue is connected to an interface to user logic, then increasing the address width by one (in the interface to user logic) will correct the issue. If the peripheral affected by this issue is a custom component, edit the <b>class.ptf</b> file for that component by increasing the value called <code>Address_Width</code> by one.</p>
<p>For MAX 7000S family devices, the Quartus II software version 4.2 and later reports unused I/O pins as <b>RESERVED</b> by default, or as <b>RESERVED_INPUT</b> if the setting <b>Reserve all unused pins as inputs, tri-stated</b> is selected. Previous versions report unused I/O pins as <b>GND*</b>, which is incorrect for MAX 7000S family devices.</p>	<p>To generate a correct pin-out file (<b>.pin</b>), recompile any MAX 7000S designs that were created in earlier versions of the Quartus II software.</p>

Description	Workaround
<p>The Quartus II software version 4.2 and later prohibits the placement of the IOE registers within the same LAB row as a SERDES RX or TX channel. IOE registers must be placed at least one LAB row away from an RX or TX channel. The Quartus II software version 4.1 SP2 and earlier does not prohibit the use of IOE registers in the same LAB row as a receiver (RX) or transmitter (TX) channel that utilizes the SERDES block.</p>	<p>Recompile any Stratix II design that was created in an earlier version of the Quartus II software with the current version. The setup time of the register (<math>t_{SU}</math>) will increase if the IOE register is moved to the PLD core. It is up to the designer to ensure that all setup times are met. Contact Altera Applications for more details.</p>
<p>The Tcl Console Window is disabled while a compilation or simulation flow is in progress. This behavior is necessary to prevent inadvertent changes to settings files during compilation.</p>	<p>Wait until compilation or simulation is complete before trying to run a Tcl command in the Tcl Console.</p>
<p>The <code>p11</code> megafunction has been removed from the Quartus II software version 4.2 and later. This megafunction implemented a digital PLL in logic cells, and was maintained for backward compatibility only.</p>	<p>If you wish to still use the <code>p11</code> megafunction rather than the <code>altpll</code> or <code>altclklock</code> megafunctions, you must copy the <b><code>pll.inc</code></b> and <b><code>pll.tdf</code></b> files from the <i>&lt;Path to Quartus II installation&gt;/mega</i> directory of a previous version and place them in the same directory of the current version.</p>
<p>The PLLs in Stratix, Stratix II, and Stratix GX device families no longer support delay shift (time delay elements).</p>	<p>Altera recommends using the phase shift feature of the <code>altpll</code> megafunction to implement time shifts.</p>
<p>The Quartus II software version 4.2 and later no longer supports the <code>-entity</code> option for the <code>LL_IMPORT_FILE</code> assignment.</p>	<p>You must make the <code>LL_IMPORT_FILE</code> assignment for each instance of the entity to which you want to make the assignment.</p>

Description	Workaround
<p>In the Quartus II software version 4.2 and later, the RAM atom simulation models have changed in the following ways:</p> <ol style="list-style-type: none"> <li>1. In the Quartus II software version 4.1 and earlier, all ports on the RAM atom had fixed widths (data port width=144, address port width=16, and so on). Starting in version 4.2, the widths of all ports are parameterized.</li> <li>2. The default port width in the simulation model is 1 (that is, if an input is not used, it is assumed that the width of that input is 1).</li> <li>3. Instead of using parameters such as MEM1,..., MEM9 to hold initialization data for RAM, two parameters called “MEM_INIT0 and MEM_INIT1” are used. The MEM_INIT0 parameter holds lower bytes of initialization data in increasing order of address up to a maximum of 2048 bits. The MEM_INIT1 parameter holds the remaining upper bytes.</li> </ol>	<p>You must recompile your project in the Quartus II software version 4.2 or later to generate new Verilog Output files (.vo) or VHDL Output files (.vho) for the simulation tool.</p> <p>If your design runs at a clock speed of greater than 500 MHz, you must set the simulation resolution to picoseconds (ps).</p>
<p>The Quartus II software no longer uses the registry to store non-user interface-related settings. Non-user interface-related settings are stored automatically in the <b>quartus2.ini</b> file when you open the Quartus II software user interface for the first time.</p>	<p>You must open the Quartus II software user interface at least once before using the command-line version of the software.</p>
<p>The following Tcl simulator commands are no longer supported by the Quartus II software version 4.0 and later:</p> <ul style="list-style-type: none"> <li>• dbg</li> <li>• get_time</li> <li>• get_value</li> <li>• force_value</li> <li>• release_value</li> <li>• read_memory</li> <li>• write_memory</li> <li>• run</li> <li>• print</li> <li>• get_memory_width</li> <li>• get_memory_depth</li> <li>• testbench_mode</li> </ul>	<p>There are new versions of most of these commands in the <b>::quartus::simulator</b> package, which is available in the <b>quartus_sim.exe</b> module. Refer to the Quartus II Command-Line and Tcl API Help for more details. To view Tcl online Help type the following command at a command prompt:</p> <pre>quartus_sh --qhelp &lt;Enter&gt;</pre>

Description	Workaround
<p>When you instantiate a new RAM or ROM function with the <b>MegaWizard Plug-In Manager</b>, the outputs of the memory function will be registered using the same clock as the inputs, by default. This is a change of behavior in that the Quartus II software versions earlier than version 4.0, the outputs are not registered by default.</p>	<p>This is a change of behavior that affects only new instantiations of RAM or ROM function. Existing memory functions are not affected.</p>
<p>In the Quartus II software version 3.0 and earlier, LogicLock™ assignments are stored in lowercase. In version 4.0 and later, designs written in case-sensitive languages may require that LogicLock assignments be in mixed case. Due to the difference in case-sensitivity between versions, LogicLock assignments made in the Quartus II software version 3.0 and earlier may not be usable in the Quartus II software version 4.0 and later.</p>	<p>Do not use upper case or mixed case in your HDL design files.</p>
<p>When you are using formal verification tools with a design that contains LogicLock regions that was compiled with the Quartus II software version 3.0 or earlier, under certain circumstances when you open the design in the Quartus II software version 4.0 and later, the LogicLock regions will not be handled properly.</p>	<p>Redefine the LogicLock regions in the Quartus II software version 4.0 or later to eliminate the errors.</p>
<p>Changes made to settings and/or assignments in the Assignment Editor, Floorplan Editor, or with Tcl commands in the Tcl Console window are saved to disk only when you click <b>Save Project</b> on the File menu. Clicking <b>Save</b> in the Assignment Editor, Floorplan Editor, or <b>Settings</b> dialog box saves the changes to memory only. They are not committed to disk until you click <b>Save Project</b> on the File menu, close the project, or exit from the Quartus II software. If you have turned off <b>Save changes to all files before starting a compilation, simulation, or software build</b> on the <b>Processing</b> page of the <b>Options</b> dialog box, changes you made may not be reflected in the latest compilation.</p>	<p>Turn on <b>Save changes to all files before starting a compilation, simulation, or software build</b> on the <b>Processing</b> page of the <b>Options</b> dialog box.  <i>or</i>  Click <b>Save Project</b> on the File menu after making any changes to settings or assignments.</p>

Description	Workaround
In the Quartus II software version 4.0 SP1 and later, the labeling of unused GXB_TX and GXB_RX pins has changed.	Pins previously labeled GXB_VCC+ are now labeled GXB_VCC*. Pins previously labeled GXB_GND+ are now labeled GXB_GND*.
The behavior of the Quartus II Fitter has been modified to minimize compilation time when there are no timing constraints applied to the design. This change in behavior results in an average of 40% faster compilation times and an average of 15% slower $f_{MAX}$ performance. This change to the Fitter behavior applies only when the <b>Auto Fit</b> option is chosen for <b>Fitter Effort</b> on the <b>Fitter Settings</b> page of the <b>Settings</b> dialog box on the Assignments menu, and affects only Stratix, Stratix GX, Stratix II, Cyclone, and Cyclone II device families.	To return to the same behavior as earlier versions of the Quartus II software, choose <b>Standard Fit</b> under <b>Fitter Effort</b> on the <b>Fitter Settings</b> page of the <b>Settings</b> dialog box on the Assignments menu, or apply appropriate timing constraints.
The following megafunctions have clear box simulation models that contain assignments that are not stored in the Quartus Settings File (.qsf) and are not written out to a Verilog Quartus Mapping File (.vqm): altdqs altdq altddio_bidir altddio_out altddio_input altlvds_rx altlvds_tx altufm_i2c dcfifo	Do not save your atom netlist file as a VQM file if you are using these megafunctions.
The following megafunctions now use clear box models instead of the generic model libraries: altmemmult altufm altdq altdqs altremoteupdate altpll_reconfig altclkctrl	When you are simulating a design that uses one of these megafunctions, you must use the family-specific atom model library (such as <b>stratix_atoms.v</b> ) instead of the generic <b>altera_mf.v</b> (or <b>.vhd</b> ) library.

# Known Issues & Workarounds

## General Quartus II Software Issues

Issue	Workaround
<p>After you compile a design for any device in the ACEX 1K, APEX 20K, APEX 20KE, APEX II, FLEX 10KE, MAX 3000, MAX 7000AE, or MAX 7000E families, and you have specified a migration device; when you open the Pin Planner, turn on <b>Show Fitter Placement</b>, and then click <b>Refresh</b>, the Quartus II software crashes with an internal error.</p>	<p>Remove the migration devices, recompile the design, open the Pin Planner, and then turn off <b>Show Fitter Placement</b>. You can then specify a migration device for your design.</p>
<p>Compiling a design that includes the DDR SRAM Controller core that is targeted to a device that does not have pin-out information in the Quartus II software, causes that compilation to fail.</p>	<p>Chose a device that has pin-out information in the Quartus II software.</p>
<p>If you make a single-point CUT=ON assignment to a node, and then override it with a point-to-point CUT=OFF assignment on a specific path, the OFF assignment will not be honored.</p>	
<p>If you open any optimization advisor, and you have not performed Analysis &amp; Synthesis yet, clicking any button in the advisor will cause the Quartus II software to crash with an internal error.</p>	<p>Perform Analysis &amp; Synthesis before opening any optimization advisor.</p>
<p>Under certain circumstances the Design Assistant reports Critical Warnings (that locate to the <code>altlvds_rx</code> megafunction) for your project, which uses the <code>altlvds_rx</code> megafunction or an IP core that uses the <code>altlvds_rx</code> megafunction.</p>	<p>These warnings can be safely ignored; no action is necessary.</p>

Issue	Workaround
<p>When you compile a design that uses the JTAG-to-core interface (SignalTap® II, In-System Memory Content Editor, Nios II JTAG UART, OpenCore Plus hardware evaluation, or Serial or Parallel Flash Loaders) for MAX 3000, MAX 7000, ACEX 1K, or FLEX 10K devices, the design will compile correctly, but the feature that uses the JTAG-to-core interface will not function.</p>	<p>Choose another device family. The MAX 3000, MAX 7000, ACEX 1K, and FLEX 10K device families do not support the JTAG-to-core interface.</p>
<p>When connection labels and arrowheads are shown in the Chip Editor Bird's Eye View, turning off the <b>View-&gt;Timing Labels</b> (shortcut menu) option does not cause the labels to be removed from the Bird's Eye View.</p>	<p>Resize the <b>Bird's Eye View</b> dialog box or turning the <b>View-&gt;Timing Labels</b> option on and back off will refresh the display and cause the labels to be removed.</p>
<p>You may receive a "License not found..." error if the path to the license file contains non-ASCII characters.</p>	<p>Change or remove any non-ASCII characters from the license file path.</p>
<p>If your design uses LogicLock regions, and you use the <code>set_global_assignment -name PROJECT_SHOW_ENTITY_NAME OFF</code> assignment, your design may not fit correctly.</p>	<p>Either remove the assignment, or set the value to ON, which is the default.</p>
<p>Changing the number of registers in the routing for a SignalProbe™ pin and then recompiling the design sometimes results in a message similar to the following example: "Warning: Following 1 pins have nothing, GND, or VCC driving datain port."</p>	<p>Perform the following steps:</p> <ol style="list-style-type: none"> <li>1. Turn off the SignalProbe assignment you want to change.</li> <li>2. Recompile the design.</li> <li>3. Turn on the SignalProbe assignment and change the number of registers.</li> <li>4. Start a SignalProbe compilation.</li> </ol>
<p>During a SignalProbe compilation, you might receive warning message(s) similar to the following example: "Routing constraints for signal &lt;signal_name&gt; seem to be causing unresolvable routing congestion. The constraints for the signal were removed."</p>	<p>The Compiler issues these warnings when it is unable to retain the routing constraints from a previous compilation because those routing resources were needed by the SignalProbe signal routing.</p>

Issue	Workaround
If you modify a resource (node or connection) used by a SignalProbe pin using the Resource Property Editor and then perform another SignalProbe compilation, the compilation will fail and the Quartus II software may crash with an internal error.	Do not use the Chip Editor features (Resource Property Editor, Chip Editor, or Engineering Change Manager) to modify properties of SignalProbe pins.
Not all speed grades of a given device share the same features.	Refer to the Altera device handbook or data sheet for further information.
There is no distinction between output ports and bidirectional ports in AHDL Function Prototypes; instead, all ports listed after the RETURNS keyword are treated as output ports. As a result, if you specify a bidirectional port in a logic function's Function Prototype Statement and do not connect the port to a top-level bidirectional pin or to other logic in the design where you instantiate the logic function, an error can occur.	Connect the port to a top-level bidirectional pin or to other logic in the design.
Context-sensitive Help is not available for some items in the Quartus II software.	To locate Help on those items, click <b>Index</b> on the Help menu and type the name of the item.
The Timing Analyzer does not recognize non-PLL clock signals when using any PLL megafunction.	Make clock settings assignments to all non-PLL clocks.
The Waveform Editor does not allow you to create a bus with nodes that are nonconsecutive members of a bus.	Create buses only with nodes that are consecutive members of a bus. Or, use the <b>Group</b> command on the Edit menu to create groups of arbitrary nodes.
If you are using the <code>altcam</code> , <code>altclklock</code> , <code>altlvds_rx</code> , or <code>altlvds_tx</code> megafunctions, the equations shown in the Equations Section of the Compilation Report are not complete.	To view the complete equations for any of these megafunctions, use the Equations window of the Timing Closure Floorplan.
The Quartus II software does not support design file names with more than one extension. For example, you cannot use the file name <b>file.eda.edif</b> .	Use design file names with only one extension.
If you install the Quartus II software for PCs on a UNIX server that exports shares with the Samba software version 1.9.18p10, you may experience problems accessing project files that are also on the network.	Altera recommends using version 1.9.16p11 or 2.0 of the Samba software.

Issue	Workaround
If you make assignments to reserve pins as a group or with group notation (debug [7..0]), the Quartus II software does not correctly generate simulation output files, and you receive a warning message saying “Unsupported data type in the top-level module.”	Reserve the pins using single-name notation (for example, debug [7], debug [6], and so on).
Do not change the file permissions (such as changing “read-only” to “read and write”) of Quartus II Settings File (.qsf) and Quartus II Project File (.qpf) while a Quartus II project is open.	Close the Quartus II project before making changes to the file permissions.
Node names containing numbers greater than 2 <sup>31</sup> -1 (2147483647) will cause an Internal Error in the Quartus II software.	Do not use node names containing large numbers.
Occasionally the Programmer does not allow you to use a MAX 7000AE Programmer Output File (.pof) with a MAX 7000AE device. This error sometimes occurs after a compatible MAX 7000B device is used with the MAX 7000AE POF.	Do not switch between compatible MAX 7000B and MAX 7000AE devices when a MAX 7000AE POF is loaded, or reload the MAX 7000AE POF.
Routing back-annotation may fail if the back-annotated locations do not match the location assignments in the Quartus II Settings File (.qsf) or if the location assignments are missing. This problem can occur if you change devices, or if you remove some location assignments by using the <b>Assignment Editor</b> on the Assignments menu or by manually editing the QSF.	If you experience a “no fit” or an Internal Error while using routing back-annotation, delete the Routing Constraints File (.rcf) and back-annotate the design again after a successful compilation.
If you receive an error message saying “System resources low...” or if the user interface is slow in responding and there is a lot of disk activity when you are not compiling a design, your system may be running out of free memory.	You can recover system memory by clearing messages from the Messages window. To clear messages from the Messages window, right-click anywhere in the Messages window and choose <b>Clear Messages from Window</b> (shortcut menu). Additional memory can be recovered by closing the Timing Closure Floorplan.
Occasionally, the Quartus II software may crash or hang with no error message immediately upon opening a project.	Delete the Quartus Workspace File (.qws) <project name>.qws from the project directory. If the problem persists, delete the <project directory>\db directory.

Issue	Workaround
When you are setting phase shift and duty cycle values for clock signals using the <code>altpll</code> megafunction, some combinations of settings may result in values that cannot be synthesized exactly. Under certain circumstances, the Quartus II software attempts to synthesize the phase shift parameter before the duty cycle parameter.	You should first select values for the parameter (phase shift or duty cycle) that is most important for your design.
During compilation or simulation, the Quartus II software may “hang” and not proceed to the next module if a menu or modal dialog box is open at the time the current module finishes running.	Close any open menus or modal dialog boxes before the compilation or simulation reaches the next stage.
Running individual Quartus II software executables ( <b>quartus_map</b> , <b>quartus_fit</b> , and so on) from within the Quartus II Tcl Console may cause the Quartus II software to crash.	You should run individual executables either from within the Quartus II scripting shell ( <b>quartus_sh</b> ) or directly at a command prompt.
If you have chosen migration devices in the <b>Compatible Migration Devices</b> dialog box, which is available from the <b>Device</b> page in the <b>Settings</b> dialog box on the Assignments menu, the Timing Closure floorplan displays only the pins and PLLs that are common to all the selected devices. However, the Chip Editor displays all the pins and PLLs available for the device specified for compilation.	
The time shown in the Status window may not agree with the processing times reported in the Compilation Report. This difference is due to differences in how the times are calculated during processing.	
If you type a name in the entity column of the Assignment Editor that differs from an existing name only by case, the Assignment Editor’s “auto-completion” feature always uses the existing name.	Type the new entity name in another application, such as a text editor, copy it to the clipboard, and paste the name from the clipboard into the Assignment Editor.
Altera recommends that you do not use node or entity names that differ only by case if you are using the Quartus II Simulator or Waveform Editor.	

Issue	Workaround
Under certain circumstances, a design that uses <b>Virtual Pin</b> assignments may fail to fit after back-annotation. This situation occurs because the clock signals chosen automatically for the first compilation do not match those chosen for the second compilation.	Manually assign your clock signals, using <b>Virtual Pin Clock</b> assignments before the first compilation, or use Advanced Back-Annotation to explicitly write out the virtual clock assignments before the second compilation.
If you use the <code>dcfifo</code> or <code>scfifo</code> megafunctions in an AHDL design, you may receive an error message similar to “The parameter <code>LPM_WIDTHU</code> has been set to an invalid value...”	Either remove the <code>LPM_WIDTHU</code> parameter arguments from your AHDL <code>dcfifo</code> or <code>scfifo</code> megafunction instantiation, or explicitly set the <code>LPM_WIDTHU</code> parameter to <code>ceil(log2(LPM_NUMWORDS))</code> .
If you use the <b>MegaWizard Plug-In Manager</b> to create files for your design, the Quartus II software might not retain your settings for device and so on.	The Quartus II software does not write your settings to the Quartus Settings File ( <code>.qsf</code> ) until you close the <b>MegaWizard Plug-In Manager</b> . You must save your settings with the <b>Save Project</b> command on the File menu.
Do not open, change permissions, or delete the <code>&lt;project directory&gt;/db</code> directory or any file therein while any Quartus II executable is running.	
If you are using the IP Toolbench and add a user library, the Quartus II software may add a backslash ( <code>\</code> ) to the end of the library file name. The Quartus II user interface ignores this trailing backslash.	
Support for nondecimal radix numbers (such as hexadecimal) used as constants in the <code>lpm_constant</code> , <code>lpm_compare</code> , and <code>lpm_add_sub</code> megafunctions is limited to values that can be represented by 31 bits or fewer.	For values that require more than 31 bits, use decimal radix only.

Issue	Workaround
<p>Under certain circumstances, back-annotation of routing in unreserved LogicLock regions can cause unsatisfiable routing constraints for signals going to clock and clock-enable ports of LABs. This can occur when other portions of the design are not back-annotated, and the Fitter populates empty LCELLs in the back-annotated LogicLock region during subsequent compilations.</p> <p>For example, assume that on the initial compilation, LogicLock region L contains register A, which uses the CLK1 and ENA1 ports of a LAB. When the design is recompiled, the Fitter may place register B, which is not part of region L, and uses the SLOAD input, in the same LAB as register A (assuming that the LAB has sufficient empty space to accommodate it).</p> <p>The LAB control signal generation block does not allow use of both ENA1 and SLOAD in the same LAB; therefore, register A must use the CLK0 and ENA0 ports, rather than CLK1 and ENA1. To avoid a no-route situation, the Fitter will ignore the routing constraints for the clock and enable signals, and re-route the signals using the appropriate control signal multiplexing for the CLK0 and ENA0 ports of the LAB. The Fitter picks the most appropriate routing and, in the majority of cases, the circuit's timing is not adversely affected. When the Fitter is forced to ignore routing constraints, info messages of the form "Info: Can't route signal &lt;name&gt; to atom &lt;name&gt;" are displayed to inform the user; the appearance of such messages is not a cause for alarm.</p>	<p>This situation can be avoided entirely by marking all LogicLock regions as Reserved, thereby preventing the Fitter from placing new items in a region. The tradeoff, of course, is that should a Reserved LogicLock region be under-utilized, the Fitter will be unable to place other logic items in the unused portion of the region.</p>

## Platform-Specific Issues

### Windows Platforms Only

Issue	Workaround
<p>If you receive an error message similar to the following example “The procedure entry point <code>__lc_collate_cp</code> could not be located in the dynamic link library <code>MSVCRT.dll</code>” when you launch the Quartus II software, your Windows system has a very old version of the <b>msvcrt.dll</b> file.</p>	<p>You must update the <b>msvcrt.dll</b> file before you can run the Quartus II software. You can download the Microsoft Libraries Update from the following link:  <a href="http://www.microsoft.com/windows98/downloads/contents/WURecommended/S_WUFeatured/Libraries/Default.asp">http://www.microsoft.com/windows98/downloads/contents/WURecommended/S_WUFeatured/Libraries/Default.asp</a></p>
<p>You cannot access the web-based PowerPlay Early Power Estimator on the Altera web site if you have installed Windows XP SP2 because the service pack blocks the active content.</p>	<p>Refer to the Altera Knowledge Database on the Altera web site for more information on enabling your browser to access the PowerPlay Early Power Estimator spreadsheets.</p>
<p>Some dialog box title bar text is not displayed correctly when the Quartus II software is installed on a computer running the Chinese version of Windows XP.</p>	<p>Change the font in the <b>Active Title Bar</b> section of the <b>Windows Appearance</b> Control Panel.</p>
<p>If you do not have Administrator privileges when you install the Quartus II software, certain features of the software, particularly the online help, will not work properly.</p>	<p>Altera recommends that you have Administrator privileges when installing the Quartus II software.</p>
<p>Under certain circumstances, the Quartus II installation program may crash or you may receive an error message immediately upon launching the installation program.</p>	<p>Reinstall the <b>stdole32.tlb</b> file from the original Windows distribution disks. To reinstall the file, type the appropriate command at a command prompt. (Note: the command must be typed on one line.)</p> <p><b>Windows 2000:</b> &lt;CD-ROM drive letter&gt;:\i386\expand.exe stdole32.tl_ %SystemRoot%\System32\stdole32.tlb &lt;Enter&gt;</p> <p><b>Windows XP:</b> &lt;CD-ROM drive letter&gt;:\i386\expand.exe stdole32.tl_ %SystemRoot%\System32\stdole32.tlb &lt;Enter&gt;</p>

Issue	Workaround
If the full, hierarchical name of an instance exceeds 247 characters, it may not be displayed properly in the Quartus II user interface. This problem occurs most often with EDIF netlist files generated by other EDA synthesis tools.	Limit the full, hierarchical instance name to fewer than 247 characters if possible.
Due to a limit of the Windows operating system, path names longer than 229 characters can cause an internal error in the Quartus II software.	Make sure that all path names do not exceed 229 characters. This limitation applies to UNIX and Linux installations also.
If you are running the Quartus II software from a network server, the Quartus II software will not run properly on the client computer if you share the <code>\quartus\bin</code> directory.	You must share the <code>\quartus</code> directory, not the <code>\quartus\bin</code> directory.
The Quartus II software is not compatible with the MATLAB web server.	Turn off the MATLAB web server in the <b>Services Control Panel</b> on the Start menu before running the Quartus II software.
Under some circumstances, the Quartus II splash screen appears and the Quartus II icon appears in the Taskbar, but the graphical user interface does not appear. Under other circumstances, the user interface appears but windows and/or toolbars do not appear correctly.	The registry settings controlling the position of the Quartus II windows may have become corrupted. If the user interface appears, click the <b>Reset All</b> button on the <b>Toolbars</b> page of the <b>Customize</b> dialog box, or if the user interface does not appear, type the following command at a command prompt: <code>quartus -reset_desktop &lt;Enter&gt;</code>
If you install the stand-alone Quartus II Programmer and the Quartus II software, and then uninstall either one, the Programmer may report “JTAG Server -- internal error code 82 occurred” when you click the <b>Add Hardware</b> button in the <b>Hardware Setup</b> dialog box on the Edit menu. This error occurs because uninstalling the software has disabled the JTAG Server service.	Manually restart the JTAG Server service by locating the <code>jtagserver.exe</code> program and at a command prompt for that directory, type <code>jtagserver --install &lt;Enter&gt;</code>
If you choose to uninstall a previous version of the Quartus II software during installation, and there is a “locked” file or directory, the installation program will not reboot the computer as is necessary to successfully complete the installation.	Exit from the installer and reboot the computer manually after the removal of the previous version is complete, before completing the installation of the new version.

Issue	Workaround
The Quartus II software version 4.2 and later does not allow a Parallel Port Software Guard (T-guard or dongle) to be used on the same parallel port as a ByteBlaster™ II download cable.	Use another download cable, such as a USB-Blaster or MasterBlaster™ to configure your device, or use separate parallel ports for the Software Guard and the download cable. The Quartus II Programmer is not a licensed feature, so you can remove the Software Guard to program your device, but you must replace it to use any other Quartus II software features. You can also use the USB Software Guard.
During installation of the Quartus II software, when you insert the ModelSim-Altera CD-ROM, a Windows Explorer window may appear.	Close the Windows Explorer window before proceeding with the installation.

### Solaris, HP-UX & Linux

Issue	Workaround
On certain Solaris 8 and Linux systems, the text in the Assignment Editor, and other dialog boxes, may not be readable because of the text size.	Delete or move the <code>~/.mw</code> directory and restart the Quartus II software.
If the operating system crashes, and the file system in <code>\$TMP</code> is rebuilt automatically, the data in the <code>\$TMP/Mw_&lt;user ID&gt;</code> file is corrupted, the Quartus II software may fail to start correctly.	Delete the <code>\$TMP/Mw_&lt;user ID&gt;</code> file and restart the Quartus II software.
If you are using the Exceed X server software for Windows while running the Quartus II software, the font size may be larger than the line height. This problem occurs most often if you installed the Exceed software while running at a screen resolution greater than $1024 \times 768$ .	Reinstall the Exceed software while running at a screen resolution of $1024 \times 768$ . You can then switch back to your normal, higher resolution setting.
Under some circumstances, there may be editor windows listed in the Window menu that you cannot see.	To display the hidden windows, click <b>Cascade</b> on the Window menu.
You cannot launch the AXD Debugger software from within the Quartus II software.	Launch the AXD Debugger software from outside the Quartus II software.

Issue	Workaround
Under some circumstances, the Internet connectivity features of the Quartus II software are not functional.	Specify the full path to your web browser software on the <b>Internet Connectivity</b> page of the <b>Options</b> dialog box. If you access the Internet through a proxy server, you must also specify the address of the proxy server and its port number.
Under some circumstances you cannot access the Quartus II online Help in the user interface.	To access Help, type <code>hh quartus.chm</code> <Return> at a command prompt.
If you are accessing the Quartus II software through one of the following versions of the Hummingbird Exceed software (6.2, 7.0, 7.1, or 8.0) and have any Microsoft Office application or Internet Explorer open, the Quartus II user interface may start very slowly.	Contact Hummingbird Software at <b>www.hummingbird.com</b> for a patch for the Exceed software.
If you are running the Quartus II software version 4.0 and later on a Linux or Solaris workstation, even though <b>Reopen current project and files at startup</b> is turned on, the last project is not reopened when you restart the software.	Use the <b>Recent Projects</b> command on the File menu to reopen your last project.
The stand-alone Quartus II Programmer and SignalTap II programs are not available on Solaris, Linux, and HP-UX workstations.	
If you double-click or click and hold on drop-down list boxes in the Resource Property Editor, the Quartus II software may crash.	
When you are changing values in the Resource Property Editor, you must press the Return key to apply the changed values.	

**Solaris Only**

Issue	Workaround
The <b>ARM-based Excalibur MegaWizard Plug-In</b> , which is available from the <b>MegaWizard Plug-In Manager</b> , requires the Java Runtime Environment (JRE), which has already been installed on your computer. On Solaris workstations, however, you may need to install extra patches to the operating system in order for the JRE to function properly.	Check the web site <a href="http://sunsolve.sun.com/pub-cgi/show.pl?target=patches/J2SE">http://sunsolve.sun.com/pub-cgi/show.pl?target=patches/J2SE</a> for information about any patches that might be needed.
On certain Solaris 8 systems, the position and size of the Help window are not maintained when the Quartus II software is closed and then started again.	Install Solaris OS patch 109147-12 or higher to regain the normal Help functionality.

**HP-UX Only**

Issue	Workaround
The <b>Hardware Setup</b> dialog box does not appear after you click <b>Setup</b> in the SignalTap II or In-System Memory Content Editor.	If you need to select an existing communications cable, use the <b>Hardware</b> list. If you need to set up a new communications cable, use the <b>Hardware Setup</b> dialog box in the Programmer.
You receive error messages indicating that you do not have required permissions to perform the requested operation while using Network Information Services (NIS).	Add a plus-sign (+) followed by a carriage return on a line by itself as the last line in both of the following files: <b>/etc/passwd</b> and <b>/etc/group</b> .
Programming EPC16 configuration devices is disabled on HP-UX workstations.	

**Linux Only**

Issue	Workaround
The 64-bit version of the Quartus II software for Linux workstations does not support device programming in this release.	Use the 32-bit version of the Quartus II software to program your device.
If you include a slash (/) at the end of the file path name in a file browse dialog box, the Quartus II software may crash.	Do not include a slash (/) at the end of file path names.

Issue	Workaround
<p>When you type a new value in a drop-down list in the Assignment Editor, the value is sometimes not changed after you press &lt;Return&gt;.</p>	<p>You must explicitly close the list with the up-arrow icon before pressing &lt;Return&gt;.</p>
<p>If the MasterBlaster download cable is not listed in the <b>Available hardware items</b> list in the <b>Hardware Settings</b> tab of the <b>Hardware Setup</b> dialog box, but it is connected properly, you may not have read/write permission for the serial (<code>dev/ttySx</code>) port to which the MasterBlaster cable is connected.</p>	<p>Have a system administrator assign read/write permission for the appropriate port. This change can be accomplished by adding you to the “uucp” group, or by giving read/write permission for the serial port to everyone, using the following command:  <code>chmod o+rw /dev/ttySx</code>                      where <i>x</i> is the serial port affected.</p>
<p>If you are using the ReflectionX X-server software as your display on a Linux workstation, the Quartus II software may hang and a white box may appear.</p>	<p>Set the <code>QUARTUS_MWWM</code> environment variable to <code>allwm</code> and then start the Quartus II software without the splash screen by typing the following commands at a command prompt:  <code>setenv QUARTUS_MWWM allwm &lt;Return&gt;</code>  <code>quartus -no_splash &lt;Return&gt;</code></p>
<p>Under certain circumstances, the Quartus II software may not start properly.</p>	<p>On a system with a static IP address, ensure that the <code>/etc/hosts</code> file has an entry for the hostname of the machine on which you are running. For example, if the workstation is named “orange,” there should be an entry in <code>/etc/hosts</code> with the IP address of the “orange” workstation as shown below:  <code>&lt;IP address of orange&gt; orange</code>                      In addition, the network configuration (hostname, DHCP hostname, DNS search path, and domain names) must be correct or the Quartus II software will abort on startup.</p>
<p>If you are running the Quartus II software version 4.0 and later using VNC software, the Quartus II software may terminate unexpectedly whenever you open any file or browse any directory from within the Quartus II software.</p>	<p>Make sure your VNC server software is version 3.3.4 or later.</p>
<p>If you are running the Quartus II software under Red Hat Linux 7.3, you may experience substantial degradation of compilation times if your design files are located on a separate server from the Quartus II software.</p>	<p>Make sure that the operating system kernel is upgraded to the latest available. If you are using a NetApps server, refer to the following document for more information:  <a href="http://www.netapp.com/tech_library/ftp/3183.pdf">www.netapp.com/tech_library/ftp/3183.pdf</a></p>

## Device Family Issues

### Excalibur

Issue	Workaround
<p>You may receive the message “System Build Descriptor File missing parameter programming clock frequency” for System Build Descriptor Files (.sbd) generated in the Quartus II software version 2.0 and earlier, after selecting the <b>Boot from Serial</b> option in the <b>ARM-based Excalibur MegaWizard Plug-In</b>.</p>	<p>Rerun the <b>ARM-based Excalibur MegaWizard Plug-In</b> in the current version of the Quartus II software to regenerate the SBD File and correct the error.</p>
<p>If you are using the Stripe-to-PLD Bridge in Excalibur EPXA10 Devices, your design may not function due to the Stripe-to-PLD Bridge lockup errata if either of the following options is turned on in the Quartus II software:  <b>Remove Redundant Logic Cells</b>  <b>Perform WYSIWYG Primitive Resynthesis</b>                      Please refer to the <i>EPXA10 Device Errata Sheet</i> for details on the device errata.</p>	<p>To avoid bridge lockup, ensure that the <b>Remove Redundant Logic Cells</b> option is turned off for the project.                      If the <b>Perform WYSIWYG Primitive Resynthesis</b> option is turned on for your project, you may receive warnings that the stripe signals were not routed correctly. To eliminate the warnings, re-run the <b>MegaWizard Plug-In Manager</b> in the Quartus II software version 2.2 or later. This procedure will create an additional settings file (<b>alt_exc_stripe.esf</b>) to ensure that the required logic elements are implemented.</p>

### Cyclone, Stratix & Stratix GX

Issue	Workaround
<p>When you use a Routing Constraints File (.rcf) to control fitting after performing Routing Back-Annotation, your timing analysis results may change slightly due to parasitic and other effects. Any change will be very small.</p>	
<p>If you use the SignalProbe feature to observe the signals at an output pin, by routing them to another output pin, the SignalProbe output pin signal will be shown as Unknown (X) in the Quartus II Simulator.</p>	<p>The signal will be correct in actual operation, the error appears only in the Quartus II Simulator.</p>

Issue	Workaround
<p>In the <b>SignalProbe Source to Output Delays</b> table of the Timing Analyzer Report, the following shortcut menu commands are not available although they are available in other similar Timing Analyzer Report tables:</p> <ul style="list-style-type: none"> <li>• <b>List Paths</b></li> <li>• <b>Locate in Chip Editor</b></li> <li>• <b>Locate in Timing Closure Floorplan</b></li> </ul>	<p>You can use other Timing Analyzer Report tables to list and locate the affected paths.</p>

**Stratix and Stratix GX**

Issue	Workaround
<p>If you use the <code>altddio_bidir</code> or <code>alt_dqs</code> megafunction and connect any data port directly to VCC or GND, the Quartus II software version 3.0 SP1 and later will insert an additional logic element in the circuit path.</p>	
<p>The behavior of the 0-degree phase shift setting of the <code>DLL_PHASE_SHIFT</code> parameter of the <code>altdqs</code> megafunction or the <b>DQS Phase Shift</b> logic option with the <code>altddio_bidir</code> megafunction has changed in the Quartus II software version 3.0 SP2. The previous behavior produced an uncharacterized delay that cannot be specified to fall within the specified 500 ps delay difference.</p>	<p>If your design uses this setting and does not work correctly after installing the Quartus II software version 3.0 SP2 or later, you should contact the Altera Applications department for further information.</p>

**Stratix**

Issue	Workaround
<p>Designs compiled for Stratix EP1S40ES devices must be recompiled for the EP1S40 device before programming.</p>	
<p>Stratix PLL simulation models have been enhanced to handle jitter on the input clock. This enhancement has the unintended side effect that functional simulations for LVDS designs using cascaded PLLs may be incorrect by one clock cycle.</p>	<p>Altera recommends that you perform Timing Simulation to display the correct behavior in the Quartus II Simulator or in other EDA Simulators.</p>

**Stratix II**

Issue	Workaround
On Stratix II devices that use a QDRII SRAM memory interface, in some cases the timing of the complementary clocks can lead to incorrect capture of data coming from a QDRII SRAM memory. Quartus II software will report: "Warning Message: I/O atom <name> uses complementary clocks to capture data from double data rate input pin."	Contact Altera Technical Services at <a href="http://mysupport.altera.com">http://mysupport.altera.com</a> for implementation guidelines to ensure correct data captures on QDRII interfaces.
Due to changes in the <code>altlvds_tx</code> and <code>altlvds_rx</code> megafunctions in the Quartus II software version 5.0, user-created timing assignments to the megafunctions are changed. The megafunctions now make most timing assignments automatically.	Check your assignments to make sure that the Quartus II software implemented them correctly.
The Quartus II software version 5.0 does not support programming file generation for some Stratix II devices when M-RAM blocks are used in some memory modes, and if the <code>STRATIXII_MRAM_COMPATIBILITY</code> option is turned off.	For more information about programming file support for Stratix II devices, please refer to the <i>Stratix II FPGA Family Errata Sheet</i> , which is available on the Altera web site.
The Quartus II software version 4.2 and later supports programming file generation for EP2S60 ES devices, but only for designs where the M-RAM memory is not used.	For more information about programming file support for Stratix II devices, please refer to the <i>Stratix II FPGA Family Errata Sheet</i> , which is available on the Altera web site.
The Quartus II software may crash with an internal Error if you try to assign a SignalProbe pin to a register that has been packed into an I/O element with the <b>Auto Register Packing</b> option.	Do not assign SignalProbe pins to packed registers.
Back-annotating some designs targeted to a Stratix II device with the <b>Demote cell assignments to</b> option set to <b>LABs</b> may prevent the design from fitting.	Back-annotate the design with <b>Demote cell assignments to</b> turned off.

**Stratix GX**

<b>Issue</b>	<b>Workaround</b>
The RREFB pin names for EP1SGX10C, EP1SGX25C, EP1SGX25D, and the EP1SGX40F devices changed in the Quartus II software version 5.0. This may affect your PCB layout.	Each RREFB pin must be tied to ground through a resistor. Altera recommends that you not connect multiple RREFB pins through a single resistor to ground.

**Cyclone**

Issue	Workaround
Altera recommends that the frequency of the external clock output of the PLLs be limited to 312 MHz.	
The Cyclone EP1C3T100 device does not support the <b>LVDS</b> I/O standard on any pins.	Use the Cyclone EP1C3T144 device instead. It supports the <b>LVDS</b> I/O standard.
The operating frequency range of the Cyclone PLL has been changed. In the Quartus II software version 3.0 and earlier, the range was 300 MHz to 800 MHz. In version 3.0 Service Pack 1 and later, that range changed to 500 MHz to 1000 MHz because of concerns about jitter at frequencies below 500 MHz. Because of this change, the minimum input frequency is now 15.625 MHz (previously 15 MHz) and the minimum output frequency is also 15.625 MHz (previously 9.38 MHz).	Recompile your design after installing the current version of the Quartus II software.
The PLL lock circuit does not function correctly for PFD (Phase Frequency Detector) frequencies below 200 MHz when the temperature is below -20°C.	If operation at temperatures below -20°C is required, choose a higher input frequency and clock division (N) factor such that the PFD input frequency is higher than 200 MHz.

**Cyclone II**

Issue	Workaround
Turning on the <b>Perform WYSIWYG primitive resynthesis</b> option while using the <code>alt_lvds</code> megafunctions in designs targeting Cyclone II devices causes the Quartus II software to crash with an internal error.	Turn off the <b>Perform WYSIWYG primitive resynthesis</b> option.
Back-annotating some designs targeted to a Cyclone II device with the <b>Demote cell assignments to</b> option set to <b>LABs</b> may prevent the design from fitting.	Back-annotate the design with <b>Demote cell assignments to</b> turned off.

**Cyclone II & Stratix II**

Issue	Workaround
<p>An internal error is encountered during the Partition Merge stage while performing an incremental compilation using the Quartus II incremental compilation for a design containing a PLL used to generate an external clock. The PLL is assigned to a partition and is set to <b>Netlist Type Post-Fit</b>.</p>	<p>Several workaround are available:</p> <ol style="list-style-type: none"> <li>1. Set the partition containing the PLL to <b>Netlist Type Post Synthesis</b>. The contents of the partition containing the PLL must be replaced and preservation of timing in this partition is not possible.</li> <li>2. Restructure your partitions and HDL such that the PLL and the pin for the external clock are in the same partition. Typically, this will be the Top partition. The advantage of this method is that after restructuring your partitions all the features of Incremental Compilation can continue to be used.</li> <li>3. Turn off the <b>Full Incremental Compilation</b> option.</li> </ol>

**HardCopy Stratix**

Issue	Workaround
<p>The pin table shown in the Quartus II online Help for the HC1S40F780 HardCopy Stratix device incorrectly shows pins U12 and U18 as user I/O pins.</p>	<p>These pins are factory test pins and should be connected to GND. Select the <b>EP1S40_HardCopy_Prototype</b> when compiling for this device.</p>

**MAX II**

Issue	Workaround
<p>The Usercode value shown in the Assembler section of the Compilation Report for MAX II designs is not correct.</p>	<p>Use the Usercode value shown in the Programmer window, it is the correct value.</p>
<p>When the <b>Perform WYSIWYG primitive resynthesis</b> option is turned on for a MAX II design that has been synthesized with the Synplify software version 8.0, and the design has a bidirectional pin that acts as an input pin (i.e., the output enable is GND), then the compiler will give an error stating that the corresponding WYSIWYG primitive has a missing connection to the DATAIN input port.</p>	<p>Either hand-edit the Verilog Quartus Mapping File (<b>.vqm</b>) output from the Synplify software to connect the DATAIN port, or change your HDL to make the bidirectional pin into an input pin.</p>

**HardCopy II**

Issue	Workaround
You may receive Revision Comparison warnings about differing EDA tool settings if your project directory contains a Quartus II Defaults File (.qdf).	Delete the Quartus II Defaults File from your project directory.
The HardCopy II Revision Comparison table may show certain blocks as being only in the current revision, and other blocks with slightly different names in the companion revision only.	Be sure there are no assignments to those blocks and ignore the warnings.
If you have selected multiple FPGAs for vertical migration when migrating to HardCopy II, the Comparison table will show pin-out differences that prevent migration.	Do not choose vertical migration for the companion device.
The HardCopy II Revision Comparison table erroneously reports differences in DQS Bus widths between the HardCopy II device and the Stratix II companion device.	It is acceptable for DQS Bus widths to not match across HardCopy II and Stratix II companion revisions. The difference can be ignored.

**Design Flow Issues****Verification**

Issue	Workaround
If you are using IP Toolbench to generate simulation models for Altera IP Megacore® functions, you will get an error if support for the Stratix device family is not installed.	Install support for the Stratix device family.
Incremental routing may fail for nodes assigned to the SignalTap II Logic Analyzer if you have turned on any of the Physical Synthesis Fitter optimizations, such as <b>Perform physical synthesis for combinational logic</b> or <b>Perform register duplication</b> or <b>Perform register retiming</b> .	

**Integrated Synthesis (VHDL and Verilog HDL)**

Issue	Workaround
<p>When you are using Quartus II integrated synthesis with any family, you may receive a warning similar to the following example:            “Warning: Converting TRI node "&lt;name&gt;" that feeds logic to a wire”</p> <p>If you receive this warning, there is a chance that synthesis will generate incorrect logic. This happens only when there is a tri-state that feeds internal logic only (that is, no output or bidir pins), and the tri-stated data is GND. In this case, the tri-state will be incorrectly replaced by VCC.</p>	<p>Remove the internal tri-states for which this warning was given from their source code.</p>
<p>The Quartus II software version 4.0 and later may give the message “Error: Duplicate entity &lt;name&gt; found in file &lt;filename1&gt; colliding with the one found in file &lt;filename2&gt;,” for a project that compiled successfully with Quartus II 2.2 or earlier.</p>	<p>The Quartus II software gives an error message when it finds two or more entities with the same name. To avoid this error in the future, remove the duplicate entity or entities. If you cannot remove the duplicate entity, you can direct the Quartus II software to ignore the duplication by adding  <pre>set_global_assignment -name IGNORE_DUPLICATE_DESIGN_ENTITY ON</pre>           to your Quartus II Settings File (.qsf). Altera recommends that you avoid using this workaround if possible.</p>

**Verilog HDL Integrated Synthesis**

Issue	Workaround
<p>The Quartus II integrated synthesis may incorrectly synthesize registered logic inside an Always Construct whose Event Control creates a clock signal based off a posedge/negedge of an indexed identifier, e.g. "posedge clk[0]". Incorrect synthesis occurs when the clock signal is the LSB of the identifier and the Always Construct references the identifier inside the Always Construct.</p>	<p>Assign the indexed ID to a temporary variable, then use the temporary variable in the Event Control.</p>

Issue	Workaround
Verilog-2001 mode is enabled by default. This mode can cause some issues with Verilog-1995 designs, most commonly due to new reserved words in Verilog-2001 such as <code>config</code> .	Do not use Verilog-2001 reserved words as identifiers or select <b>Verilog-1995</b> on the <b>Verilog HDL Input</b> page under <b>Analysis &amp; Synthesis Settings</b> of the <b>Settings</b> dialog box.
Verilog HDL escaped names that look like vectors can cause problems in the Quartus II software. For example, if you have a single-bit component port named <code>\my_vector_port [3:0]</code> , the Quartus II software versions 2.1 and later will treat it as an array port.	You should avoid using escaped port names in the Quartus II software version 2.1 and later.
Some designs that compiled successfully in the Quartus II software version 3.0 may fail with the error message “Index Z cannot be outside range (x to y) of array <name>.”	The Quartus II software version 4.0 and later does not allow out-of-bounds array accesses. The Quartus II software version 3.0 would return “don't care.” You must rewrite your design to keep array accesses within the valid range of the array.

**SignalTap II**

Issue	Workaround
If you change the Incremental Compilation mode of a SignalTap II Logic Analyzer, you may receive an error message that says “Compile the project to continue” immediately after completing a successful compilation.	The message is erroneous and can be safely ignored. <i>Or:</i> Close and reopen the SignalTap II (.stp) File.

**Quartus II Incremental Compilation**

Issue	Workaround
You cannot turn on the <code>HARD_POST_FIT</code> option if you are using the Design Space Explorer in distributed mode. The option is ignored.	Turn off the <code>HARD_POST_FIT</code> option, or do not use DSE in distributed mode.
The Quartus II software may crash with an internal error if, after you have performed a successful full compilation with incremental compilation turned on, you try to run a timing simulation after an unsuccessful attempt to generate a functional simulation netlist.	Always perform a full compilation before running timing simulation, or, always ensure that the Fitter has run successfully before running timing simulation.

<p>The Quartus II software may crash with an internal error if, after you have performed a successful full compilation and timing simulation with incremental compilation turned on, you run Partition Merge and then try to perform timing simulation again.</p>	<p>Always perform a full compilation before running timing simulation, or, always ensure that the Fitter has run successfully before running timing simulation.</p>
<p>If you change the top-level entity without changing the revision in a subsequent compilation of an incremental compilation (that is, not the initial compilation), the Quartus II software will “hang” and stop responding.</p>	<p>Use a different revision to change the top-level entity name.</p>
<p>An internal error is encountered during the Partition Merge stage while performing an incremental compilation on a design containing a PLL that is used to generate an external clock. The PLL is assigned to a partition and is set to <b>Netlist Type Post-Fit</b>.</p>	<p>Several workarounds are available:</p> <ol style="list-style-type: none"> <li>1. Set the partition containing the PLL to <b>Netlist Type Post Synthesis</b>. The contents of the partition containing the PLL must be replaced and preservation of timing in this partition is possible.</li> <li>2. Restructure your partitions and HDL such that the PLL and the pin for the external clock are in the same partition. Typically, this will be the Top partition. The advantage of this method is that after restructuring your partitions all the features of incremental compilation can continue to be used.</li> <li>3. Turn off <b>Full incremental compilation</b>.</li> </ol>

## SOPC Builder Issues

Issue	Workaround
<p>If you open more than one SOPC Builder project simultaneously, you will receive an error message similar to the following example: “bad or corrupt 'class.ptf' file.”</p>	<p>Open the SOPC Builder only when no other SOPC Builder project is already open.</p>
<p>SOPC Builder fails to open on UNIX when invoked from the <b>MegaWizard Plug-In Manager</b>.</p>	<p>Open SOPC Builder by choosing <b>SOPC Builder</b> from the Quartus II Tools menu.</p>
<p>Updated components not visible in SOPC Builder.</p>	<p>After clicking <b>Check</b>, refresh the <b>Component List</b> by clicking on another <b>Component</b> tab or by restarting SOPC Builder.</p>

Issue	Workaround
System generation fails to complete when a 0-address-width master is connected to a 0-address-width slave. An example case is when the Avalon DMA masters only a 0-address-width slave. Further, if the Avalon DMA masters a 0-address-width slave and a slave with a non-zero address width, the 0-address-width slave will not be accessible.	User-created masters should provide a non-zero width address even if they master only 0-address-width slaves. User-created zero-address-width slaves should provide a small address (which can be ignored within the peripheral).
If you have multiple versions of the Quartus II software installed, installing a new SOPC Builder component updates the search paths of all the versions of the Quartus II software to point to the new version.	Modify the SOPC Builder search path. In SOPC Builder, click <b>SOPC Builder Setup</b> on the File menu. Then modify the <b>Component/Kit Library Search Path</b> to point to the desired kit version
You may see random display errors, such as streaks and blotches, in the SOPC Builder GUI.	Lower the <b>Hardware Acceleration</b> setting on the <b>Troubleshooting</b> tab of the <b>Advanced Display Settings</b> dialog box in your <b>Display Settings</b> control panel. There is a known incompatibility between the current Java Runtime Environment (JRE) and certain laptop graphics drivers.
The Component Editor in SOPC Builder does not allow you to specify that signals be shared with other peripherals. For Avalon tri-state slave interfaces, the data, address, and byte enable signals are automatically shared with other peripherals connected to the same tri-state interface. For example, when multiple Avalon tri-state slave peripherals are connected to the same Avalon tri-state bridge, the data, address, and byte enable signals are shared by all the peripherals.	Shared pins are handled automatically by the new SOPC Builder pin-mapper, which is available for all Altera-supported boards. For external boards, use the <b>Interface to User Logic</b> wizard to create the component. Pin mapper support for all PCBs will be available in a future version of SOPC Builder.
When creating a component with the SOPC Builder Component Editor, you must not choose a component name that exactly matches the HDL file name or the top-level module name. If the names are the same, SOPC Builder will generate an error during system generation. This problem will be fixed in a future version of SOPC Builder.	Using the SOPC Builder Component Editor, rename the component to a different name. In the SOPC Builder table of active components, add the newly-named component to your system, and delete the old component.
If the Quartus II software is installed in a directory that has space characters in its name, the SOPC Builder software will not run.	Install the Quartus II software in a directory that does not have space characters in the path.

Issue	Workaround
<p>When adding an Excalibur Stripe component in conjunction with Avalon peripherals, you may encounter SOPC Builder errors indicating that too many masters are present.</p>	<p>If the master-connection patch-panel is not visible, click <b>Show Master Connections</b> on the View menu. Then click the master/slave intersection indicated by the error message. This will remove the connection. Click again to restore the connection and the error will not reappear.</p>
<p>Designs targeting Excalibur devices that use Boot From Flash mode may not operate when downloaded to the target board if the Quartus II Software Builder or SOPC Builder Excalibur-build script was used to generate the flash programming file.</p>	<p>The Excalibur boot loader in the Quartus II software version 3.0 and later does not function correctly if the Quartus II Software Builder is used to generate the flash programming file. This is because the compression option that is used with the <b>makeprogfile</b> utility during the software build process does not work with this version of the boot loader. To work around this issue, do not use the Software Builder to generate a programming file, but instead use the <b>makeprogfile</b> utility at the command line with the <b>-nc</b> (no compression) option. If you are using the SOPC Builder Excalibur-build script, you must edit the script located in the <code>&lt;XA dev kit install directory&gt;\bin</code> folder. Modify line 1034 of this script to remove the <b>-nc</b> option. For example, line 1034 should be changed as shown in this example.</p> <pre>\$command = "makeprogfile -nc -b \${fileBase}_bootdata.o \$SBD \$SBI \${fileBase}.hex" ;</pre> <p>You must recompile your software project for this change to take effect.</p>
<p>The SOPC Builder and Nios Software Development Kit shell may “hang” and become unresponsive when run while the Frisk antivirus software is running.</p>	<p>Turn off the Dynamic Virus Checking feature of the Frisk software before running SOPC Builder or the Nios SDK shell.</p>

## EDA Integration Issues

Issue	Workaround
<p>The current version of the Quartus II software allows you to select the Synplicity Amplify software as a physical optimization tool. However, this setting is for an automated mode called ATOPS, which is currently not supported by the Amplify software.</p>	<p>Contact Synplicity for the support schedule for the Amplify software ATOPS mode.</p>
<p>Support has been added for generation of IBIS Output Files (.ibs) for EPCS1 and EPCS4 Serial Configuration Devices.</p>	<p>The IBIS Output File will be generated in the <code>\&lt;project name&gt;\board\ibis</code> directory after compilation when the design is targeted to a Cyclone device and Active Serial configuration scheme using EPCS1 or EPCS4 devices is chosen.</p>
<p>NativeLink support does not work with versions of Mentor Graphics Precision RTL Synthesis Software earlier than version 2003b due to a change in the Precision project interface.</p>	

## Simulation Model Changes

### altera\_mf Models

#### Memory Models

Model	Change
altsyncram	<ul style="list-style-type: none"> <li>• When the <code>byteenable</code> signal is unknown 'X,' the byte written into the RAM is corrupted with value 'X.'</li> <li>• Added parameter <code>power_up_uninitialize</code>. Contents of RAM power up to 'X' if set to ON. The default is OFF.</li> <li>• Added parameter "<code>implement_in_les</code>". RAM will power up to '0' if the value is ON. The default is OFF.</li> <li>• Added support for HardCopy II.</li> </ul>

**I/O Models**

Model	Change
altdio_bidir altdio_out	<ul style="list-style-type: none"> <li>Added parameter <code>invert_output</code> to allow output inversion for Cyclone II device family.</li> </ul>
altlvds_tx altlvds_rx	<ul style="list-style-type: none"> <li>Added parameter <code>implement_in_les</code> to enable serdes support in logic cells for Stratix, Stratix GX, Stratix II, and HardCopyII families.</li> </ul>
altpll	<ul style="list-style-type: none"> <li>Fixed Stratix II behavior to ensure <code>scandone</code> signal is asserted only after PLL reprogramming is completed.</li> <li>Added parameters to control port connectivity for all PLL input and output ports.</li> <li>Fixed Stratix II PLL to revert counter phase taps to initial configuration values when PLL is reset after dynamic reconfiguration.</li> </ul>

**Megafunction Models**

Model	Change
altufm_i2c	<ul style="list-style-type: none"> <li>Added <code>page-write</code> (choice of 8 bytes, 16 bytes or 32 bytes)</li> <li>Added 8K memory size option</li> </ul>
lpm_divide	<ul style="list-style-type: none"> <li><code>lpm_divide</code> produced an output of '0' (instead of 'X') when the asynchronous clear signal was asserted.</li> </ul>

**Notes:**

- The ModelSim software gives the following warning when **altera\_mf** or **220models** megafunction models are compiled with the -87 option:

```
*** Warning (vcom-1148) Condition in IF GENERATE must
be static
```

You can safely ignore this warning because under the 1987 rules, the constant is not considered to be static because of the initialization from the function call.

- RAM Megafunction models only support HEX format for all other EDA simulators. Manually convert Memory Initialization File (**.mif**) format to a Hexadecimal (Intel-Format) File (**.hex**) first in the Quartus II software.

## Power Model Changes

### PowerPlay Power Analyzer

The following power models have been updated in the PowerPlay Power Analyzer. An upcoming Early Power Estimation Spreadsheet (EPE) will have the same update published on the Altera web site.

- Updated Clock Tree Power Model for the Stratix device family
- Updated RAM Power Model for the following families:
  - Stratix
  - Cyclone
  - Stratix GX
- Updated LVDS Power model for the following families:
  - Stratix
  - Stratix GX
- Updated the GXB Power model for the Stratix GX device family

### PowerPlay Early Power Estimation

- Entry through WEB-based Early Power Estimation is no longer supported.
- HardCopy APEX Web-based Early Power Estimation will be removed.
- HardCopy Stratix Web-based Early Power Estimation will be replaced with the standard Early Power Estimation Spreadsheet (EPE).

## Software Issues Resolved

This Quartus II software Service Pack corrects issues in the following areas:

- Fixed a problem which caused the total slack and clock skew values specified in a list paths operation do not match those in the Timing Analysis report.
- Fixed a problem in which a file necessary for programming the EP2S60 was omitted from the installation.
- Fixed a problem in which the Quartus II Programmer stops with “Error 1” when programming a JTAG Indirect Configuration file (.jic) into a EPCS64 device.
- Fixed a bug that caused the Quartus II software to crash with an internal error when an inversion on a Stratix II logic cell input was absorbed without inserting an inverter LCELL.
- Fixed a problem that caused the Quartus II software to crash with an internal error when the DQSBUSOUT port of an I/O cell is used under some circumstances.
- Fixed a problem in which the PLL clock output was non-functional at certain phase shift settings, on Cyclone II devices.
- Fixed a problem in which designs with RAM failed to fit if there were certain constraints.
- Fixed a problem with Cyclone II M4K RAM block Port A writes by adding a parameter to the `altsyncram` megafunction.
- Added full programming support for Cyclone II EP2C5, EP2C8, and EP2C50 devices.
- Fixes a problem in which the Quartus II Fitter fails during physical synthesis with the following message: `Can't place 2 nodes into a single ALM`.
- Fixes a problem with the Stratix II Fast PLL simulation model, which doesn't handle the phase shift on port enable0 correctly.
- Fixes a bug which causes the `altlvds` megafunction to not meet timing requirements in Cyclone devices.
- Fixed a bug that causes the I/O register enable and clock enable signals to be incorrectly inverted when fed by the same clock signal.
- Fixes a bug that causes the Quartus II software to crash with an internal error when copying a netlist with a module that contains a top-level multidimensional variable.
- Fixes a bug that caused the Quartus II software to crash with an internal error when placing carry chain cells in Stratix II devices.
- Fixed a problem with programming Stratix II devices with EPCS64 in Active or Passive Serial Mode.
- Fixed a problem with dual-clock FIFOs in Stratix II and Cyclone II devices.

- Fixed a problem with Quartus II-generated Standard Delay Output file (.sdo) for gate-level simulation in ModelSim.
- Fixed a problem with redundant register names in netlist.
- Fixed a problem that caused the Quartus II software to crash with an internal error when using Block Design Files (.bdf).
- Fixed a problem with the EDA Netlist Writer in which it did not write out the correct parameter to support delay simulation in ModelSim.
- Fixed a bug in the Verilog HDL simulation model for timing simulation of the altlvds megafunction in Stratix II devices.
- Fixed a problem in which the properties of a wire-LUT were set improperly during physical synthesis.
- Fixes a bug that causes the Quartus II integrated synthesis to incorrectly report that a state machine has a complex reset state.
- Fixes a problem in which a file was missing from the 64-bit Linux installation.

## Service Requests Closed in This Service Pack

The following table lists the Service Requests that were closed for this Service Pack.

10503942	10504878	10505603	10504756
10505598	10507966	10508976	10509808
10507986	10464114	10510752	10512843
10509163	10512436	10512823	10507326
10507326	10514452	10514452	10514173
10514818	10515369	10513074	10513470
10513703			

## Latest Known Quartus II Software Issues

For known software issues after publication of this version of the *Quartus II Software Release Notes*, please look for information in the **Quartus II Latest Known Issues** section of the Altera Support Find Answers Database at the following URL:

[http://answers.altera.com/altera/index.jsp?Topics/Support/Solutions/Known Issues/Software/Quartus II](http://answers.altera.com/altera/index.jsp?Topics/Support/Solutions/Known%20Issues/Software/Quartus%20II)

## Revision History

Revision	Description
1.0	Initial Release

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