



Quartus II Software Release Notes

March 2006

Quartus II version 5.1 Service Pack 2

This document provides late-breaking information about the following areas of this version of the Altera® Quartus® II software. For information about memory, disk space, and system requirements, refer to the **readme.txt** file in your `\altera\quartus<version number>` directory.

New Features & Enhancements	2
Device Support & Pin-Out Status	2
Full Device Support.....	2
Advance Device Support.....	2
Initial Information Support.....	2
Changes in Device Support	3
Timing Models	4
Preliminary Timing Models	4
Final Timing Models	5
Changes to Timing Models	6
Power Models.....	7
EDA Interface Information	8
Changes to Software Behavior	9
Known Issues & Workarounds.....	10
General Quartus II Software Issues	10
Platform-Specific Issues.....	19
Device Family Issues.....	25
Design Flow Issues.....	33
Logic Analyzer Interface.....	36
SOPC Builder Issues	36
EDA Integration Issues	38
Simulation Model Changes	39
Software Issues Resolved.....	40
Latest Known Quartus II Software Issues	41
Revision History.....	41

New Features & Enhancements

The Quartus II software version 5.1 Service Pack 2 includes the following new features and enhancements:

- Software and timing model changes for Cyclone II devices, described below
- The new features and enhancements provided in Quartus II software version 5.1 Service Pack 1 are incorporated in Service Pack 2. For details, see the Quartus II software version 5.1 Service Pack 1 Release Notes.

Device Support & Pin-Out Status

This section contains information about the status of support in the Quartus II software for the listed devices.

Full Device Support

Full compilation, simulation, timing analysis, and programming support is now available for the following new devices and device packages:

Devices with Full Support

Device Family	Devices
Stratix II	EP2S90F780

Advance Device Support

Compilation, simulation, and timing analysis support is provided for the following devices that will be released in the near future. Although the Compiler generates pin-out information for these devices, it does not generate programming files for them in this release.

Devices with Advance Support

Device Family	Devices
Stratix II GX	EP2SGX90EF1152
Stratix II	EP2S90H484

Initial Information Support

Compilation, simulation, and timing analysis support is provided for the following devices that will be released in the near future. Programming files and pin-out information, however, are not generated for these devices in this release.

Devices with Initial Information Support

Device Family	Devices
None	

Changes in Device Support

The changes in device support provided in Quartus II software version 5.1 Service Pack 1 are incorporated in Service Pack 2. For details, see the Quartus II software version 5.1 Service Pack 1 Release Notes.

Timing Models

This section contains a summary of timing model status in the current version of the Quartus II software.

Preliminary Timing Models

The following table shows the devices with preliminary timing models in the current version of the Quartus II software:

Devices with Preliminary Timing Models

Device Family	Device
HardCopy II	HC210
	HC220
	HC230
	HC240
Cyclone II	EP2C5*
	EP2C50*

* These devices had significant changes to their timing models in the version 5.1 release of the Quartus II software. You should run the Timing Analyzer on your design to see any effects of these changes.

Final Timing Models

The following table lists the devices with final timing models that are available in the current version of the Quartus II software:

Devices with Final Timing Models

Device Family	Device	Timing Models Final in Quartus II Version Number
Cyclone	EP1C3	3.0 SP1
	EP1C4	4.0
	EP1C6	3.0
	EP1C12	3.0 SP1
	EP1C20	3.0
Cyclone II	EP2C8	5.1 SP2
	EP2C20	5.1 SP2
	EP2C35	5.1 SP2
	EP2C70	5.1 SP2
FLEX 10K [®]	All	3.0
FLEX 10KA	All	3.0
MAX [®] 7000S	All	3.0
MAX II	EPM240	5.0
	EPM1270	5.0
	EPM570	5.0 SP1
	EPM2240	5.0 SP1
Stratix	EP1S10	4.1
	EP1S20	4.1
	EP1S25	4.1
	EP1S30	4.1
	EP1S40	4.1
	EP1S60	4.1
	EP1S80	4.1
Stratix II	EP2S15*	5.0 SP1
	EP2S30*	5.0
	EP2S60*	5.0
	EP2S90*	5.0 SP1
	EP2S130*	5.0 SP1
	EP2S180	5.1
Stratix GX	EP1SGX10	4.1
	EP1SGX25	4.1
	EP1SGX40	4.1

* The final timing models were updated in Version 5.1, for details see the *Quartus II Software Version 5.1 Release Notes* available on the Altera website.

The current version of the Quartus II software also includes final timing models for the ACEX[®] 1K, APEX[®] 20K, APEX 20KE, APEX 20KC, APEX II, Excalibur[™], FLEX[®] 6000, and FLEX 10KE device families. Timing models for these device families became final in versions earlier than version 3.0.

Changes to Timing Models

The changes to timing models provided in Quartus II software version 5.1 Service Pack 1 are incorporated in Service Pack 2. For details, see the Quartus II software version 5.1 Service Pack 1 Release Notes.

The following changes were made to the Quartus II timing models in this release.

Cyclone II Timing Model Changes

The package trace delays for EP2C8, EP2C20, EP2C35, and EP2C70 devices are updated. This change affects the delay of I/O pins. The magnitude of the change is less than 100ps.

The PLL compensation settings for EP2C20 devices are updated. This change improves the accuracy of PLL phase compensation and is less than 1ns in magnitude.

The timing model for the M4K memory block is updated. In addition, the programmable settings used to configure the M4K block are updated for some modes. The performance of the M4K block depends on the device speed grade, the memory mode, the clock signals used by the memory, and whether the design is recompiled to incorporate the updated programmable settings.

The effect of the updated timing model and settings for the M4K block depends on the device speed grade used:

Speed Grade	Effect
C8 and I8	None
C7	M4K speed affected for Single Port and True Dual Port modes, some or all speed may be recovered if design is recompiled
C6	M4K speed affected for all RAM modes, some or all speed may be recovered if design is recompiled

Altera recommends that you recompile all Cyclone II designs for C6 speed grade that use M4K memory blocks and that you recompile all Cyclone II designs for C7 speed grade that use M4K memory blocks in Single Port or True Dual Port mode.

Power Models

This section contains a summary of power model status for recent devices in the current version of the Quartus II software.

Device Family	Power Model Status
Stratix II	Preliminary
Cyclone II	Preliminary
MAX II	Final – 5.0 SP1
Stratix	Final – 5.1
Stratix GX	Final – 5.1
Cyclone	Final – 5.1
MAX 3000A	Final – 5.1
MAX 7000AE	Final – 5.1
MAX 7000B	Final – 5.1

EDA Interface Information

The current version of the Quartus II software supports the following EDA tools.

Supported EDA Tools

Synthesis Tools	Version	NativeLink® support
Mentor Graphics® LeonardoSpectrum	2005a Update 1	✓
Synopsys Design Compiler	2004.12-SP4	
Synopsys Design Compiler FPGA	2005.09	
Synopsys FPGA Compiler II	3.8	✓
Mentor Graphics Precision RTL Synthesis	2005b	✓
Synplicity Synplify and Synplify Pro	8.2.2a or later	✓
Magma Design Automation PALACE™	2.4	✓
Verification Tools	Version	NativeLink support
Cadence NC-Verilog	5.4 s011	✓
Cadence NC-VHDL	5.4 s011	✓
Cadence Verilog-XL (Windows)	3.3	
Cadence Verilog-XL (UNIX)	5.4	
Mentor Graphics ModelSim®	6.0e	✓
Mentor Graphics ModelSim-Altera	6.0e	✓
Mentor Graphics Tau	ISD 2004 SPac3	
Mentor Graphics IO Designer	2004 SPac2	
Synopsys PrimeTime	2005.06	✓
Synopsys VCS / VCS MX	7.2	✓
Synopsys VSS	2002.06	
Synopsys Formality	2005.09	
Cadence Encounter Conformal	5.1	

Changes to Software Behavior

The changes to software behavior provided in Quartus II software version 5.1 Service Pack 1 are incorporated in Service Pack 2. For details, see the Quartus II software version 5.1 Service Pack 1 Release Notes.

Known Issues & Workarounds

General Quartus II Software Issues

Issue	Workaround
<p>There is a possibility of functional failures for designs with ROMs inferred by Quartus II Integrated Synthesis or that contain RAMs with an initial contents file. This is an issue with Quartus II 5.1, 5.1SP1 and 5.1SP2. This is not an issue with Quartus II versions 5.0 and earlier. A functional failure may occur in designs with either of the following characteristics:</p> <p>The design contains inferred ROM. A design with inferred ROM has the following Information messages in the Analysis & Synthesis Messages :</p> <pre>Info: Inferred <number> megafunctions from design logic Info: Inferred altsyncram megafunction (OPERATION_MODE=ROM, ...) from the following design logic: <logic name></pre> <p>The path for the memory initialization file of any RAM or ROM is specified through User Library paths. RAM or ROM instantiations that specify absolute paths to memory initialization files, or with memory initialization files in the project directory, are not affected.</p> <p>The issue occurs when changes to RAM and ROM memory initialization files are not recognized properly in a subsequent compilation. This can cause the design to fail functionally in simulation or hardware after a successful compilation.</p>	<p>Refer to the Solution at the following URL for further information and to download the required patch. Contact Altera Technical Services if you have further questions.</p> <p>www.altera.com/support/kdb/solutions/rd03062006_72.html</p>

Issue	Workaround
<p>The Quartus II 5.1 SP1 Programmer incorrectly programs flash devices through PFL when the flash data bus interface is 8 bits wide (i.e. byte addressing mode). The programming of flash devices when the flash data bus interface is 16 bits wide (i.e. word addressing mode) is unaffected.</p>	<p>Contact your Altera technical services representative for a software patch. The issue will be fixed in a future version of the Quartus II software.</p>
<p>Changing global levels on input ports with the Resource Property Editor may cause the Quartus II software to crash in the following scenarios:</p> <ul style="list-style-type: none"> • Assigning global levels to ports that do not support global levels other than Off or Don't Care (for example, CIN). • Assigning a global level that is not supported by the current device to an input port. • Assigning a global level that is inaccessible due to location constraints on the CLKBUF and the destination input port. 	<p>Do not assign a global level to signals meeting any of these criteria.</p>
<p>Opening the Paths dialog box by selecting a critical path in the Timing Closure Floorplan and then right-clicking and selecting Properties causes the destination node in the Paths dialog box to be populated with the source node name.</p>	<p>Double-click a critical path in the Timing Closure Floorplan instead of using the shortcut menu.</p>
<p>Restoring an I/O cell that was deleted with the Chip Editor may not restore all the settings associated with that I/O cell.</p>	
<p>The Quartus II software may crash with an internal error if you turn on Full Incremental Compilation and you turn on Allow In-System Memory Content Editor to capture and update content independently of the system clock in a RAM- or ROM-related megafunction. Or if you instantiated the RAM- or ROM-related megafunction directly and added "ENABLE_RUNTIME_MOD=YES" as part of the LPM_HINT parameter value.</p>	<p>Disable the feature or change the parameter value to "ENABLE_RUNTIME_MOD=NO". If you need to use the feature, turn off Incremental Compilation.</p>

Issue	Workaround
When you are using the Chip Editor to delete the connections in carry chains, the destination node must be in a legal location for the carry chain. If this is not the case you will not be able to undo the operation or any prior operations.	Perform the following steps: 1. Delete the Remove-Chain command in the Change Manager. 2. Move the node back to its legal position. 3. Recreate the chain in the Resource Property editor. 4. Move the node to the desired position.
The Quartus II Fitter may fail with an error if the path to the Quartus II installation directory is longer than 96 characters.	Install in a directory with a path with fewer than 96 characters in its length.
If your design for Stratix, Stratix GX, Stratix II, Stratix II GX, Cyclone, Cyclone II, or MAX II device families uses virtual pins, the number of registers shown in the Synthesis and Fitter reports is under reported by exactly the number of virtual pins used in the design.	Manually add the number of virtual pins to the reported number of registers.
The Quartus II archive feature does not correctly archive files that have duplicate filenames, even when they are in different directories. This failure can cause compilation failures when you are using the distributed processing feature of Design Space Explorer (DSE).	Make all design file names unique.
If you remove an input signal connection or an output signal connection from a pin with the Chip Editor, and then use the Undo command, it is possible that that the pin's delay chain settings may revert to their default settings.	Use the Resource Property Editor to reset the delay chain settings for the affected pin.
If you have specified the Mozilla Firefox browser as your default browser, or specified it on the Internet Connectivity page of the Options dialog box, you may not be able to open the HDL Tutorial PDF files from the Help menu.	Use the Adobe Acrobat reader to browse to and open the PDF files.
If your design contains illegal pin assignments, and you open the Resources window in the Pin Planner, the Quartus II software may crash.	Remove any illegal pin location assignments before opening the Resources window.

Issue	Workaround
<p>When you are listing paths from a Timing Analyzer table in the Report Window and the row number is ≥ 65536, the results displayed in the Messages window will be for the wrong nodes.</p>	<p>Use the <code>list_path</code> Tcl command shown in the following example to obtain the correct results.</p> <pre>list_path -npaths 1 -from <From> -to <To> <other options></pre> <p>Where the <code><From></code> and <code><To></code> correspond to the values in the "From" and "To" columns in the Report Window table.</p> <p>The <code><other options></code> depend on the type of table. For example, use <code>-clock_setup</code> for Clock Setup tables, and so on. See the help on the <code>list_path</code> command for more information.</p>
<p>If you make a single-point CUT=ON assignment to a node, and then override it with a point-to-point CUT=OFF assignment on a specific path, the OFF assignment will not be honored.</p>	
<p>Under certain circumstances the Design Assistant reports Critical Warnings (that locate to the <code>altlvds_rx</code> or <code>dcfifo</code> megafunction) for your project, which uses the <code>altvds_rx</code> or <code>dcfifo</code> megafunction or an IP core that uses the <code>altvds_rx</code> or <code>dcfifo</code> megafunction.</p>	<p>These warnings can be safely ignored; no action is necessary.</p>
<p>You may receive a "License not found..." error if the path to the license file contains non-ASCII characters.</p>	<p>Change or remove any non-ASCII characters from the license file path.</p>
<p>During a SignalProbe™ compilation, you might receive warning message(s) similar to the following example:</p> <p>"Routing constraints for signal <code><signal_name></code> seem to be causing unresolvable routing congestion. The constraints for the signal were removed."</p>	<p>The Compiler issues these warnings when it must modify the routing of some signal nets from the prior compilation in order to complete the routing of the SignalProbe signals. Be aware that the timing of the signals listed in the warning may have changed due to the addition of SignalProbe signals.</p>

Issue	Workaround
If you modify a resource (node or connection) used by a SignalProbe pin using the Resource Property Editor feature of the Chip Editor and then perform another SignalProbe compilation, the compilation will fail and the Quartus II software may crash with an internal error.	Do not use the Chip Editor features (Resource Property Editor, Chip Editor, or Engineering Change Manager) to modify properties of SignalProbe pins.
There is no distinction between output ports and bidirectional ports in AHDL Function Prototypes; instead, all ports listed after the RETURNS keyword are treated as output ports. As a result, if you specify a bidirectional port in a logic function's Function Prototype Statement and do not connect the port to a top-level bidirectional pin or to other logic in the design where you instantiate the logic function, an error can occur.	Connect the port to a top-level bidirectional pin or to other logic in the design.
Context-sensitive Help is not available for some items in the Quartus II software.	To locate Help on those items, click Search on the Help menu, and type the name of the item.
The Timing Analyzer does not recognize non-PLL clock signals when using any PLL megafunction.	Make clock settings assignments to all non-PLL clocks.
The Waveform Editor does not allow you to create a bus with nodes that are nonconsecutive members of a bus.	Create buses only with nodes that are consecutive members of a bus. Or, use the Group command on the Edit menu to create groups of arbitrary nodes.
If you are using the <code>altcam</code> , <code>altclklock</code> , <code>altlvds_rx</code> , or <code>altlvds_tx</code> megafunctions, the equations shown in the Equations Section of the Compilation Report are not complete.	To view the complete equations for any of these megafunctions, use the Equations window of the Timing Closure Floorplan.
The Quartus II software does not support design file names with more than one extension. For example, you cannot use the file name file.eda.edif .	Use design file names with only one extension.
If you install the Quartus II software for PCs on a UNIX server that exports shares with the Samba software version 1.9.18p10, you may experience problems accessing project files that are also on the network.	Altera recommends using version 1.9.16p11 or 2.0 of the Samba software.

Issue	Workaround
If you make assignments to reserve pins as a group or with group notation (debug [7..0]), the Quartus II software does not correctly generate simulation output files, and you receive a warning message saying “Unsupported data type in the top-level module.”	Reserve the pins using single-name notation (for example, debug [7], debug [6], and so on).
Do not change the file permissions (such as changing “read-only” to “read and write”) of Quartus II Settings File (.qsf) and Quartus II Project File (.qpf) while a Quartus II project is open.	Close the Quartus II project before making changes to the file permissions.
Node names containing numbers greater than 2 ³¹ -1 (2147483647) will cause an Internal Error in the Quartus II software.	Do not use node names containing large numbers.
Occasionally the Programmer does not allow you to use a MAX 7000AE Programmer Output File (.pof) with a MAX 7000AE device. This error sometimes occurs after a compatible MAX 7000B device is used with the MAX 7000AE POF.	Do not switch between compatible MAX 7000B and MAX 7000AE devices when a MAX 7000AE POF is loaded, or reload the MAX 7000AE POF.
Routing back-annotation may fail if the back-annotated locations do not match the location assignments in the Quartus II Settings File (.qsf) or if the location assignments are missing. This problem can occur if you change devices, or if you remove some location assignments by using the Assignment Editor on the Assignments menu or by manually editing the Quartus II Settings File.	If you experience a “no fit” or an Internal Error while using routing back-annotation, delete the Routing Constraints File (.rcf) and back-annotate the design again after a successful compilation.
If you receive an error message saying “System resources low...” or if the user interface is slow in responding and there is a lot of disk activity when you are not compiling a design, your system may be running out of free memory.	You can recover system memory by clearing messages from the Messages window. To clear messages from the Messages window, right-click anywhere in the Messages window and click Clear Messages from Window on the shortcut menu. Additional memory can be recovered by closing the Timing Closure Floorplan.
Occasionally, the Quartus II software may crash or hang with no error message immediately upon opening a project.	Delete the Quartus II Workspace File (.qws) <project name>.qws from the project directory. If the problem persists, delete the \<project directory>\db directory.

Issue	Workaround
When you are setting phase shift and duty cycle values for clock signals using the <code>altpll</code> megafunction, some combinations of settings may result in values that cannot be synthesized exactly. Under certain circumstances, the Quartus II software attempts to synthesize the phase shift parameter before the duty cycle parameter.	You should first select values for the parameter (phase shift or duty cycle) that is most important for your design.
During compilation or simulation, the Quartus II software may “hang” and not proceed to the next module if a menu or modal dialog box is open at the time the current module finishes running.	Close any open menus or modal dialog boxes before the compilation or simulation reaches the next stage.
Running individual Quartus II software executables (quartus_map , quartus_fit , and so on) from within the Quartus II Tcl Console may cause the Quartus II software to crash.	You should run individual executables either from within the Quartus II scripting shell (quartus_sh) or directly at a command prompt.
If you have chosen migration devices in the Compatible Migration Devices dialog box, which is available from the Device page in the Settings dialog box on the Assignments menu, the Timing Closure floorplan displays only the pins and PLLs that are common to all the selected devices. However, the Chip Editor displays all the pins and PLLs available for the device specified for compilation.	
The time shown in the Status window may not agree with the processing times reported in the Compilation Report. This difference is due to differences in how the times are calculated during processing.	
If you type a name in the entity column of the Assignment Editor that differs from an existing name only by case, the Assignment Editor’s “auto-completion” feature always uses the existing name.	Type the new entity name in another application, such as a text editor, copy it to the clipboard, and paste the name from the clipboard into the Assignment Editor.
Altera recommends that you do not use node or entity names that differ only by case if you are using the Quartus II Simulator or Waveform Editor.	

Issue	Workaround
Under certain circumstances, a design that uses Virtual Pin assignments may fail to fit after back-annotation. This situation occurs because the clock signals chosen automatically for the first compilation do not match those chosen for the second compilation.	Manually assign your clock signals, using Virtual Pin Clock assignments before the first compilation, or use Advanced Back-Annotation to explicitly write out the virtual clock assignments before the second compilation.
If you use the <code>dcfifo</code> or <code>scfifo</code> megafunctions in an AHDL design, you may receive an error message similar to “The parameter <code>LPM_WIDTHU</code> has been set to an invalid value...”	Either remove the <code>LPM_WIDTHU</code> parameter arguments from your AHDL <code>dcfifo</code> or <code>scfifo</code> megafunction instantiation, or explicitly set the <code>LPM_WIDTHU</code> parameter to <code>ceil(log2(LPM_NUMWORDS))</code> .
Do not open, change permissions, or delete the <code><project directory>/db</code> directory or any file therein while any Quartus II executable is running.	
If you are using the IP Toolbench and add a user library, the Quartus II software may add a backslash (\) to the end of the library file name. The Quartus II user interface ignores this trailing backslash.	
Support for non-decimal radix numbers (such as hexadecimal) used as constants in the <code>lpm_constant</code> , <code>lpm_compare</code> , and <code>lpm_add_sub</code> megafunctions is limited to values that can be represented by 31 bits or fewer.	For values that require more than 31 bits, use decimal radix only.

Issue	Workaround
<p>Under certain circumstances, back-annotation of routing in unreserved LogicLock regions can cause routing constraints that cannot be satisfied for signals going to clock and clock-enable ports of LABs. This can occur when other portions of the design are not back-annotated, and the Fitter populates empty LCELLs in the back-annotated LogicLock region during subsequent compilations. For example, assume that on the initial compilation, LogicLock region L contains register A, which uses the CLK1 and ENA1 ports of a LAB. When the design is recompiled, the Fitter may place register B, which is not part of region L, and uses the SLOAD input, in the same LAB as register A (assuming that the LAB has sufficient empty space to accommodate it).</p> <p>The LAB control signal generation block does not allow use of both ENA1 and SLOAD in the same LAB; therefore, register A must use the CLK0 and ENA0 ports, rather than CLK1 and ENA1. To avoid a no-route situation, the Fitter will ignore the routing constraints for the clock and enable signals, and re-route the signals using the appropriate control signal multiplexing for the CLK0 and ENA0 ports of the LAB. The Fitter picks the most appropriate routing and, in the majority of cases, the circuit's timing is not adversely affected. When the Fitter is forced to ignore routing constraints, info messages of the form "Info: Can't route signal <name> to atom <name>" are displayed to inform the user; the appearance of such messages is not a cause for alarm.</p>	<p>This situation can be avoided entirely by marking all LogicLock regions as Reserved, thereby preventing the Fitter from placing new items in a region. The tradeoff, of course, is that should a Reserved LogicLock region be under-utilized, the Fitter will be unable to place other logic items in the unused portion of the region.</p>

Platform-Specific Issues

Windows Platforms Only

Issue	Workaround
The introduction of Microsoft Security Update MS05-026 prevents the proper display of Quartus II Help across a network.	To properly display HTML Help files, you must access them from a local PC. If you are unable to access Help files locally, go to Microsoft Knowledge Base Article 896054 (support.microsoft.com/?kbid=896054) for more information about possible workarounds.
The keyboard accelerators (underlines) for Alt+ key combinations do not appear in the Quartus II user interface until the Alt key is pressed the first time.	This behavior is a Windows 2000 user-specified preference. To change to the previous behavior, follow these steps: <ol style="list-style-type: none"> 1. On the Start menu, click Control Panel 2. Click Display properties 3. Click the Appearance tab 4. Click Effects 5. Turn off "Hide underlined letters for keyboard navigation until I press the Alt key"
If you use Windows 2000 as a software server to serve the Quartus II software to a client computer running Windows XP, running the Quartus II software on the Windows 2000 server at the same time clients are running the Quartus II software, will cause the Quartus II software on the server to crash.	Do not run the Quartus II software on the Windows 2000 server.
Some dialog box title bar text is not displayed correctly when the Quartus II software is installed on a computer running the Chinese version of Windows XP.	Change the font in the Active Title Bar section of the Windows Appearance Control Panel to Arial 10 pt, Trebuchet 10 pt, or a smaller size of the current font.
If you do not have Administrator privileges when you install the Quartus II software, certain features of the software, particularly the online Help, will not work properly.	Altera recommends that you have Administrator privileges when installing the Quartus II software.

Issue	Workaround
<p>Under certain circumstances, the Quartus II installation program may crash or you may receive an error message immediately upon launching the installation program.</p>	<p>Reinstall the stdole32.tlb file from the original Windows distribution disks. To reinstall the file, type the appropriate command at a command prompt. (Note: the command must be typed on one line.)</p> <p>Windows 2000: <CD-ROM drive letter>:\i386\expand.exe stdole32.tl_ %SystemRoot%\System32\stdole32.tlb <Enter></p> <p>Windows XP: <CD-ROM drive letter>:\i386\expand.exe stdole32.tl_ %SystemRoot%\System32\stdole32.tlb <Enter></p>
<p>If the full, hierarchical name of an instance exceeds 247 characters, it may not be displayed properly in the Quartus II user interface. This problem occurs most often with EDIF netlist files generated by other EDA synthesis tools.</p>	<p>Limit the full, hierarchical instance name to fewer than 247 characters if possible.</p>
<p>Due to a limit of the Windows operating system, path names longer than 229 characters can cause an internal error in the Quartus II software.</p>	<p>Make sure that all path names do not exceed 229 characters. This limitation applies to UNIX and Linux installations also.</p>
<p>If you are running the Quartus II software from a network server, the Quartus II software will not run properly on the client computer if you share the \quartus\bin directory.</p>	<p>You must share the \quartus directory, not the \quartus\bin directory.</p>
<p>The Quartus II software is not compatible with the MATLAB web server.</p>	<p>Turn off the MATLAB web server in the Services Control Panel on the Start menu before running the Quartus II software.</p>
<p>Under some circumstances, the Quartus II splash screen appears and the Quartus II icon appears in the Taskbar, but the graphical user interface does not appear. Under other circumstances, the user interface appears but windows and/or toolbars do not appear correctly.</p>	<p>The registry settings controlling the position of the Quartus II windows may have become corrupted. If the user interface appears, click the Reset All button on the Toolbars page of the Customize dialog box, or, if the user interface does not appear, type the following command at a command prompt: quartus -reset_desktop <Enter></p>

Issue	Workaround
<p>If you install the stand-alone Quartus II Programmer and the Quartus II software, and then uninstall either one, the Programmer may report “JTAG Server -- internal error code 82 occurred” when you click the Add Hardware button in the Hardware Setup dialog box on the Edit menu. This error occurs because uninstalling the software has disabled the JTAG Server service.</p>	<p>Manually restart the JTAG Server service by locating the jtagserver.exe program and at a command prompt for that directory, type <code>jtagserver --install</code> <Enter></p>
<p>If you choose to uninstall a previous version of the Quartus II software during installation, and there is a “locked” file or directory, the installation program will not reboot the computer as is necessary to successfully complete the installation.</p>	<p>Exit from the installer and reboot the computer manually after the removal of the previous version is complete, before completing the installation of the new version.</p>
<p>The Quartus II software version 4.2 and later does not allow a Parallel Port Software Guard (T-guard or dongle) to be used on the same parallel port as a ByteBlaster™ II download cable.</p>	<p>Use another download cable, such as a USB-Blaster™ or MasterBlaster™ to configure your device, or use separate parallel ports for the Software Guard and the download cable. The Quartus II Programmer is not a licensed feature, so you can remove the Software Guard to program your device, but you must replace it to use any other Quartus II software features. You can also use the USB Software Guard.</p>
<p>During installation of the Quartus II software, when you insert the ModelSim-Altera CD-ROM, a Windows Explorer window may appear.</p>	<p>Close the Windows Explorer window before proceeding with the installation.</p>

Solaris, HP-UX & Linux

Issue	Workaround
<p>On certain Solaris 8 and Linux systems, the text in the Assignment Editor and in other dialog boxes may not be readable because of the text size.</p>	<p>Delete or move the <code>~/mw</code> directory and restart the Quartus II software.</p>
<p>If the operating system crashes, and the file system in \$TMP is rebuilt automatically, the data in the <code>\$TMP/Mw_<user ID></code> file is corrupted, the Quartus II software may fail to start correctly.</p>	<p>Delete the <code>\$TMP/Mw_<user ID></code> file and restart the Quartus II software.</p>

Issue	Workaround
If you are using the Exceed X server software for Windows while running the Quartus II software, the font size may be larger than the line height. This problem occurs most often if you installed the Exceed software while running at a screen resolution greater than 1024 × 768.	Reinstall the Exceed software while running at a screen resolution of 1024 × 768. You can then switch back to your normal, higher resolution setting.
Under some circumstances, there may be editor windows listed on the Window menu that you cannot see.	To display the hidden windows, click Cascade on the Window menu.
You cannot launch the AXD Debugger software from within the Quartus II software.	Launch the AXD Debugger software from outside the Quartus II software.
Under some circumstances, the Internet connectivity features of the Quartus II software are not functional.	Specify the full path to your web browser software on the Internet Connectivity page of the Options dialog box. If you access the Internet through a proxy server, you must also specify the address of the proxy server and its port number.
Under some circumstances you cannot access the Quartus II online Help in the user interface.	To access Help, type <code>hh quartus.chm</code> <Return> at a command prompt.
If you are accessing the Quartus II software through one of the following versions of the Hummingbird Exceed software (6.2, 7.0, 7.1, or 8.0) and have any Microsoft Office application or Internet Explorer open, the Quartus II user interface may start very slowly.	Contact Hummingbird Software at www.hummingbird.com for a patch for the Exceed software.
If you are running the Quartus II software version 4.0 and later on a Linux or Solaris workstation, even though Reopen current project and files at startup is turned on, the last project is not reopened when you restart the software.	Use the Recent Projects command on the File menu to reopen your last project.
The stand-alone Quartus II Programmer and SignalTap® II programs are not available on Solaris, Linux, and HP-UX workstations.	

Solaris Only

Issue	Workaround
The Excalibur™ MegaWizard Plug-In , which is available from the MegaWizard Plug-In Manager , requires the Java Runtime Environment (JRE), which has already been installed on your computer. On Solaris workstations, however, you may need to install extra patches to the operating system in order for the JRE to function properly.	Check the web site http://sunsolve.sun.com/pub-cgi/show.pl?target=patches/J2SE for information about any patches that might be needed.

HP-UX Only

Issue	Workaround
You receive error messages indicating that you do not have required permissions to perform the requested operation while using Network Information Services (NIS).	Add a plus-sign (+) followed by a carriage return on a line by itself as the last line in both of the following files: /etc/passwd and /etc/group .
Programming EPC16 configuration devices is disabled on HP-UX workstations.	

Linux Only

Issue	Workaround
If you run a remote Linux desktop session in a Windows client such as Exceed, depending on your configuration, the SignalTap II Logic Analyzer may be unstable and could crash with a segmentation fault.	Use an Xterm window to access the Quartus II software instead of a remote desktop session.
Clicking the “X” close button is visible on the Chip Editor loading progress dialog box may cause the Quartus II software to crash.	Do not click the “X” button while the Chip Editor is loading.
If the MasterBlaster™ download cable is not listed in the Available hardware items list in the Hardware Settings tab of the Hardware Setup dialog box, but it is connected properly, you may not have read/write permission for the serial (<code>dev/ttySx</code>) port to which the MasterBlaster cable is connected.	Have a system administrator assign read/write permission for the appropriate port. This change can be accomplished by adding you to the “uucp” group, or by giving read/write permission for the serial port to everyone, using the following command: <code>chmod o+rw /dev/ttySx</code> where <i>x</i> is the serial port affected.

Issue	Workaround
<p>If you are using the ReflectionX X-server software as your display on a Linux workstation, the Quartus II software may hang and a white box may appear.</p>	<p>Set the <code>QUARTUS_MWWM</code> environment variable to <code>allwm</code> and then start the Quartus II software without the splash screen by typing the following commands at a command prompt: <code>setenv QUARTUS_MWWM allwm <Return></code> <code>quartus -no_splash <Return></code></p>
<p>Under certain circumstances, the Quartus II software may not start properly.</p>	<p>On a system with a static IP address, ensure that the <code>/etc/hosts</code> file has an entry for the host name of the machine on which you are running. For example, if the workstation is named “orange,” there should be an entry in <code>/etc/hosts</code> with the IP address of the “orange” workstation as shown below: <code><IP address of orange> orange</code> In addition, the network configuration (hostname, DHCP host name, DNS search path, and domain names) must be correct or the Quartus II software will abort on startup.</p>
<p>If you are running the Quartus II software version 4.0 and later using VNC software, the Quartus II software may terminate unexpectedly whenever you open any file or browse any directory from within the Quartus II software.</p>	<p>Make sure your VNC server software is version 3.3.4 or later.</p>
<p>If you are running the Quartus II software under Red Hat Linux 8.0, you may experience substantial degradation of compilation times if your design files are located on a separate server from the Quartus II software.</p>	<p>Make sure that the operating system kernel is upgraded to the latest available. If you are using a NetApps server, refer to the following document for more information: www.netapp.com/tech_library/ftp/3183.pdf</p>

Device Family Issues

Excalibur

Issue	Workaround
<p>You may receive the message “System Build Descriptor File missing parameter programming clock frequency” for System Build Descriptor Files (.sbd) generated in the Quartus II software version 2.0 and earlier, after selecting the Boot from Serial option in the ARM-based Excalibur MegaWizard Plug-In.</p>	<p>Rerun the ARM-based Excalibur MegaWizard Plug-In in the current version of the Quartus II software to regenerate the SBD File and correct the error.</p>
<p>If you are using the Stripe-to-PLD Bridge in Excalibur EPXA10 Devices, your design may not function due to the Stripe-to-PLD Bridge lockup errata if either of the following options is turned on in the Quartus II software: Remove Redundant Logic Cells Perform WYSIWYG Primitive Resynthesis Please refer to the <i>EPXA10 Device Errata Sheet</i> for details on the device errata.</p>	<p>To avoid bridge lockup, ensure that the Remove Redundant Logic Cells option is turned off for the project. If the Perform WYSIWYG Primitive Resynthesis option is turned on for your project, you may receive warnings that the stripe signals were not routed correctly. To eliminate the warnings, re-run the MegaWizard Plug-In Manager in the Quartus II software version 2.2 or later. This procedure will create an additional settings file (alt_exc_stripe.esf) to ensure that the required logic elements are implemented.</p>

Cyclone, Stratix & Stratix GX

Issue	Workaround
<p>When you use a Routing Constraints File (.rcf) to control fitting after performing Routing Back-Annotation, your timing analysis results may change slightly due to parasitic and other effects. Any change will be very small.</p>	
<p>If you use the SignalProbe feature to observe the signals at an output pin, by routing them to another output pin, the SignalProbe output pin signal will be shown as Unknown (X) in the Quartus II Simulator.</p>	<p>The signal will be correct in actual operation, the error appears only in the Quartus II Simulator.</p>

Issue	Workaround
<p>In the SignalProbe Source to Output Delays table of the Timing Analyzer Report, the following shortcut menu commands are not available although they are available in other similar Timing Analyzer Report tables:</p> <ul style="list-style-type: none"> • List Paths • Locate in Chip Editor • Locate in Timing Closure Floorplan 	<p>You can use other Timing Analyzer Report tables to list and locate the affected paths.</p>

Stratix and Stratix GX

Issue	Workaround
<p>If you use the <code>altddio_bidir</code> or <code>alt_dqs</code> megafunction and connect any data port directly to VCC or GND, the Quartus II software version 3.0 SP1 and later will insert an additional logic element in the circuit path.</p>	
<p>The behavior of the 0-degree phase shift setting of the <code>DLL_PHASE_SHIFT</code> parameter of the <code>altdqs</code> megafunction or the DQS Phase Shift logic option with the <code>altddio_bidir</code> megafunction has changed in the Quartus II software version 3.0 SP2. The previous behavior produced an uncharacterized delay that cannot be specified to fall within the specified 500 ps delay difference.</p>	<p>If your design uses this setting and does not work correctly after installing the Quartus II software version 3.0 SP2 or later, you should contact the Altera Applications department for further information.</p>

Stratix

Issue	Workaround
<p>Designs compiled for Stratix EP1S40ES devices must be recompiled for the EP1S40 device before programming.</p>	
<p>Stratix PLL simulation models have been enhanced to handle jitter on the input clock. This enhancement has the unintended side effect that functional simulations for LVDS designs using cascaded PLLs may be incorrect by one clock cycle.</p>	<p>Altera recommends that you perform Timing Simulation to display the correct behavior in the Quartus II Simulator or in other EDA Simulators.</p>

Stratix II

Issue	Workaround
An intermittent read failure has been detected on Stratix II M4K RAM blocks due to a software configuration error for designs compiled with Quartus II software version 5.0 SP1 and earlier.	This issue has been resolved in the Quartus II software 5.0 Service Pack 2 and Quartus II software version 5.1. To learn more about this issue, please refer to the Stratix II Errata on the Altera web site.
Due to changes in the <code>altlvds_tx</code> and <code>altlvds_rx</code> megafunctions in the Quartus II software version 5.0, user-created timing assignments to the megafunctions are changed. The megafunctions now make most timing assignments automatically.	Check your assignments to make sure that the Quartus II software implemented them correctly.
The Quartus II software version 5.0 does not support programming file generation for some Stratix II devices when M-RAM blocks are used in some memory modes, and if the <code>STRATIXII_MRAM_COMPATIBILITY</code> option is turned off.	For more information about programming file support for Stratix II devices, please refer to the <i>Stratix II FPGA Family Errata Sheet</i> , which is available on the Altera web site.
The Quartus II software version 4.2 and later supports programming file generation for EP2S60 ES devices, but only for designs where the M-RAM memory is not used.	For more information about programming file support for Stratix II devices, please refer to the <i>Stratix II FPGA Family Errata Sheet</i> , which is available on the Altera web site.
Back-annotating some designs targeted to a Stratix II device with the Demote cell assignments to option set to LABs may prevent the design from fitting.	Back-annotate the design with Demote cell assignments to turned off.

Stratix GX

Issue	Workaround
The RREFB pin names for EP1SGX10C, EP1SGX25C, EP1SGX25D, and the EP1SGX40F devices changed in the Quartus II software version 5.0. This may affect your PCB layout.	Each RREFB pin must be tied to ground through a resistor. Altera recommends that you not connect multiple RREFB pins through a single resistor to ground.

Stratix II GX

Issue	Workaround
<p>In the Quartus II software release 5.1 SP1, a single <code>alt2gxb_reconfig</code> megafunction can feed only one <code>alt2gxb</code> megafunction with up to 4 GXB channels. If it feeds more than one <code>alt2gxb</code> megafunction, or if it feeds a single <code>alt2gxb</code> megafunction with more than 4 GXB channels, you will receive the following error:</p> <pre>“Error: Output port dprioout of GXB Central Control Unit "xxx" can only be connected to logic generated from alt2gxb reconfig megafunction.”</pre>	<p>To control more than 4 GXB channels, you can create up to five identical <code>alt2gxb_reconfig</code> megafunctions, each driving a single <code>alt2gxb</code> megafunction with up to 4 GXB channels each.</p>
<p>The Quartus II software automatically assigns PCI Express related reference clock input pins in the design to the 1.2V PCML I/O standard. In version 6.0 and later, the Quartus II software will allow the specification of the HCSL (Host Clock Signal Level) I/O standard which will allow the reference clock to be DC coupled on the board.</p>	<p>The board can be laid out using the Quartus II software version 5.1 SP1 assuming that DC coupling support for the reference clock pins that will be provided for PCI Express-related reference clock input pins in a future release of the Quartus II software.</p>
<p>The Quartus II software issues a warning when the GXB Transmitter PLLs in the designs are not clocked by the dedicated GXB REFCLK pins (in the same Quad or in a different Quad). The warning is issued because the REFCLK pins provide the best jitter performance and are recommended for providing the reference input clock to the GXB Transmitter PLLs.</p>	<p>If you desire the best jitter performance from the GXB Transmitters that are fed from the Transmitter PLL, use a GXB REFCLK pin to feed the reference input clock signal.</p>
<p>The <code>fixedclk</code> signal for PCI Express <code>alt2gxb</code> designs should have a frequency of 125 MHz. Versions of the Quartus II software previous to 5.1 SP1 did not enforce this frequency limit. The Quartus II software version 5.1 SP1 and later issue a warning if it detects that the <code>fixedclk</code> signal is not 125 MHz or higher.</p>	<p>Ensure that the <code>fixedclk</code> signal is 125 MHz or higher.</p>

Issue	Workaround
<p>The <code>rmfifodatadeleted[]</code>, <code>rmfifodatainserted[]</code> ports have been removed from the <code>alt2gxb</code> megafunction and are no longer supported. Designs with these signals result in a no-fit in the Quartus II software version 5.1 SP1.</p>	<p>Remove these signals from your <code>alt2gxb</code> megafunction instantiation.</p>
<p>If you assign an I/O standard of LVDS, LVPECL or 3.3V PCML to the GXB REFCLK I/Os in the transceiver banks, the Quartus II Fitter will not fit the design and will issue error messages similar to "Pin uses I/O standard <code><io std></code>, which has a VCCIO requirement incompatible with that bank's VCCIO setting or its other pins that use VCCIO <code><1.5V/1.2V></code>" when the transceiver I/O bank has GXB Receiver or GXB Transmitter channels used.</p> <p>The GXB REFCLK pins support the following I/O standards: 1.2V PCML, 1.5V PCML, 3.3V PCML, LVPECL and LVDS.</p>	<p>Assign the reference clock pins in your design to the 1.5V PCML or 1.2V PCML I/O standards. On your board, you can plan to bring in your LVDS, LVPECL or 3.3V PCML clock pin, as long as it is AC-coupled. The Quartus II software version 6.0 will correctly support the LVDS, LVPECL and 3.3V PCML I/O standards on the REFCLK I/O pins.</p>
<p>The Quartus II software will crash with an internal error if you make a SignalProbe connection within an HSSI block.</p>	<p>Do not make SignalProbe connections within an HSSI block.</p>
<p>In Basic protocol, when the 8B10B encoder is used, the <code>alt2gxb</code> MegaWizard provides the <code>tx_forcedisp</code> and <code>tx_dispval</code> ports. These ports do not have any effect on the transmitted serial data when used in the Quartus II software version 5.1. This behavior is reflected in simulation.</p>	<p>None necessary.</p>

Cyclone

Issue	Workaround
<p>Altera recommends that the frequency of the external clock output of the PLLs be limited to 312 MHz.</p>	

Issue	Workaround
<p>The operating frequency range of the Cyclone PLL has been changed. In the Quartus II software version 3.0 and earlier, the range was 300 MHz to 800 MHz. In version 3.0 Service Pack 1 and later, that range changed to 500 MHz to 1000 MHz because of concerns about jitter at frequencies below 500 MHz. Because of this change, the minimum input frequency is now 15.625 MHz (previously 15 MHz) and the minimum output frequency is also 15.625 MHz (previously 9.38 MHz).</p>	<p>Recompile your design after installing the current version of the Quartus II software.</p>
<p>The PLL lock circuit does not function correctly for PFD (Phase Frequency Detector) frequencies below 200 MHz when the temperature is below -20°C.</p>	<p>If operation at temperatures below -20°C is required, choose a higher input frequency and clock division (N) factor such that the PFD input frequency is higher than 200 MHz.</p>

Cyclone II

Issue	Workaround
<p>The PowerPlay Power Analyzer in Quartus II 5.1 and Quartus II 5.1 SP1 does not correctly compute the Static Thermal Power Dissipation of the Vccint power supply for Cyclone II devices when Maximum device power characteristics are chosen. Devices other than Cyclone II are not affected, and Cyclone II typical power is not affected.</p>	<p>Use the Cyclone II PowerPlay Early Power Estimator located on the Altera web site.</p>
<p>The pin-out (.pin) file generated by the Quartus II software for Cyclone II devices in 256-pin and 484-pin FBGA packages shows erroneous “NC” pins when vertical migration is selected. On 256-pin packages, pins J10 and K8 are mislabeled. On 484-pin packages the following pins are mislabeled: J8, J9, K8, K15, L7, L15, L16, M7, M8, M15, M16 N8, and P14.</p>	<p>The “Direction” and “Voltage” columns of the pin-out file contains the correct information for the affected pins.</p>

Issue	Workaround
A write error has been detected on Cyclone II M4K RAMs when using dual ports and dual clocks for designs compiled with Quartus II software version 5.0 SP1 and earlier.	A software workaround is available to address this issue in the Quartus II software version 5.0 SP2 and Quartus II software version 5.1. To learn more, please refer to the Cyclone II Errata on the Altera web site
If your design uses dual-port, dual-clock memory with a Memory Initialization File (.mif) and you have set the CYCLONE_SAFE_WRITE parameter in the altsyncram megafunction to RESTRUCTURE, any changes to the MIF file contents will be ignored if you have Smart Compilation turned on.	
Back-annotating some designs targeted to a Cyclone II device with the Demote cell assignments to option set to LABs may prevent the design from fitting.	Back-annotate the design with Demote cell assignments to turned off.

MAX II

Issue	Workaround
If your design uses an <code>altparallel_flash_loader</code> instantiation created in the Quartus II software version 5.0 SP1 or earlier, you may receive errors during compilation because the port names have changed in the <code>altparallel_flash_loader</code> megafunction included in the Quartus II software version 5.1.	Use the Megawizard Plug-in Manager to regenerate your <code>altparallel_flash_loader</code> instantiation. Modify your design files to connect to the new <code>altparallel_flash_loader</code> port names.

HardCopy II

Issue	Workaround
<p>The HardCopy II Companion Revision Comparison tool can be too strict and produce false positives. That is, it flags certain netlist block differences as functionality differences when they do not actually produce different behavior in silicon. The following examples illustrate this behavior:</p> <ul style="list-style-type: none"> • When a DSP multiplier uses distinct asynchronous clears on its input registers, they might be ordered differently on the two revisions, but still have the same functionality. • Additional clock buffers may be inserted by the Fitter during routing that are different between the two revisions, but function identically. • The Companion Revision Comparison tool considers a global assignment of <NONE> to be different from "" (null), and reports a difference. 	<p>In each of these cases, the functionality of the two revisions is the same in silicon, but you must manually verify that the functionality is the same. You can use the block names listed in the Companion Revision Report to locate to the Resource Property Editor to verify the functionality</p>
<p>If you have multiple Stratix II devices in a migration chain for a HardCopy II device, you will receive a critical warning that the feature is not supported in the software.</p>	<p>Ignore the critical warning, it is in error, the feature is supported.</p>
<p>PCI core designs compiled with versions of the PCI Compiler earlier than 4.0.0 will cause numerous spurious differences to be reported in the Companion Revision Compare section of the Compilation Report, even though the source files are correct.</p>	<p>Recompile the PCI core with the PCI Compiler version 4.0.0 or later.</p>
<p>If a PLL placed at a corner PLL location (PLL_7, PLL_8, PLL_9, or PLL_10) uses global clocks for its clock outputs, then the Companion Revision Compare report may incorrectly report that the PLL changed between the Stratix II and the HardCopy II compilation.</p>	<p>Make GLOBAL_SIGNAL assignments to the PLL clock outputs, recompile the design, and run the Companion Revision Compare command again.</p>

Issue	Workaround
If a PLL is being driven by a side clock, the Companion Revision Compare report may incorrectly report a difference in the PLL structures because the name of the CLKCTRL atom driving the PLL may be different in the Stratix II revision versus the HardCopy II revision.	Use global clocks to drive the PLL.
You may receive Revision Comparison warnings about differing EDA tool settings if your project directory contains a Quartus II Defaults File (.qdf).	Delete the Quartus II Defaults File from your project directory.

Design Flow Issues

Verification

Issue	Workaround
When an application that uses the JTAG interface to communicate with an Altera device (that is, SignalTap II, Nios II, and so on) is running, a Tcl script that calls the commands in the <code>jtag</code> Tcl package may fail with a timeout error if the <code>-timeout</code> argument is not specified with the <code>device_lock</code> Tcl command. The default timeout value of 0 sets the timeout to immediate.	Specify a non-zero timeout value when calling the <code>device_lock</code> command
If you are using IP Toolbench to generate simulation models for Altera IP Megacore [®] functions, you will get an error if support for the Stratix device family is not installed.	Install support for the Stratix device family.
If you are using IP Toolbench to generate simulation models for Altera IP Megacore [®] functions, and you do not turn on Generate Simulation Model in the Set Up Simulation Model dialog box during setup, you will get an error when you launch the simulation using <code>Modelsim</code> .	Turn on Generate Simulation Model in the Set Up Simulation Model dialog box and regenerate the Megacore [®] .

Issue	Workaround
<p>Incremental routing may fail for nodes assigned to the SignalTap II Logic Analyzer if you have turned on any of the Physical Synthesis Fitter optimizations, such as Perform physical synthesis for combinational logic or Perform register duplication or Perform register retiming.</p>	

Integrated Synthesis (VHDL and Verilog HDL)

Issue	Workaround
<p>When a VHDL or Verilog design specifies a RAM, there are a few cases in which the read-during-write behavior of the RAM will differ between the original design and the hardware implementation and no warning will be given. The following examples illustrate this behavior:</p> <p>The first case occurs when a RAM in a lower-level module directly drives a set of registers in an upper-level module. To work around this problem, move the registers to the lower-level module.</p> <p>The second case occurs when there is combinational logic between a RAM and a set of registers, and the design specifies the write operation of the RAM will occur before the read operation. To work around this problem, remove the logic between the RAM and the registers.</p> <p>The third case is the same as the second case, with the exception that the design specifies the read operation of the RAM will occur before the write operation, and the read address of the RAM is registered. To get around this problem, either remove the logic between the RAM and the registers, or set the Automatic RAM Replacement option to “Off.”</p>	<p>The workaround for each case is shown immediately following the example.</p>

Issue	Workaround
<p>The Quartus II software version 4.0 and later may give the message “Error: Duplicate entity <name> found in file <filename1> colliding with the one found in file <filename2>,” for a project that compiled successfully with Quartus II 2.2 or earlier.</p>	<p>The Quartus II software gives an error message when it finds two or more entities with the same name. To avoid this error in the future, remove the duplicate entity or entities. If you cannot remove the duplicate entity, you can direct the Quartus II software to ignore the duplication by adding <code>set_global_assignment -name IGNORE_DUPLICATE_DESIGN_ENTITY ON</code> to your Quartus II Settings File (.qsf). Altera recommends that you avoid using this workaround if possible.</p>

Verilog HDL Integrated Synthesis

Issue	Workaround
<p>A Verilog HDL design that compiles successfully in earlier versions fails in the Quartus II software version 5.1 with the message “Formal port <port_name> must be connected to a structural net expression.”</p>	<p>The Verilog language requires that a module instance output port be connected to a net, and not to a reg variable or to a constant. Previous versions of the Quartus II software did not enforce this restriction. Change the variable connected to the module instance output port to a wire datatype.</p>
<p>A Verilog design that compiles successfully in earlier versions fails in the Quartus II software version 5.0 with the message “Error: Verilog HDL or VHDL error at <filename(line)>: object "<pin_name>" declared in a List of Port Declarations cannot be redeclared within the Module Body”</p>	<p>Remove the declaration in the module body. Ports must be completely specified in the Verilog 2001 list of ports declaration, including where necessary the direction, width, net or variable type, and whether the port is signed or unsigned.</p>

SignalTap II

Issue	Workaround
<p>Under some circumstances, an incremental SignalTap II compilation that follows a full compilation for a Cyclone II device, will fail with an error message reporting that an input port cannot be inverted.</p>	<p>Perform a full compilation and reapply the SignalTap II settings.</p>

Issue	Workaround
<p>In SignalTap II, nodes dropped in from the Node Finder are always sorted and inserted in descending order, for example, <code>foo[3]</code>, <code>foo[2]</code>, <code>foo[1]</code>, <code>foo[0]</code>. If this is the incorrect order, you can select the LSB on Top, MSB on Bottom option. In version 5.1, negative ranges are now allowed in Verilog HDL, however negative numbers are inserted in the reverse order, for example, <code>foo[3]</code>, <code>foo[2]</code>, <code>foo[1]</code>, <code>foo[0]</code>, <code>foo[-3]</code>, <code>foo[-2]</code>, <code>foo[-1]</code>.</p>	

Logic Analyzer Interface

Issue	Workaround
<p>When multiple instances of the Logic Analyzer Interface (.jai) are instantiated in a design, the I/O pins for each instance will have identical names, causing an error.</p>	<p>Open the Logic Analyzer Interface file in a text editor and rename the duplicate pin names. Then, assign locations to the corrected pin names with the Quartus II Pin Planner.</p>

SOPC Builder Issues

Issue	Workaround
<p>Back-to-back burst transfers from a master to a slave that has a different burst count or bandwidth may fail.</p>	<p>Wait until the slave has finished the read burst before starting a write burst.</p>
<p>Under some circumstances, the automatic addressing feature does not function correctly.</p>	<p>Assign the base address for the component manually.</p>
<p>Under some circumstances, the SOPC Builder does not display correctly on systems in which the graphics card uses hardware acceleration.</p>	<p>Turn off, or reduce the level of hardware acceleration.</p>
<p>In SOPC Builder, Avalon Masters that address more than 32 bits of slave address space do not issue warning.</p>	<p>Redesign your system to avoid giving masters greater than 32 bits of address space.</p>

Issue	Workaround
<p>On the SOPC Builder PLL component, you cannot access the <code>pfdena</code> signal through the <code>Avalon control</code> register. If you enable the <code>pfdena</code> signal on the <code>altpll</code> block, the PLL component configuration GUI allows you to select that you want to access the <code>pfdena</code> signal via the <code>PFDENA</code> bit in the <code>control</code> register. However, the hardware does not support this mode of operation. Software attempting to access the <code>PFDENA</code> bit will not function correctly.</p>	<p>You can export the <code>pfdena</code> signal to the top level of the system module, or you can disable the <code>pfdena</code> signal on the <code>altpll</code>. This feature will be supported in a future version of the Quartus II software.</p>
<p>If you open more than one SOPC Builder project simultaneously, you will receive an error message similar to the following example: “bad or corrupt 'class.ptf' file.”</p>	<p>Open the SOPC Builder only when no other SOPC Builder project is already open.</p>
<p>SOPC Builder fails to open on UNIX when invoked from the MegaWizard Plug-In Manager.</p>	<p>Open SOPC Builder by clicking SOPC Builder on the Quartus II Tools menu.</p>
<p>You may see random display errors, such as streaks and blotches, in the SOPC Builder GUI.</p>	<p>Lower the Hardware Acceleration setting on the Troubleshooting tab of the Advanced Display Settings dialog box in your Display Settings control panel. There is a known incompatibility between the current Java Runtime Environment (JRE) and certain laptop graphics drivers.</p>
<p>When creating a component with the SOPC Builder Component Editor, you must not choose a component name that exactly matches the HDL file name or the top-level module name. If the names are the same, SOPC Builder will generate an error during system generation. This problem will be fixed in a future version of SOPC Builder.</p>	<p>Using the SOPC Builder Component Editor, rename the component to a different name. In the SOPC Builder table of active components, add the newly-named component to your system, and delete the old component.</p>
<p>If the Quartus II software is installed in a directory that has space characters in its name, the SOPC Builder software will not run.</p>	<p>Install the Quartus II software in a directory that does not have space characters in the path.</p>

Issue	Workaround
<p>When adding an Excalibur Stripe component in conjunction with Avalon peripherals, you may encounter SOPC Builder errors indicating that too many masters are present.</p>	<p>If the master-connection patch-panel is not visible, click Show Master Connections on the View menu. Then click the master/slave intersection indicated by the error message. This will remove the connection. Click again to restore the connection and the error will not reappear.</p>
<p>Designs targeting Excalibur devices that use Boot From Flash mode may not operate when downloaded to the target board if the Quartus II Software Builder or SOPC Builder Excalibur-build script was used to generate the flash programming file.</p>	<p>The Excalibur boot loader in the Quartus II software version 3.0 and later does not function correctly if the Quartus II Software Builder is used to generate the flash programming file. This is because the compression option that is used with the makeprogfile utility during the software build process does not work with this version of the boot loader. To work around this issue, do not use the Software Builder to generate a programming file, but instead use the makeprogfile utility at the command line with the -nc (no compression) option. If you are using the SOPC Builder Excalibur-build script, you must edit the script located in the <code><XA dev kit install directory>\bin</code> folder. Modify line 1034 of this script to remove the -nc option. For example, line 1034 should be changed as shown in this example.</p> <pre>\$command = "makeprogfile -nc -b \${fileBase}_bootdata.o \$SBD \$SBI \${fileBase}.hex" ;</pre> <p>You must recompile your software project for this change to take effect.</p>
<p>The SOPC Builder and Nios Software Development Kit shell may “hang” and become unresponsive if you run either program while the Frisk antivirus software is running.</p>	<p>Turn off the Dynamic Virus Checking feature of the Frisk software before running SOPC Builder or the Nios SDK shell.</p>

EDA Integration Issues

Issue	Workaround
<p>Timing simulation with the Synopsys VCS MX software is not supported in the Quartus II software version 5.1.</p>	

Issue	Workaround
You cannot perform RTL simulation of the SerialLite and RLDRAM IP MegaCores in 3 rd party simulators using the NativeLink integration feature.	Perform simulation manually as described in the User Guide for the MegaCore you are using.
FIFO Partitioner instances can only be simulated in 3 rd party simulators using the original VHDL source files from the quartus/libraries/megafunctions/ directory, and NativeLink integration is not supported.	Perform simulation manually as described in the FIFO Partitioner User Guide available from the Literature page of the Altera web site.
The current version of the Quartus II software allows you to select the Synplicity Amplify software as a physical optimization tool. However, this setting is for an automated mode called ATOPS, which is currently not supported by the Amplify software.	Contact Synplicity for the support schedule for the Amplify software ATOPS mode.
Support has been added for generation of IBIS Output Files (. ibs) for EPCS1 and EPCS4 Serial Configuration Devices.	The IBIS Output File will be generated in the <code>\<project name>\board\ibis</code> directory after compilation when the design is targeted to a Cyclone device and Active Serial configuration scheme using EPCS1 or EPCS4 devices is chosen.
NativeLink support does not work with versions of Mentor Graphics Precision RTL Synthesis Software earlier than version 2003b due to a change in the Precision project interface.	

Simulation Model Changes

The simulation model changes provided in Quartus II software version 5.1 Service Pack 1 are incorporated in Service Pack 2. For details, see the Quartus II software version 5.1 Service Pack 1 Release Notes.

Software Issues Resolved

The software issue resolutions provided in Quartus II software version 5.1 Service Pack 1 are incorporated in Service Pack 2. For details, see the Quartus II software version 5.1 Service Pack 1 Release Notes

Latest Known Quartus II Software Issues

For known software issues after publication of this version of the *Quartus II Software Release Notes*, please look for information in the **Quartus II Latest Known Issues** section of the Altera Support Find Answers Database at the following URL:

[http://answers.altera.com/altera/index.jsp?/Topics/Support/Solutions/Known Issues/Software/Quartus II](http://answers.altera.com/altera/index.jsp?/Topics/Support/Solutions/Known%20Issues/Software/Quartus%20II)

Revision History

Revision	Description
1.0	Initial Release

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