



Quartus II Device Support Release Notes

May 2006

Quartus II version 6.0

This document provides late-breaking information about device support in this version of the Altera® Quartus® II software. For information about memory, disk space, and system requirements, refer to the **readme.txt** file in your `\altera\quartus<version number>` directory. For information about New Features, EDA Tool version support, and existing and resolved software issues, refer to the *Quartus II Software Release Notes*.

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Device Support & Pin-Out Status

This section contains information about the status of support in the Quartus II software for the listed devices.

Full Device Support

Full compilation, simulation, timing analysis, and programming support is now available for the following new devices and device packages:

Devices with Full Support

Device Family	Devices	
Stratix® II	EP2S90H484	
Stratix II GX	EP2SGX90EF1152	EP2SGX90FF1508
HardCopy® II	HC210F484	HC220F672
	HC220F780	

Advance Device Support

Compilation, simulation, and timing analysis support is provided for the following devices that will be released in the near future. Although the Compiler generates pin-out information for these devices, it does not generate programming files for them in this release.

Devices with Advance Support

Device Family	Devices	
Stratix II GX	EP2SGX30CF780	EP2SGX30DF780
	EP2SGX60CF780	EP2SGX60DF780
	EP2SGX60EF1152	EP2SGX130GF1508
HardCopy II	HC210WF484	HC240F1020
	HC240F1508	

Timing Models

This section contains a summary of timing model status in the current version of the Quartus II software.

Preliminary Timing Models

The following table shows the devices with preliminary timing models in the current version of the Quartus II software:

Devices with Preliminary Timing Models

Device Family	Device	
HardCopy II	HC210	HC210W
	HC220	HC230
	HC240	
Stratix II GX	EP2SGX30	EP2SGX60
	EP2SGX90	EP2SGX130

Final Timing Models

The following table lists the devices with final timing models that are available in the current version of the Quartus II software:

Devices with Final Timing Models

Device Family	Device	Timing Models Final in Quartus II Version Number
Cyclone®	EP1C3	3.0 SP1
	EP1C4	4.0
	EP1C6	3.0
	EP1C12	3.0 SP1
	EP1C20	3.0
Cyclone II	EP2C5	6.0
	EP2C8	5.1 SP2
	EP2C20	5.1 SP2
	EP2C35	5.1 SP2
	EP2C50	6.0
	EP2C70	5.1 SP2
MAX® II	EPM240	5.0
	EPM1270	5.0
	EPM570	5.0 SP1
	EPM2240	5.0 SP1
Stratix	EP1S10	4.1
	EP1S20	4.1
	EP1S25	4.1
	EP1S30	4.1
	EP1S40	4.1
	EP1S60	4.1
	EP1S80	4.1
Stratix II	EP2S15	5.0 SP1
	EP2S30	5.0
	EP2S60	5.0
	EP2S90	5.0 SP1
	EP2S130	5.0 SP1
	EP2S180	5.1
Stratix GX	EP1SGX10	4.1
	EP1SGX25	4.1
	EP1SGX40	4.1

The current version of the Quartus II software also includes final timing models for the ACEX® 1K, APEX® 20K, APEX 20KE, APEX 20KC, APEX II,

FLEX[®] 6000, FLEX 10K, FLEX 10KA, FLEX 10KE, and MAX 7000S device families. Timing models for these device families became final in versions earlier than version 4.0.

Power Models

This section contains a summary of power model status for recent devices in the current version of the Quartus II software.

Device Family	Power Model Status
Stratix	Final – 5.1
Stratix GX	Final – 5.1
Stratix II	Final – 6.0
Stratix II GX	Preliminary
Cyclone	Final – 5.1
Cyclone II	Final – 6.0
MAX 3000A	Final – 5.1
MAX 7000AE	Final – 5.1
MAX 7000B	Final – 5.1
MAX II	Final – 5.0 SP1
HardCopy II	Preliminary

Changes in Device Support

Stratix II GX I/O Bank Locations

This issue affects EP2SGX130 devices. The Quartus II software version 5.1 SP1, and the pre-release Beta version of the Quartus II software version 6.0 show incorrect locations for I/O banks 15, 16, and 17. As a consequence, those software versions also show incorrect locations for the I/O banks used for PCI Express x8 applications. The Quartus II software version 6.0 shows the correct locations for the I/O banks.

Stratix II GX PCI Express x8 Configurations

This issue affects Stratix II GX devices. In the two quads that pair up for a PIPE x8 configuration, the bottom quad must be the driver quad, and the top quad must be the receiver(controlled) quad. Versions of the Quartus II software prior to version 6.0 allow an incorrect grouping with the driver quad being the top quad. Note that the Quartus II software allows the correct grouping also.

This issue is resolved in the Quartus II software version 6.0. Recompile your design with the Quartus II software version 6.0. If the Fitter reports errors due to the quad groupings, you must fix your location assignments and potentially your board layout. Please refer to the “Channel Clock Distribution” section in the Stratix II GX Transceiver User Guide for more information.

Stratix II PLL Scan Chain Frequency

This issue affects Stratix II and Stratix II GX devices. Final timing models are affected. PLL scan chain frequencies slightly below 100 MHz were flagged as timing violations by the Quartus II timing analyzer in previous releases. The PLL scan chain can be operated at up to 100 MHz in all Stratix II devices and all speed grades, and this version of the Quartus II software updates the timing analyzer to allow operation at this speed. Because this change increases only the maximum operation frequency of the PLL scan chain, you do not have to rerun the Timing Analyzer on any design which met timing in a previous version of the Quartus II software.

Stratix II M-RAM Byte Enable Support for x128 and x144 Modes

This issue affects Stratix II, Stratix II GX, and HardCopy II devices. M-RAM blocks in x128 or x144 mode support byte enables only when using single clock mode. If clock enables are used in x128 or x144 single clock mode, you must use

the same clock enable setting for both ports A and B. Byte enables are supported for other memory widths and modes as described in the TriMatrix Embedded Memory Blocks in Stratix II & Stratix II GX Devices chapter in volume 2 of the Stratix II Device Handbook. Software support for the affected modes is removed.

Cyclone II I/O Delays

The package trace delays for EP2C5 and EP2C50 devices are updated. This change affects the delay of I/O pins. The magnitude of the change is less than 100ps.

Cyclone II PowerPlay Early Power Estimator Spreadsheet

Support for Cyclone II extended temperature range devices is added to the Cyclone II PowerPlay Early Power Estimator spreadsheet version 6.0.

Stratix II DQS Phase Shift Limit

This change affects Stratix II, Stratix II GX, and HardCopy II devices. A maximum limit applies to DQS delays. Each delay buffer in the DQS delay chain is limited to a maximum delay of 0.833 ns in 6-bit mode, or 0.416 ns in 5-bit mode for the fast corner timing model. This limit affects memory interfaces using the Frequency Modes and Frequency Ranges shown in the table below. If the DLL and DQS are operating slower than the minimum frequency range in the table, then it is recommended to re-analyze your design timing using the fast corner timing model.

DLL and DQS Frequency Modes

Frequency Mode	Frequency Range (MHz)	Number of DLL Delay Buffers	Delay Buffer Mode	Available DQS Phase Shifts
0	100-175	12	low (6-bit)	30, 60, 90, 120
1	150-230	16	high (5-bit)	22.5, 45, 67.5, 90
2	200-310	12	high (5-bit)	30, 60, 90, 120

Frequency Mode	Frequency Range (MHz)	Number of DLL Delay Buffers	Delay Buffer Mode	Available DQS Phase Shifts
3	240-400 (C3 speed grade) 240-350 (C4 and C5 speed grades, and HardCopy II)	10	high (5-bit)	36, 72, 108, 144

Stratix, Stratix II PLL Reconfiguration Feature

This issue affects the PLL Reconfiguration feature in Stratix, Stratix GX, HardCopy Stratix, Stratix II, Stratix II GX, and HardCopy II devices. For any non-phase shift changes to properly take effect, the `Areset` signal must be asserted after PLL reconfiguration. For phase-shift changes to take effect, at least three `scanclk` cycles must elapse following PLL reconfiguration. (For more information, see the Errata documents for the affected device families.) The `altpll_reconfig` megafunction now adds state machine logic to generate the needed `Areset` pulse or three `scanclk` cycle delay. Altera recommends that you recompile your design with the new version of the megafunction.

Stratix II PLL Self-reset Feature

This change affects Stratix II, Stratix II GX, and HardCopy II devices. The option for PLLs to reset automatically on loss of lock is supported. This option is enabled in the `altpll` megafunction by selecting **Enable self-reset on loss of lock**. When this option is used, the option to hold the locked output low for a specified number of cycles after PLL initialization must also be used.

Cyclone II PLL Source-synchronous Mode

Source-synchronous PLL operation is supported in Cyclone II devices. This mode is activated in the `altpll` megafunction by selecting the option **Use the feedback path inside the PLL in source-synchronous compensation mode** under Operation mode. You can use it in the `altlvds` megafunction by turning on the option **Use source-synchronous mode of the PLL**. When used with the `altlvds` megafunction, this option improves the receiver sampling window compared to the Normal mode, and is recommended for new designs.

Revision History

Revision	Description
1.0	Initial Release

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