



Quartus II Software Release Notes

June 2006

Quartus II version 6.0 Service Pack 1

This document provides late-breaking information about the following areas of this version of the Altera® Quartus® II software. For information about memory, disk space, and system requirements, refer to the **readme.txt** file in your `\altera\quartus<version number>` directory. For information about device support in this version of the Quartus II software, along with the latest information about timing and power models, refer to the *Quartus II Device Support Release Notes* on the Altera website at **<http://www.altera.com/literature/lit-qts.jsp>**.

New Features & Enhancements	2
EDA Interface Information	2
Changes to Software Behavior	4
Known Issues & Workarounds.....	17
General Quartus II Software Issues	17
Platform-Specific Issues.....	25
Device Family Issues.....	31
Design Flow Issues.....	40
SOPC Builder Issues	44
EDA Integration Issues	45
Simulation Model Changes	47
Latest Known Quartus II Software Issues	50
Revision History.....	50

New Features & Enhancements

The Quartus II software version 6.0 Service Pack 1 includes the following new features and enhancements:

- Design Security enabled for Stratix II device family designs
- Support for mixed protocols and datarates within the same Quad for Stratix II GX devices
- Full device support for Cyclone II devices: EP2C8AF256, EP2C15AF256, EP2C15AF484, EP2C20AF256, and EP2C20AF484
- Full device support for MAX II devices: EPM240F100, EPM240M100, EPM570F100, EPM570M100, EPM570M256, and EPM1270M256

EDA Interface Information

The current version of the Quartus II software supports the following EDA tools.

Supported EDA Tools

Synthesis Tools	Version	NativeLink Support
Synplicity Synplify & Synplify Pro	8.5	✓
Mentor Graphics Precision RTL Synthesis	2005c	✓
Mentor Graphics LeonardoSpectrum	2005b	✓
Synopsys Design Compiler FPGA	2005.09	
Synopsys FPGA Compiler II	3.8	✓
Synopsys Design Compiler	2004.12-SP4	
Magma Design Automation PALACE	2.4	✓
Simulation Tools	Version	NativeLink Support
Mentor Graphics ModelSim	6.1d	✓
Mentor Graphics ModelSim-Altera	6.1d	✓
Cadence NC-Sim (Windows)	5.4 s011	✓
Cadence NC-Sim (UNIX)	5.5 s12	
Cadence Verilog-XL (UNIX)	5.5 s12	
Synopsys VCS / VCS MX	2005.06-SP1	✓
Aldec Active-HDL	7.1 / 7.1 SP1	
Formal Verification Tools (Equivalence Checking)	Version	NativeLink Support
Cadence Encounter Conformal	5.2	
Synopsys Formality	2005.09	

Chip Level Static Timing Analysis	Version	NativeLink Support
Synopsys PrimeTime	2005.12	✓
Board Level Static Timing Analysis	Version	NativeLink Support
Mentor Graphics TAU	3.5	
Board Level Symbol/Pin-out Management	Version	NativeLink Support
Mentor Graphics IO Designer	2005	

Changes to Software Behavior

This section documents instances in which the behavior and default settings of this release of the Quartus II software have been changed from earlier releases of the software.

Items listed in the following table represent cases in which the behavior of the current release of the Quartus II software is different from a previous version.

Description	Workaround
Version 6.0 SP1	
Designs that used the <code>alt2gxb</code> megafunction in PCI Express mode in the Quartus II software version 6.0 and earlier may have output voltage settings that are not within the PCI Express specification.	Use the MegaWizard Plug-In Manager in the Quartus II software version 6.0 SP1 or later to regenerate your <code>alt2gxb</code> megafunction and recompile your design.
In the Quartus II software version 6.0 and earlier, when you created a receiver-only instance of the <code>alt2gxb</code> megafunction, a CMU PLL was created that has <code>p11_inclk</code> and <code>p11_locked</code> ports. These ports prevented the combination of two receiver-only implementations at different data rates in the same quad.	In the Quartus II software version 6.0 SP1, a CMU PLL is no longer created when you create a receiver-only instance. You must recreate the megafunction instance with the MegaWizard Plug-In Manager or manually remove the <code>p11_inclk</code> and <code>p11_locked</code> ports from the wrapper file.
In the Quartus II software version 6.0 SP1 and later, the TimeQuest Timing Analyzer no longer recognizes uppercase pin suffix names in an SDC constraints file.	You must manually change the pin name suffixes to lowercase in your SDC file. For example <code>[get_pins myreg CLK]</code> should be changed to <code>[get_pins myreg clk]</code> .
Version 6.0	
The TimeQuest Timing Analyzer's QSF2SDC conversion utility cannot properly convert all Classic Timing Analyzer timing assignments. The results from the TimeQuest Timing Analyzer may also be different from the Classic Timing Analyzer due to other default behavior differences.	The QSF2SDC conversion utility is considered a guide to help reduce the time to switch to the TimeQuest analyzer, and it is not intended to make the TimeQuest analyzer a plug-in replacement for the Quartus II Classic Timing Analyzer. You should review all converted SDC constraints for correctness and completeness. Refer to the <i>Switching To TimeQuest</i> chapter in the Quartus II Software Handbook for more information.

Description	Workaround
The maximum frequency limit on the calibration block clock in Stratix II GX devices has been lowered from 200 MHz to 125 MHz in this release of the Quartus II software.	Ensure that your calibration block clock frequency does not exceed 125 MHz.
The Quartus II software version 6.0 does not create a Verilog Quartus Mapping File (.vqm) for any Stratix II GX design that contains any GXB-related blocks.	If a VQM is necessary, partition your design so the GXB-related block is in one partition, then create VQMs for the other portions of the design.
The maximum frequency of the GXB – core clock signal for the -5 speed grade of Stratix II GX devices has been lowered from 250 MHz to 200 MHz in this release of the Quartus II software.	If your design requires a GXB – core clock frequency higher than 200 MHz, use a -4 or -3 speed grade device.
For designs that target Stratix II GX devices, that use the alt2gxb megafunction in a transmitter-only configuration, the loop_filter_resistor_control value was not correctly written to the megafunction instance.	Use the MegaWizard Plug-In Manager in the Quartus II software version 6.0 to generate a new instance of the alt2gxb megafunction.
If you created a Verilog Quartus Mapping File (.vqm) for a design containing the alt2gxb megafunction in its XAUI configuration with the Quartus II software version 5.1 SP2 or earlier, the setting for Force Signal Detect was incorrectly set to false.	You should regenerate the alt2gxb instantiation in a XAUI configuration using the Quartus II software version 6.0.
In the Quartus II software version 5.1, the Stratix GX PLL algorithm treated all clock frequencies that were within 0.1% of the requested frequency as equivalent. In version 6.0, the algorithm was improved to prefer clock frequencies that are closer to the desired frequency, and pick only non-exact frequencies if an exact frequency setting is not available or yields unacceptable performance.	If you want the settings chosen by the PLL algorithm in the 5.1 version of the Quartus II software, change the desired frequency in the altpll megafunction wizard to the frequency actually implemented by the Quartus II software version 5.1.
In versions of the Quartus II software prior to 6.0, the software erroneously accepted nested generate/endgenerate statements in Verilog HDL design files. The Quartus II software now correctly flags nested generate/endgenerate statements as an error.	Remove any such statements to eliminate the error. If you have loops within a loop, you need only one generate/endgenerate pair.

Description	Workaround
Beginning in the 6.0 release, the Quartus II Parallel Flash Loader megafunction (<code>altparallel_flash_loader</code>) erases flash memory blocks before programming them.	No action is required.
Results from Design Space Explorer runs are now placed in the <code>./dse</code> directory rather than the <code>./dse/results</code> directory where they were placed in releases prior to 6.0.	Update any scripts that use the <code>./dse/results</code> directory.
The column names “from” and “to” in the Source Assignments panel of the Analysis & Synthesis section of the Compilation Report have changed to “From” and “To” in this release.	If you are accessing the contents of these columns using a script, you must update your script to reflect the change in capitalization, or use a case-insensitive search.
Beginning in the 6.0 release, the Quartus II integrated synthesis handles bidirectional pins differently. For example if <code>bidir1</code> and <code>bidir2</code> are declared as <code>inouts</code> , the assignment <code>bidir1 <= bidir2</code> creates a directional connection in which data flows from <code>bidir2</code> to <code>bidir1</code> . In the Quartus II software version 5.1 and earlier, a bidirectional connection was created.	If your design requires that data flow in both directions, you must directly connect the bidirectional pins together without using an assignment statement. Assignment statements always produce a unidirectional data flow.
In versions of the Quartus II software prior to 6.0, the software incorrectly merged PLLs when they were set to different operating modes.	Beginning in version 6.0, you cannot merge PLLs that are in different operating modes unless you use the Ignore PLL mode when merging PLLs assignment.
In versions of the Quartus II software prior to version 6.0, the output clock division factors (outclock_divide_by) were incorrectly reported by a factor of 2, when the <code>altlvds</code> megafunction was implemented in LEs (such as in Cyclone and Cyclone II families).	

Description	Workaround
<p>The following changes were made to menu commands and their locations in this release:</p> <p>Project menu</p> <ul style="list-style-type: none"> • Generate Bottom-Up Design Partition Scripts (new feature) • Organize Quartus II Settings File (new feature) <p>Assignment menu</p> <ul style="list-style-type: none"> • Timing Analysis Settings (was Timing Settings) <p>Processing menu</p> <ul style="list-style-type: none"> • Start TimeQuest Timing Analyzer (new feature) • Update Memory Initialization File (new feature) • Compiler Tool (moved from Tools menu) • Simulator Tool (moved from Tools menu) • Timing Analysis Tool (moved from Tools menu) • PowerPlay Power Analyzer Tool (moved from Tools menu) <p>Tools menu</p> <ul style="list-style-type: none"> • TimeQuest Timing Analyzer (new feature) • Advisors (all Advisors moved to sub-menu) • Netlist Viewers (all netlist viewers moved to sub-menu) • SignalProbe Pins (was in Settings dialog box) 	
<p>The method the Quartus II NativeLink interface uses to locate other EDA tools changed in this release. You might receive a message indicating that the tool cannot be found when you launch it through the NativeLink interface.</p>	<p>You must specify the path to the EDA tool program file on the EDA Tool Options page of the Options dialog box, or with the <code>set_user_command Tcl</code> command.</p>
<p>The maximum data rate for receive-only configurations of the <code>alt2gxb</code> megafunction were not correctly checked in versions of the Quartus II software prior to 6.0.</p>	<p>You must recompile your design in the Quartus II software version 6.0 or later.</p>

Description	Workaround
Version 5.1 SP2 and earlier	
<p>Beginning with version 5.1, implicit or explicit declarations inside unnamed generate blocks are no longer visible outside the generate block.</p>	<p>Declare the object outside the generate block. You can also add a name to the generate block and refer to the object with a hierarchical name.</p>
<p>The following primitives now use a new library instead of the altera_mf library:</p> <p>CARRY CARRY_SUM CASCADE CLKLOCK EXP GLOBAL LUT_INPUT LUT_OUTPUT ROW_GLOBAL TRI SOFT OPNDRN DFF DFFE DFFEAS JKFF JKFFE DFFEAS LATCH SRFF SRFFE TFF TFFE ALT_INBUF ALT_IOBUF ALT_OUTBUF ALT_OUTBUF_TRI .</p>	<p>To perform functional simulations in Verilog HDL, you must use the altera_primitives.v library located in the <Quartus II installation directory>\eda\sim_lib directory. For VHDL, you must use the altera_primitives.vhd library located in the <Quartus II installation directory>\eda\sim_lib directory. The VHDL component declaration file is located in the altera_primitives_components.vhd library in the <Quartus II installation directory>\eda\sim_lib directory.</p>
<p>The frequency limit on the PLL reference clock on Stratix GX devices changed to 640 MHz.</p>	<p>To take advantage of the new setting, change your design and recompile after installing the Service Pack.</p>
<p>Designs compiled with the Quartus II software version 5.0 and earlier could fail their boundary-scan test (BST) if the test expected all input buffers to be active after device configuration. Under some circumstances, unused input buffers are disabled by the Quartus II software to minimize power usage in Stratix II, Cyclone II, and MAX II device families.</p>	<p>Beginning in version 5.0 Service Pack 1, the Quartus II software supports the always_enable_input_buffers option to prevent unused input buffers from being disabled during configuration.</p>

Description	Workaround
The Quartus II software version 5.0 and earlier did not correctly enforce the Fitter rule that there must be one row of separation between dynamic phase alignment (DPA) channels to prevent interference.	Beginning in version 5.0 Service Pack 1, the Quartus II software gives a critical warning of this condition if the maximum data rate is between 701 MHz and 1 GHz and an error if the data rate is 1GHz and above. If you receive such warning, reassign your DPA channels to have one row of separation between them.
The Quartus II software version 5.0 and earlier incorrectly permitted the VCCIO voltage of an I/O bank that contains On-Chip Termination RUP and RDN pins to be different from the VCCIO of the associated I/O standard on Stratix II devices.	Beginning in version 5.0 Service Pack 1, the Quartus II software requires that the voltage assignments be the same. This restriction may cause designs that fit using the Quartus II software version 5.0 to not fit when compiling after installing Service Pack 1.
The data_out[] bus signals from the <code>altremote_update</code> megafunction are incorrectly inverted in the Quartus II software version 5.0. This condition is corrected in version 5.0 SP1.	Recompile your design after installing the Quartus II software version 5.0 Service Pack 1.
The settings for Stratix II PLLs are updated in the Quartus II software version 5.0. The changes reflect the allowable settings for the PLL resulting from device characterization.	
The Quartus II software version 5.0 SP1 no longer supports use of the HyperTransport I/O standard on clock inputs and outputs on Top Edge and Bottom Edge pins.	
The Quartus II software version 5.0 and later supports Comma-Separated Value files (.csv) for using the PowerPlay Early Power Estimation spreadsheet with Stratix II and Cyclone II devices.	
You cannot use the Quartus II stand-alone Programmer to erase devices when you are using JAM files (.jam) or Jam Byte Code files (.jbc).	

Description	Workaround
<p>Some designs that compiled without error in the Quartus II software version 4.2 and earlier may cause an error similar to the following example to be displayed, when compiled in the Quartus II software 5.0 and later:</p> <pre>Error: Fast PLL DPA-mode channels span rows 2 to 28, but location assignment of LVDS DPA-mode SERDES driven by PLL altlvds_rx:altlvds_rx_component lvds_rx_9p31:auto_generated pl l is not within 25 from driving fast PLL</pre>	<p>Remove your pin assignments and recompile the design with the Quartus II software version 5.0 or later.</p>
<p>The Quartus II software version 5.0 corrects a previous problem in which the Cyclone and Cyclone II CRC configuration oscillator was shown to run at 100 MHz rather than the 80 MHz rate correctly shown in the device family handbooks.</p>	
<p>In the Quartus II software version 5.0 and later, you can assign the Allow XOR Gate Usage logic option to individual nodes and entities. In previous versions, you could apply this logic option only to the entire design (that is, it was a global logic option).</p>	
<p>In the Quartus II software version 5.0 and later, if your Quartus II Settings File (.qsf) contains an error, you cannot compile the project until the error has been corrected. In previous versions, a warning message was displayed and compilation continued.</p>	
<p>In the Quartus II software version 5.0 and later, the <code>\altera\qdesigns<version number>\ll_makefile</code> directory has been replaced by the the <code>\altera\qdesigns<version number>\logiclock_makefile</code> directory.</p>	
<p>The <code>altgxb</code> megafunction has been updated in the Quartus II software version 5.0. Any Stratix GX project that used the <code>altgxb</code> megafunction and was archived with the Include functions from system libraries option turned on will not compile correctly.</p>	<p>You must delete the <code>altgxb.tdf</code> file that is included in the project archive, and recompile your design.</p>

Description	Workaround
<p>The Quartus II software version 5.0 and later does not support Advanced NativeLink integration with the Synopsys VCS MX software.</p>	
<p>For all Stratix GX devices, a change has been made to the PLL settings in the gigabit transceiver blocks, which results in a reduction of total jitter for a specific data rate range. If your design has a data rate in the range of 1.01 Gbps to 1.25 Gbps, recompiling your design in the Quartus II software version 5.0 and later will result in a reduction in Total Transmit Jitter by ~35%.</p>	
<p>In the Quartus II software version 4.2 SP1 and later for UNIX and Linux workstations, the Copy command is disabled when the RTL Viewer, Technology Map Viewer, and certain Report window panes are open.</p>	

Description	Workaround
<p>SOPC Builder systems using an Avalon™ Tri-State Bridge may fail to compile after upgrading to the Quartus II software version 4.2 and later due to an address width mismatch.</p>	<p>In the Quartus II software versions 4.1 and earlier, SOPC Builder created an extra most-significant-address bit for registered slave peripherals (also called native peripherals) connected to an Avalon Tri-State Bridge. If this bridge has only native slave devices connected to it, then some designers may have connected this extra address bit in their design to a peripheral. This extra address bit no longer exists if the embedded system is regenerated using the Quartus II software version 4.2 and later. If a design uses the extra address bit and the Quartus II software is upgraded to version 4.2 and later, a compilation error will occur due to the most significant address bit not being connected. This issue can be corrected without the need to modify software or hardware interconnects. If the peripheral affected by this issue is connected to an interface to user logic, then increasing the address width by one (in the interface to user logic) will correct the issue. If the peripheral affected by this issue is a custom component, edit the class.ptf file for that component by increasing the value called Address_Width by one.</p>
<p>For MAX 7000S family devices, the Quartus II software version 4.2 and later reports unused I/O pins as RESERVED by default, or as RESERVED_INPUT if the setting Reserve all unused pins as inputs, tri-stated is selected. Previous versions report unused I/O pins as GND*, which is incorrect for MAX 7000S family devices.</p>	<p>To generate a correct Pin-Out File (.pin), recompile any MAX 7000S designs that were created in earlier versions of the Quartus II software.</p>

Description	Workaround
<p>The Quartus II software version 4.2 and later prohibits the placement of the IOE registers within the same LAB row as a SERDES RX or TX channel. IOE registers must be placed at least one LAB row away from an RX or TX channel. The Quartus II software version 4.1 SP2 and earlier does not prohibit the use of IOE registers in the same LAB row as a receiver (RX) or transmitter (TX) channel that utilizes the SERDES block.</p>	<p>Recompile any Stratix II design that was created in an earlier version of the Quartus II software with the current version. The setup time of the register (t_{SU}) will increase if the IOE register is moved to the PLD core. It is up to the designer to ensure that all setup times are met. Contact Altera Applications for more details.</p>
<p>The Tcl Console Window is disabled while a compilation or simulation flow is in progress. This behavior is necessary to prevent inadvertent changes to settings files during compilation.</p>	<p>Wait until compilation or simulation is complete before trying to run a Tcl command in the Tcl Console.</p>
<p>The <code>p11</code> megafunction has been removed from the Quartus II software version 4.2 and later. This megafunction implemented a digital PLL in logic cells, and was maintained for backward compatibility only.</p>	<p>If you wish to still use the <code>p11</code> megafunction rather than the <code>altpll</code> or <code>altclklock</code> megafunctions, you must copy the <code>pll.inc</code> and <code>pll.tdf</code> files from the <code>/<Path to Quartus II installation>/mega</code> directory of a previous version and place them in the same directory of the current version.</p>
<p>The PLLs in Stratix, Stratix II, and Stratix GX device families no longer support delay shift (time delay elements).</p>	<p>Altera recommends using the phase shift feature of the <code>altpll</code> megafunction to implement time shifts.</p>
<p>The Quartus II software version 4.2 and later no longer supports the <code>-entity</code> option for the <code>LL_IMPORT_FILE</code> assignment.</p>	<p>You must make the <code>LL_IMPORT_FILE</code> assignment for each instance of the entity to which you want to make the assignment.</p>

Description	Workaround
<p>In the Quartus II software version 4.2 and later, the RAM atom simulation models have changed in the following ways:</p> <ol style="list-style-type: none"> 1. In the Quartus II software version 4.1 and earlier, all ports on the RAM atom had fixed widths (data port width=144, address port width=16, and so on). Starting in version 4.2, the widths of all ports are parameterized. 2. The default port width in the simulation model is 1 (that is, if an input is not used, it is assumed that the width of that input is 1). 3. Instead of using parameters such as MEM1,..., MEM9 to hold initialization data for RAM, two parameters called “MEM_INIT0 and MEM_INIT1” are used. The MEM_INIT0 parameter holds lower bytes of initialization data in increasing order of address up to a maximum of 2048 bits. The MEM_INIT1 parameter holds the remaining upper bytes. 	<p>You must recompile your project in the Quartus II software version 4.2 or later to generate new Verilog Output files (.vo) or VHDL Output files (.vho) for the simulation tool.</p> <p>If your design runs at a clock speed of greater than 500 MHz, you must set the simulation resolution to picoseconds (ps).</p>
<p>The Quartus II software no longer uses the registry to store non-user interface-related settings. Non-user interface-related settings are stored automatically in the quartus2.ini file when you open the Quartus II software user interface for the first time.</p>	<p>You must open the Quartus II software user interface at least once before using the command-line version of the software.</p>
<p>The following Tcl simulator commands are no longer supported by the Quartus II software version 4.0 and later:</p> <ul style="list-style-type: none"> • dbg • get_time • get_value • force_value • release_value • read_memory • write_memory • run • print • get_memory_width • get_memory_depth • testbench_mode 	<p>There are new versions of most of these commands in the ::quartus::simulator package, which is available in the quartus_sim.exe module. Refer to the Quartus II Command-Line and Tcl API Help for more details. To view Tcl online Help type the following command at a command prompt:</p> <pre>quartus_sh --qhelp <Enter></pre>

Description	Workaround
<p>When you instantiate a new RAM or ROM function with the MegaWizard® Plug-In Manager, the outputs of the memory function will be registered using the same clock as the inputs, by default. This is a change of behavior in that the Quartus II software versions earlier than version 4.0, the outputs are not registered by default.</p>	<p>This is a change of behavior that affects only new instantiations of RAM or ROM function. Existing memory functions are not affected.</p>
<p>In the Quartus II software version 3.0 and earlier, LogicLock™ assignments are stored in lowercase. In version 4.0 and later, designs written in case-sensitive languages may require that LogicLock assignments be in mixed case. Due to the difference in case-sensitivity between versions, LogicLock assignments made in the Quartus II software version 3.0 and earlier may not be usable in the Quartus II software version 4.0 and later.</p>	<p>Do not use uppercase or mixed case in your HDL design files.</p>
<p>When you are using formal verification tools with a design that contains LogicLock regions that was compiled with the Quartus II software version 3.0 or earlier, under certain circumstances when you open the design in the Quartus II software version 4.0 and later, the LogicLock regions will not be handled properly.</p>	<p>Redefine the LogicLock regions in the Quartus II software version 4.0 or later to eliminate the errors.</p>
<p>In the Quartus II software version 4.0 SP1 and later, the labeling of unused GXB_TX and GXB_RX pins has changed.</p>	<p>Pins previously labeled GXB_VCC+ are now labeled GXB_VCC*. Pins previously labeled GXB_GND+ are now labeled GXB_GND*.</p>
<p>The behavior of the Quartus II Fitter has been modified to minimize compilation time when there are no timing constraints applied to the design. This change in behavior results in an average of 40% faster compilation times and an average of 15% slower f_{MAX} performance. This change to the Fitter behavior applies only when you select the Auto Fit option for Fitter Effort on the Fitter Settings page of the Settings dialog box, and affects only Stratix, Stratix GX, Stratix II, Cyclone, and Cyclone II device families.</p>	<p>To return to the same behavior as earlier versions of the Quartus II software, select Standard Fit under Fitter Effort on the Fitter Settings page of the Settings dialog box, or apply appropriate timing constraints.</p>

Description	Workaround
<p>The following megafunctions have clear box models that contain assignments that are not stored in the Quartus Settings File (.qsf) and are not written out to a Verilog Quartus Mapping File (.vqm):</p> <pre> altdqs altdq altddio_bidir altddio_out altddio_input altlvds_rx altlvds_tx altufm_i2c dcfifo alt2gxb_reconfig </pre>	<p>Do not save your atom netlist file as a Verilog Quartus Mapping file if you are using these megafunctions.</p>
<p>The following megafunctions now use clear box models instead of the generic model libraries:</p> <pre> altmemmult altufm altdq altdqs altremoteupdate altpll_reconfig altclkctrl </pre>	<p>When you are simulating a design that uses one of these megafunctions, you must use the family-specific atom model library (such as stratix_atoms.v) instead of the generic altera_mf.v (or .vhd) library.</p>

Known Issues & Workarounds

General Quartus II Software Issues

Issue	Workaround
Version 6.0 SP1	
When evaluating a Tcl script in the TimeQuest Timing Analyzer, calling <code>exit</code> before deleting the timing netlist may result in a Internal Error.	Delete the timing netlist and close the project before exiting TimeQuest using the commands <code>delete_timing_netlist</code> and <code>project_close</code> .
Running multiple instances of the Quartus II software using the same Quartus Project File (.qpf) may cause unpredictable results or may cause the Quartus II software to crash.	Altera recommends that you not open multiple instances of the Quartus II software using the same project.
Version 6.0	
In the classic Timing Analyzer, when a clock (base or derived) is assigned to an internal register, then data paths to and from the register are not analyzed for clock setup and clock hold analysis.	First, analyze the design with the clock settings assigned to the internal registers. Then remove the clock settings from the internal registers and perform a second analysis, checking only paths to and from those registers.
If you change an I/O primitive assignment or an <code>altera_attribute</code> assignment, or any assignment made in a Verilog HDL or VHDL design file, the assignment may not be applied to the design database correctly in the next compilation.	Delete the <code><project>\db</code> directory and recompile the design.
Assignments made to I/O primitives in lower-level partitions are not honored at the top level in a Bottom-Up Incremental Compilation flow.	Do not use I/O primitives in a Bottom-Up Incremental Compilation Flow.
In the TimeQuest Timing Analyzer, report timing accounts for clock setup uncertainty or clock hold uncertainty on paths affected by the <code>set_max_delay</code> and <code>set_min_delay</code> timing exceptions, but the clock domain summaries (for example, Report Setup Summary) do not account for uncertainty.	Use report timing to verify worst-case slacks for each analysis (setup, hold, recovery, and removal).

Issue	Workaround
<p>If you assign a value of less than 3 to the instruction register width parameter (SLD_IR_WIDTH) in the <code>sld_virtual_jtag</code> megafunction, the VHDL simulation model will be incorrect and may cause simulation to fail. The Verilog HDL model is also incorrect and the simulation will complete, but with incorrect results.</p>	<p>Set the <code>SLD_IR_WIDTH</code> parameter to a value greater than 3 for simulation. After simulation and before final synthesis, use the MegaWizard Plug-In Manager to set the parameter to the value you want.</p>
<p>The SignalProbe dialog box may take a long time to open, so it appears that the Quartus II software is “hanging.” The delay is dependent upon the size of the netlist and the number of device pins.</p>	<p>Do not open the SignalProbe dialog box while a compilation is in progress.</p>
<p>The TimeQuest Timing Analyzer erroneously analyzes paths to the asynchronous data pins of registers (that is, the <code>adata</code> pin) during a recovery/removal analysis.</p>	<p>Apply the <code>set_false_path</code> command from the asynchronous data signal’s source port or register to declare these paths as false paths.</p>
<p>Under some circumstances, your web browser software may fail to launch correctly from the IP MegaStore MegaWizard Plug-In Manager. The web browser defined in the MegaWizard Plug-In Manager for the IP MegaStore inherits the environment settings from the Quartus II software. Specifically, the <code>LD_LIBRARY_PATH</code> environment variable may contain entries that conflict with web browsers such as FireFox, preventing them from starting correctly.</p>	<p>Edit the script that launches the web browser to make sure the Quartus II directories are the last entries in the <code>LD_LIBRARY_PATH</code> variable.</p>
<p>If you change the type of a parameter setting in the Quartus II Settings File (<code>.qsf</code>) or a Block Design File (<code>.bdf</code>) and recompile your design, your change appears to have no effect. The type of a parameter is denoted by appending a prefix such as “B” (binary), “D” (decimal). For example, B“10101” represents the binary string “10101”, but D“10101” represents the decimal number 10101.</p>	<p>Delete the <code><project>\db</code> directory and recompile the design.</p>

Issue	Workaround
Version 5.1 SP2 and earlier	
Due to a limit of the Windows operating system, path names longer than 229 characters can cause an internal error in the Quartus II software.	Make sure that all path names do not exceed 229 characters. This limitation applies to UNIX and Linux installations also.
When you are using the Chip Editor to delete the connections in carry chains, the destination node must be in a legal location for the carry chain. If this is not the case, you will not be able to undo the operation or any prior operations.	Perform the following steps: 1. Delete the Remove-Chain command in the Change Manager. 2. Move the node back to its legal position. 3. Recreate the chain in the Resource Property editor. 4. Move the node to the desired position.
The Quartus II archive feature does not correctly archive files that have duplicate file names, even when they are in different directories. This failure can cause compilation failures when you are using the distributed processing feature of Design Space Explorer (DSE).	Make all design file names unique.
If your design contains illegal pin assignments, and you open the Resources window in the Pin Planner, the Quartus II software may crash.	Remove any illegal pin location assignments before opening the Resources window.
If you make a single-point CUT=ON assignment to a node, and then override it with a point-to-point CUT=OFF assignment on a specific path, the OFF assignment will not be honored.	
Under certain circumstances the Design Assistant reports Critical Warnings (that locate to the <code>altlvds_rx</code> or <code>dcfifo</code> megafunction) for your project, which uses the <code>altvds_rx</code> or <code>dcfifo</code> megafunction or an IP core that uses the <code>altvds_rx</code> or <code>dcfifo</code> megafunction.	These warnings can be safely ignored; no action is necessary.
You may receive a "License not found..." error if the path to the license file contains non-ASCII characters.	Change or remove any non-ASCII characters from the license file path.

Issue	Workaround
<p>During a SignalProbe™ compilation, you might receive warning message(s) similar to the following example: “Routing constraints for signal <signal_name> seem to be causing unresolvable routing congestion. The constraints for the signal were removed.”</p>	<p>The Compiler issues these warnings when it is unable to retain the routing constraints from a previous compilation because those routing resources were needed by the SignalProbe signal routing.</p>
<p>There is no distinction between output ports and bidirectional ports in AHDL Function Prototypes; instead, all ports listed after the RETURNS keyword are treated as output ports. As a result, if you specify a bidirectional port in a logic function’s Function Prototype Statement and do not connect the port to a top-level bidirectional pin or to other logic in the design where you instantiate the logic function, an error can occur.</p>	<p>Connect the port to a top-level bidirectional pin or to other logic in the design.</p>
<p>Context-sensitive Help is not available for some items in the Quartus II software.</p>	<p>To locate Help on those items, click Search on the Help menu, and type the name of the item.</p>
<p>The Classic Timing Analyzer does not recognize non-PLL clock signals when using any PLL megafunction.</p>	<p>Make clock settings assignments to all non-PLL clocks.</p>
<p>The Waveform Editor does not allow you to create a bus with nodes that are nonconsecutive members of a bus.</p>	<p>Create buses only with nodes that are consecutive members of a bus. Or, use the Group command on the Edit menu to create groups of arbitrary nodes.</p>
<p>If you are using the altcam, altclklock, altlvds_rx, or altlvds_tx megafunctions, the equations shown in the Equations Section of the Compilation Report are not complete.</p>	<p>To view the complete equations for any of these megafunctions, use the Equations window of the Timing Closure Floorplan.</p>
<p>The Quartus II software does not support design file names with more than one extension. For example, you cannot use the file name file.eda.edif.</p>	<p>Use design file names with only one extension.</p>

Issue	Workaround
If you install the Quartus II software for PCs on a UNIX server that exports shares with the Samba software version 1.9.18p10, you may experience problems accessing project files that are also on the network.	Altera recommends using version 1.9.16p11 or 2.0 of the Samba software.
If you make assignments to reserve pins as a group or with group notation (debug [7 . . 0]), the Quartus II software does not correctly generate simulation output files, and you receive a warning message saying “Unsupported data type in the top-level module.”	Reserve the pins using single-name notation (for example, debug [7] , debug [6] , and so on).
Do not change the file permissions (such as changing “read-only” to “read and write”) of Quartus II Settings File (.qsf) and Quartus II Project File (.qpf) while a Quartus II project is open.	Close the Quartus II project before making changes to the file permissions.
Node names containing numbers greater than 2 ³¹ -1 (2147483647) will cause an Internal Error in the Quartus II software.	Do not use node names containing large numbers.
Occasionally the Programmer does not allow you to use a MAX 7000AE Programmer Object File (.pof) with a MAX 7000AE device. This error sometimes occurs after a compatible MAX 7000B device is used with the MAX 7000AE POF.	Do not switch between compatible MAX 7000B and MAX 7000AE devices when a MAX 7000AE POF is loaded, or reload the MAX 7000AE POF.
Routing back-annotation may fail if the back-annotated locations do not match the location assignments in the Quartus II Settings File (.qsf) or if the location assignments are missing. This problem can occur if you change devices, or if you remove some location assignments by using the Assignment Editor on the Assignments menu or by manually editing the Quartus II Settings File.	If you experience a “no fit” or an Internal Error while using routing back-annotation, delete the Routing Constraints File (.rcf) and back-annotate the design again after a successful compilation.
Occasionally, the Quartus II software may crash or hang with no error message immediately upon opening a project.	Delete the Quartus II Workspace File (.qws) <project name>.qws from the project directory. If the problem persists, delete the \<project directory>\db directory and recompile the design.

Issue	Workaround
When you are setting phase shift and duty cycle values for clock signals using the <code>altpll</code> megafunction, some combinations of settings may result in values that cannot be synthesized exactly. Under certain circumstances, the Quartus II software attempts to synthesize the phase shift parameter before the duty cycle parameter.	You should first select values for the parameter (phase shift or duty cycle) that is most important for your design.
During compilation or simulation, the Quartus II software may “hang” and not proceed to the next module if a menu or modal dialog box is open at the time the current module finishes running.	Close any open menus or modal dialog boxes before the compilation or simulation reaches the next stage.
Running individual Quartus II software executables (quartus_map , quartus_fit , and so on) from within the Quartus II Tcl Console may cause the Quartus II software to crash.	Run individual executables either from within the Quartus II scripting shell (quartus_sh) or directly at a command prompt.
If you have chosen migration devices in the Compatible Migration Devices dialog box, which is available from the Device page in the Settings dialog box on the Assignments menu, the Timing Closure floorplan displays only the pins and PLLs that are common to all the selected devices. However, the Chip Editor displays all the pins and PLLs available for the device specified for compilation.	
The time shown in the Status window may not agree with the processing times reported in the Compilation Report. This difference is due to differences in how the times are calculated during processing.	
If you type a name in the entity column of the Assignment Editor that differs from an existing name only by case, the Assignment Editor’s “auto-completion” feature always uses the existing name.	Type the new entity name in another application, such as a text editor, copy it to the clipboard, and paste the name from the clipboard into the Assignment Editor.
Altera recommends that you do not use node or entity names that differ only by case if you are using the Quartus II Simulator or Waveform Editor.	

Issue	Workaround
Under certain circumstances, a design that uses Virtual Pin assignments may fail to fit after back-annotation. This situation occurs because the clock signals chosen automatically for the first compilation do not match those chosen for the second compilation.	Manually assign your clock signals, using Virtual Pin Clock assignments before the first compilation, or use Advanced Back-Annotation to explicitly write out the virtual clock assignments before the second compilation.
If you use the <code>dcfifo</code> or <code>scfifo</code> megafunctions in an AHDL design, you may receive an error message similar to “The parameter <code>LPM_WIDTHU</code> has been set to an invalid value...”	Either remove the <code>LPM_WIDTHU</code> parameter arguments from your AHDL <code>dcfifo</code> or <code>scfifo</code> megafunction instantiation, or explicitly set the <code>LPM_WIDTHU</code> parameter to <code>ceil(log2(LPM_NUMWORDS))</code> .
Do not open, change permissions, or delete the <code><project directory>/db</code> directory or any file therein while any Quartus II executable is running.	
If you are using the IP Toolbench and add a user library, the Quartus II software may add a backslash (\) to the end of the library file name. The Quartus II user interface ignores this trailing backslash.	
Support for non-decimal radix numbers (such as hexadecimal) used as constants in the <code>lpm_constant</code> , <code>lpm_compare</code> , and <code>lpm_add_sub</code> megafunctions is limited to values that can be represented by 31 bits or fewer.	For values that require more than 31 bits, use decimal radix only.

Issue	Workaround
<p>Under certain circumstances, back-annotation of routing in unreserved LogicLock regions can cause unsatisfiable routing constraints for signals going to clock and clock-enable ports of LABs. This can occur when other portions of the design are not back-annotated, and the Fitter populates empty LCELLs in the back-annotated LogicLock region during subsequent compilations.</p> <p>For example, assume that on the initial compilation, LogicLock region L contains register A, which uses the CLK1 and ENA1 ports of a LAB. When the design is recompiled, the Fitter may place register B, which is not part of region L, and uses the SLOAD input, in the same LAB as register A (assuming that the LAB has sufficient empty space to accommodate it).</p> <p>The LAB control signal generation block does not allow use of both ENA1 and SLOAD in the same LAB; therefore, register A must use the CLK0 and ENA0 ports, rather than CLK1 and ENA1. To avoid a no-route situation, the Fitter will ignore the routing constraints for the clock and enable signals, and re-route the signals using the appropriate control signal multiplexing for the CLK0 and ENA0 ports of the LAB. The Fitter picks the most appropriate routing and, in the majority of cases, the circuit's timing is not adversely affected. When the Fitter is forced to ignore routing constraints, info messages of the form "Info: Can't route signal <name> to atom <name>" are displayed to inform the user; the appearance of such messages is not a cause for alarm.</p>	<p>This situation can be avoided entirely by marking all LogicLock regions as Reserved, thereby preventing the Fitter from placing new items in a region. The tradeoff, of course, is that should a Reserved LogicLock region be under-utilized, the Fitter will be unable to place other logic items in the unused portion of the region.</p>

Platform-Specific Issues

Windows Platforms Only

Issue	Workaround
Version 6.0	
If you are running the Quartus II software on the Windows XP64 operating system, the software may “hang” when the Text Editor is opened.	You must end the quartus.exe process in the Process tab of the Windows Task Manager, delete all the files in your %TEMP% directory, and restart the Quartus II software.
If you are running the Quartus II software on the Windows XP64 operating system with a USB Software Guard, you may receive a message that there is no license found.	You must install the Sentinel driver for the Software Guard by browsing to the quartus/drivers/sentinel/win_xp64 directory when asked for the location of the driver.
Version 5.1 SP2 and earlier	
The introduction of Microsoft Security Update MS05-026 prevents the proper display of Quartus II Help across a network.	To properly display HTML Help files, you must access them from a local PC. If you are unable to access Help files locally, go to Microsoft Knowledge Base Article 896054 (support.microsoft.com/?kbid=896054) for more information about possible workarounds.
The keyboard accelerators (underlines) for Alt+ key combinations do not appear in the Quartus II user interface until the Alt key is pressed the first time.	This behavior is a Windows 2000 user-specified preference. To change to the previous behavior, follow these steps: <ol style="list-style-type: none"> 1. On the Start menu, click Control Panel 2. Click Display properties 3. Click the Appearance tab 4. Click Effects 5. Turn off "Hide underlined letters for keyboard navigation until I press the Alt key"
If you use Windows 2000 as a software server to serve the Quartus II software to a client computer running Windows XP, running the Quartus II software on the Windows 2000 server at the same time clients are running the Quartus II software, will cause the Quartus II software on the server to crash.	Do not run the Quartus II software on the Windows 2000 server.

Issue	Workaround
You cannot access the web-based PowerPlay Early Power Estimator on the Altera web site if you have installed Windows XP SP2 because the service pack blocks the active content.	Refer to the Altera Knowledge Database on the Altera web site for more information on enabling your browser to access the PowerPlay Early Power Estimator spreadsheets.
Some dialog box title bar text is not displayed correctly when the Quartus II software is installed on a computer running the Chinese version of Windows XP.	Change the font in the Active Title Bar section of the Windows Appearance Control Panel .
<p>If you do not have Administrator privileges when you install the Quartus II software, certain features of the software, particularly the online Help, will not work properly, for example:</p> <ul style="list-style-type: none"> • Software guards (parallel and USB) • Programming with JTAG server 	Altera recommends that you have Administrator privileges when installing the Quartus II software.
Under certain circumstances, the Quartus II installation program may crash or you may receive an error message immediately upon launching the installation program.	<p>Reinstall the stdole32.tlb file from the original Windows distribution disks. To reinstall the file, type the appropriate command at a command prompt. (Note: the command must be typed on one line.)</p> <p>Windows 2000: <CD-ROM drive letter>:\i386\expand.exe stdole32.tl_ %SystemRoot%\System32\stdole32.tlb <Enter></p> <p>Windows XP: <CD-ROM drive letter>:\i386\expand.exe stdole32.tl_ %SystemRoot%\System32\stdole32.tlb <Enter></p>
If the full, hierarchical name of an instance exceeds 247 characters, it may not be displayed properly in the Quartus II user interface. This problem occurs most often with EDIF netlist files generated by other EDA synthesis tools.	Limit the full, hierarchical instance name to fewer than 247 characters if possible.

Issue	Workaround
If you are running the Quartus II software from a network server, the Quartus II software will not run properly on the client computer if you share the <code>\quartus\bin</code> directory.	You must share the <code>\quartus</code> directory, not the <code>\quartus\bin</code> directory.
The Quartus II software is not compatible with the MATLAB web server.	Turn off the MATLAB web server in the Services Control Panel on the Start menu before running the Quartus II software.
Under some circumstances, the Quartus II splash screen appears and the Quartus II icon appears in the Taskbar, but the graphical user interface does not appear. Under other circumstances, the user interface appears but windows and/or toolbars do not appear correctly.	The registry settings controlling the position of the Quartus II windows may have become corrupted. If the user interface appears, click the Reset All button on the Toolbars page of the Customize dialog box, or, if the user interface does not appear, type the following command at a command prompt: <code>quartus -reset_desktop <Enter></code>
If you install the stand-alone Quartus II Programmer and the Quartus II software, and then uninstall either one, the Programmer may report “JTAG Server -- internal error code 82 occurred” when you click the Add Hardware button in the Hardware Setup dialog box on the Edit menu. This error occurs because uninstalling the software has disabled the JTAG Server service.	Manually restart the JTAG Server service by locating the <code>jtagserver.exe</code> program and at a command prompt for that directory, type <code>jtagserver --install <Enter></code>
If you choose to uninstall a previous version of the Quartus II software during installation, and there is a “locked” file or directory, the installation program will not reboot the computer as is necessary to successfully complete the installation.	Exit from the installer and reboot the computer manually after the removal of the previous version is complete, before completing the installation of the new version.
The Quartus II software version 4.2 and later does not allow a Parallel Port Software Guard (T-guard or dongle) to be used on the same parallel port as a ByteBlaster™ II download cable.	Use another download cable, such as a USB-Blaster™ or MasterBlaster™ to configure your device, or use separate parallel ports for the Software Guard and the download cable. The Quartus II Programmer is not a licensed feature, so you can remove the Software Guard to program your device, but you must replace it to use any other Quartus II software features. You can also use the USB Software Guard.

Issue	Workaround
During installation of the Quartus II software, when you insert the ModelSim-Altera CD-ROM, a Windows Explorer window may appear.	Close the Windows Explorer window before proceeding with the installation.

Solaris & Linux

Issue	Workaround
Version 6.0	
When using the TimeQuest Timing Analyzer Graphical User Interface, occasionally when sourcing a script or generating several report panels in rapid succession (for example, the “Macros” in the Task pane), the user interface may not display any report data at all, or the report data may be old or incomplete. On Linux, the GUI may crash completely. This is due to UNIX file systems not synchronizing between when the user interface reads the report file while the report panels are being generated. The problem is worse with large reports and on slow file systems (for example across a slow network).	Generate only one individual report panel at a time manually from the GUI. This gives the TimeQuest analyzer a chance to finish generating the report panel before the GUI reads and displays it.
Performing any operation on a flash memory connected to a MAX II device used in a Parallel Flash Loader configuration scheme may cause the Quartus II software to crash with an internal error.	Use a Windows-based computer to configure devices used in a Parallel Flash Loader configuration scheme.
While any shortcut menu is open from an undocked dockable window, if you right-click in the title bar, then all activity in the title bar (left-click and drag, right click context menu, 'X' close button) stops working.	Display a shortcut menu again and perform any action except right-clicking in the title bar to restore normal operation.
Version 5.1 SP2 and earlier	
If the operating system crashes, and the file system in \$TMP is rebuilt automatically, the data in the \$TMP/Mw_<user ID> file is corrupted, the Quartus II software may fail to start correctly.	Delete the \$TMP/Mw_<user ID> file and restart the Quartus II software.

Issue	Workaround
If you are using the Exceed X server software for Windows while running the Quartus II software, the font size may be larger than the line height. This problem occurs most often if you installed the Exceed software while running at a screen resolution greater than 1024 × 768.	Reinstall the Exceed software while running at a screen resolution of 1024 × 768. You can then switch back to your normal, higher resolution setting.
Under some circumstances, there may be editor windows listed on the Window menu that you cannot see.	To display the hidden windows, click Cascade on the Window menu.
You cannot launch the AXD Debugger software from within the Quartus II software.	Launch the AXD Debugger software from outside the Quartus II software.
Under some circumstances, the Internet connectivity features of the Quartus II software are not functional.	Specify the full path to your web browser software on the Internet Connectivity page of the Options dialog box. If you access the Internet through a proxy server, you must also specify the address of the proxy server and its port number.
Under some circumstances you cannot access the Quartus II online Help in the user interface.	To access Help, type <code>hh quartus.chm</code> <Return> at a command prompt.
If you are accessing the Quartus II software through one of the following versions of the Hummingbird Exceed software (6.2, 7.0, 7.1, or 8.0) and have any Microsoft Office application or Internet Explorer open, the Quartus II user interface may start very slowly.	Contact Hummingbird Software at www.hummingbird.com for a patch for the Exceed software.
The stand-alone Quartus II Programmer and SignalTap [®] II programs are not available on Solaris and Linux workstations.	

Linux Only

Issue	Workaround
Version 6.0	
The Quartus II software may crash with a core dump if you close the Quartus II software while a properties dialog box is open from any link in Help.	Do not open the properties dialog box on any link in Help.

Issue	Workaround
When you are running the Quartus II software on Red Hat Enterprise Linux 4.0 and using the KDE 3.3 desktop, the Quartus II software may 'hang' when a graphical tool such as the Chip Editor or Pin Planner displays a tooltip when you select an element to edit.	Set the environment variable <code>cui_disable_tooltips = 1</code> to disable tooltips.
Your programming hardware is not shown in the Add Hardware dialog box when running under Red Hat Enterprise Linux 64.	Only the EthernetBlaster is supported for programming on 64-bit platforms.
You may receive an error message if you click Run EDA Gate-Level Simulation in the EDA Simulation Tool menu under Red Hat Linux when Cadence NC-Sim is specified at the simulation tool.	You must run the NC-Sim software manually.
Version 5.1 SP2 and earlier	
If you run a remote Linux desktop session in a Windows client such as Exceed, depending on your configuration, the SignalTap II Logic Analyzer may be unstable and could crash with a segmentation fault.	Use an Xterm window to access the Quartus II software instead of a remote desktop session.
Clicking the "X" close button is visible on the Chip Editor loading progress dialog box may cause the Quartus II software to crash.	Do not click the "X" button while the Chip Editor is loading.
If the MasterBlaster™ download cable is not listed in the Available hardware items list in the Hardware Settings tab of the Hardware Setup dialog box, but it is connected properly, you may not have read/write permission for the serial (<code>/dev/ttySx</code>) port to which the MasterBlaster cable is connected.	Have a system administrator assign read/write permission for the appropriate port. This change can be accomplished by adding you to the "uucp" group, or by giving read/write permission for the serial port to everyone, using the following command: <code>chmod o+rw /dev/ttySx</code> where <i>x</i> is the serial port affected.
If you are using the ReflectionX X-server software as your display on a Linux workstation, the Quartus II software may hang and a white box may appear.	Set the <code>QUARTUS_MWWM</code> environment variable to <code>allwm</code> and then start the Quartus II software without the splash screen by typing the following commands at a command prompt: <code>setenv QUARTUS_MWWM allwm <Return></code> <code>quartus -no_splash <Return></code>

Issue	Workaround
Under certain circumstances, the Quartus II software may not start properly.	On a system with a static IP address, ensure that the <code>/etc/hosts</code> file has an entry for the host name of the machine on which you are running. For example, if the workstation is named “orange,” there should be an entry in <code>/etc/hosts</code> with the IP address of the “orange” workstation as shown below: <pre><IP address of orange> orange</pre> In addition, the network configuration (hostname, DHCP host name, DNS search path, and domain names) must be correct or the Quartus II software will abort on startup.
If you are running the Quartus II software version 4.0 and later using VNC software, the Quartus II software may terminate unexpectedly whenever you open any file or browse any directory from within the Quartus II software.	Make sure your VNC server software is version 3.3.4 or later.
If you are running the Quartus II software under Red Hat Linux 8.0, you may experience substantial degradation of compilation times if your design files are located on a separate server from the Quartus II software.	Make sure that the operating system kernel is upgraded to the latest available. If you are using a NetApps server, refer to the following document for more information: www.netapp.com/tech_library/ftp/3183.pdf

Device Family Issues

Cyclone, Stratix & Stratix GX

Issue	Workaround
Version 6.0	
The Altera PCI core may have timing violations if you have selected Use TimeQuest Timing Analyzer during compilation and you are targeting a Stratix, Stratix GX or Cyclone II device.	To improve the optimization of the PCI core in this case, which will likely resolve the timing violations, add the following line to your <code><revision_name>.qsf</code> file: <pre>set_global_assignment -name INI_VARS "FITTER OPTIMIZE BIAS FOR PCI=ON"</pre>

Issue	Workaround
Editing the global level of an input port in Resource Property Editor for Stratix, Stratix GX, Cyclone or MAX II devices may cause an Internal Error when you click Check and Save All Netlist Changes .	In order to prevent this error, either 1) modify the global levels of <i>all</i> input ports fed by the driving output port of the input port; or 2) remove the connections associated with the other fan-outs of the driving output port using the Resource Property Editor and restore the logical connection using the Change Manager
The method used to report power for clock networks is different between the Quartus II PowerPlay Power Analyzer and the PowerPlay Early Power Estimator (EPE). The Quartus II PowerPlay analyzer reports the power for the resource (pin or PLL) that drives the network, while the EPE reports the power in the Clock Network section of the spreadsheet.	No action is necessary.
Version 5.1 SP2 and earlier	
When you use a Routing Constraints File (.rcf) to control fitting after performing Routing Back-Annotation, your timing analysis results may change slightly due to parasitic and other effects. Any change will be very small.	
If you use the SignalProbe feature to observe the signals at an output pin, by routing them to another output pin, the SignalProbe output pin signal will be shown as Unknown (X) in the Quartus II Simulator.	The signal will be correct in actual operation, the error appears only in the Quartus II Simulator.
In the SignalProbe Source to Output Delays table of the Timing Analyzer Report, the following shortcut menu commands are not available although they are available in other similar Timing Analyzer Report tables: <ul style="list-style-type: none"> • List Paths • Locate in Chip Editor • Locate in Timing Closure Floorplan 	You can use other Timing Analyzer Report tables to list and locate the affected paths.

Stratix and Stratix GX

Issue	Workaround
Version 6.0	
<p>The Quartus II PowerPlay Power Analyzer reports PLL, XGMII state machine, GXB transceiver, and I/O pin power as contributors to the power reported for High Speed Transceiver blocks. However, the PowerPlay Early Power Estimator (EPE) spreadsheet reports this power in a “High Speed Transceiver Blocks” section as well as an entry in the “Clock Networks” section. Similarly, the PLL, SERDES blocks, and I/O pins of an LVDS block are reported in the PowerPlay Power Analyzer, and as entries in the Clock Networks and HSDI sections of the EPE spreadsheet.</p>	
Version 5.1 SP2 and earlier	
<p>If you use the <code>altdio_bidir</code> or <code>alt_dqs</code> megafunction and connect any data port directly to VCC or GND, the Quartus II software version 3.0 SP1 and later will insert an additional logic element in the circuit path.</p>	
<p>The behavior of the 0-degree phase shift setting of the <code>DLL_PHASE_SHIFT</code> parameter of the <code>altdqs</code> megafunction or the DQS Phase Shift logic option with the <code>altdio_bidir</code> megafunction has changed in the Quartus II software version 3.0 SP2. The previous behavior produced an uncharacterized delay that cannot be specified to fall within the specified 500 ps delay difference.</p>	<p>If your design uses this setting and does not work correctly after installing the Quartus II software version 3.0 SP2 or later, you should contact the Altera Applications department for further information.</p>

Stratix

Issue	Workaround
<p>Designs compiled for Stratix EP1S40ES devices must be recompiled for the EP1S40 device before programming.</p>	

Issue	Workaround
Stratix PLL simulation models have been enhanced to handle jitter on the input clock. This enhancement has the unintended side effect that functional simulations for LVDS designs using cascaded PLLs may be incorrect by one clock cycle.	Altera recommends that you perform Timing Simulation to display the correct behavior in the Quartus II Simulator or in other EDA Simulators.

Stratix II

Issue	Workaround
An intermittent read failure has been detected on Stratix II M4K RAMs due to a software configuration error for designs compiled with Quartus II software version 5.0 SP1 and earlier.	This issue has been resolved in the Quartus II software 5.0 Service Pack 2 and Quartus II software version 5.1. To learn more about this issue, please refer to the Stratix II Errata on the Altera web site.
Due to changes in the <code>altlvds_tx</code> and <code>altlvds_rx</code> megafunctions in the Quartus II software version 5.0, user-created timing assignments to the megafunctions are changed. The megafunctions now make most timing assignments automatically.	Check your assignments to make sure that the Quartus II software implemented them correctly.
The Quartus II software version 5.0 does not support programming file generation for some Stratix II devices when M-RAM blocks are used in some memory modes, and if the <code>STRATIXII_MRAM_COMPATIBILITY</code> option is turned off.	For more information about programming file support for Stratix II devices, please refer to the <i>Stratix II FPGA Family Errata Sheet</i> , which is available on the Altera web site.
The Quartus II software version 4.2 and later supports programming file generation for EP2S60 ES devices, but only for designs where the M-RAM memory is not used.	For more information about programming file support for Stratix II devices, please refer to the <i>Stratix II FPGA Family Errata Sheet</i> , which is available on the Altera web site.
Back-annotating some designs targeted to a Stratix II device with the Demote cell assignments to option set to LABs may prevent the design from fitting.	Back-annotate the design with Demote cell assignments to turned off.

Stratix GX

Issue	Workaround
Version 6.0	
Timing simulation performed in the Quartus II software on designs that use the <code>altgxb</code> megafunction in Stratix GX devices is not accurate on the <code>rx_clkout</code> and <code>rx_out</code> outputs. The simulation is functionally correct, but the relative timing delays between the signals are not accurate.	Perform your timing simulation in another tool such as ModelSim.
Version 5.1 SP2 and earlier	
The RREFB pin names for EP1SGX10C, EP1SGX25C, EP1SGX25D, and the EP1SGX40F devices changed in the Quartus II software version 5.0. This may affect your PCB layout.	Each RREFB pin must be tied to ground through a resistor. Altera recommends that you not connect multiple RREFB pins through a single resistor to ground.

Stratix II GX

Issue	Workaround
Version 6.0 SP1	
When you select SONET OC-48 configurations in the <code>alt2gxb</code> megafunction and the “ Flip word alignment pattern bits ” option is turned off, it is possible that the byte ordering block may lock to a data pattern that is not optimal.	Do not turn off the “ Flip word alignment pattern bits ” option (it is on by default).
Version 6.0	
The latency of <code>alt2gxb</code> megafunction simulations on Stratix II GX is not accurate in comparison to the device. This is due to approximation used in the Quartus II simulation in modeling the analog portion of the hardware. The latency on the digital portion is within the range of a few clock cycles of the device. The latency is an exact match with the hardware when input vectors are carefully made and do not contain any race conditions.	The Stratix II GX handbook has specified latency range information. The latency information from Quartus II simulations is a good approximation.

Issue	Workaround
<p>You may receive an error message saying “The Quartus II software could not combine the following GXB REFCLK divider(s)...” when performing incremental compilation on a Stratix II GX design. These error messages result from two causes:</p> <ol style="list-style-type: none"> 1. You are trying to combine multiple alt2gxb megafunctions and they are not in the same partition. 2. You are using multiple alt2gxb megafunctions that use a calibration block, and are not in the same partition. 	<ol style="list-style-type: none"> 1. Place all alt2gxb megafunctions in the same partition. 2. There is only one calibration block in the device. You should enable the calibration block for one instance of the alt2gxb megafunction only, and disable the calibration block for the other instances.
Version 5.1 SP2 and earlier	
<p>In Basic protocol, when the 8B10B encoder is used, the alt2gxb MegaWizard provides the tx_forcedisp and tx_dispval ports. These ports do not have any effect on the transmitted serial data when used in the Quartus II software version 5.1. This behavior is reflected in simulation.</p>	<p>None necessary.</p>

Cyclone

Issue	Workaround
<p>Altera recommends that the frequency of the external clock output of the PLLs be limited to 312 MHz.</p>	
<p>The operating frequency range of the Cyclone PLL has been changed. In the Quartus II software version 3.0 and earlier, the range was 300 MHz to 800 MHz. In version 3.0 Service Pack 1 and later, that range changed to 500 MHz to 1000 MHz because of concerns about jitter at frequencies below 500 MHz. Because of this change, the minimum input frequency is now 15.625 MHz (previously 15 MHz) and the minimum output frequency is also 15.625 MHz (previously 9.38 MHz).</p>	<p>Recompile your design after installing the current version of the Quartus II software.</p>

Issue	Workaround
The PLL lock circuit does not function correctly for PFD (Phase Frequency Detector) frequencies below 200 MHz when the temperature is below -20°C.	If operation at temperatures below -20°C is required, choose a higher input frequency and clock division (N) factor such that the PFD input frequency is higher than 200 MHz.

Cyclone II

Issue	Workaround
Version 6.0	
If your design uses a Cyclone or Cyclone II device and you add the VREF Pad column to the Pin Planner UI, the Quartus II software may crash with an internal error.	Do not use the VREF Pad column in the Pin Planner if your design is for a Cyclone or Cyclone II device. If you have already added the column, open a project that uses a device family other than Cyclone or Cyclone II, open the Pin Planner, and turn off the VREF Pad column.
Version 5.1 SP2 and earlier	
A write error has been detected on Cyclone II M4K RAMs when using dual ports and dual clocks for designs compiled with Quartus II software version 5.0 SP1 and earlier.	A software workaround is available to address this issue in the Quartus II software version 5.0 SP2 and Quartus II software version 5.1. To learn more, please refer to the Cyclone II Errata on the Altera web site
If your design uses dual-port, dual-clock memory with a Memory Initialization File (.mif) and you have set the CYCLONE_SAFE_WRITE parameter in the altsyncram megafunction to RESTRUCTURE, any changes to the MIF file contents will be ignored if you have Smart Compilation turned on.	
Back-annotating some designs targeted to a Cyclone II device with the Demote cell assignments to option set to LABs may prevent the design from fitting.	Back-annotate the design with Demote cell assignments to turned off.

MAX II

Issue	Workaround
If your design uses an <code>altparallel_flash_loader</code> instantiation created in the Quartus II software version 5.0 SP1 or earlier, you may receive errors during compilation because the port names have changed in the <code>altparallel_flash_loader</code> megafunction included in the Quartus II software version 5.1.	Use the Megawizard Plug-in Manager to re-generate your <code>altparallel_flash_loader</code> instantiation. Modify your design files to connect to the new <code>altparallel_flash_loader</code> port names.

HardCopy II

Issue	Workaround
Version 6.0	
The Quartus II software may crash with an internal error when you perform an incremental compilation on a HardCopy II design.	Turn off the Incremental Compilation option and remove your design partitions before compiling.
A HardCopy II design that contains latches with preset or clear signals and a constant (VCC or GND) data, may cause the HardCopy II Revision Compare tool to report a difference in the timing constraints because of a difference in which signal is considered the enable for the latch.	No workaround is necessary, you can safely ignore the warning.
Formal verification is not supported during development of designs for migration to HardCopy II devices.	If you must use formal verification during development of your HardCopy II design, you must turn off formal verification options, perform full compilations on both (Stratix II and HardCopy II) revisions, and perform the migration again before generating the handoff files.
When migrating a design from Stratix II to HardCopy II, the Revision Compare tool can report differences between the two revisions because of different packing of fast I/O registers because additional packing can be performed on HardCopy II devices that cannot be performed on Stratix II devices.	Either accept the additional packing, and ignore the reported differences or disable Fast I/O assignments on the nodes reported by the Revision Compare tool.

Issue	Workaround
The Design Space Explorer's Search for Lowest Power functionality is not available for HardCopy II devices.	To optimize the device power in a design that targets a HardCopy II device, follow the recommendations in the Power Optimization Advisor, and manually run the Power Analyzer in the Quartus II software to determine the results.
Under certain circumstances, the HardCopy II Companion Revision Comparison tool may report a mismatch in Memory Initialization Files (.mif) between the Stratix II and HardCopy II revisions.	Manually compare the MIF files to determine if they are functionally equivalent.
Under certain circumstances, you may receive the following error message when migrating your Stratix II design that contains RAM blocks to HardCopy II: Error: Source file <file> in directory <dir> was compiled at <time> and saved at <time>. The problem reported for the file is: Only in HardCopy II (<design>).	Turn off the Auto RAM Block Balancing option for your Stratix II design and recompile the design. Then proceed with the migration process.
Version 5.1 SP2 and earlier	
The HardCopy II Companion Revision Comparison tool can be too strict and produce false positives. That is, it flags certain netlist block differences as functionality differences when they do not actually produce different behavior in silicon. The following example illustrates this behavior: <ul style="list-style-type: none"> The Companion Revision Comparison tool considers a global assignment of <NONE> to be different from "" (null), and reports a difference. 	In each of these cases, the functionality of the two revisions is the same in silicon, but you must manually verify that the functionality is the same. You can use the block names listed in the Companion Revision Report to locate to the Resource Property Editor to verify the functionality
PCI core designs compiled with versions of the PCI Compiler earlier than 4.0.0 will cause numerous spurious differences to be reported in the Companion Revision Compare section of the Compilation Report, even though the source files are correct.	Recompile the PCI core with the PCI Compiler version 4.0.0 or later.
You may receive Revision Comparison warnings about differing EDA tool settings if your project directory contains a Quartus II Defaults File (.qdf).	Delete the Quartus II Defaults File from your project directory.

EPC2 Configuration Devices

Issue	Workaround
Version 6.0	
<p>When using the EPC2 configuration device to configure an Altera FPGA using a compressed configuration bit stream, you may encounter a configuration failure due to the CONF_DONE error checking feature. The failure mode occurs when the FPGA releases the CONF_DONE signal outside the acceptable time window. The reason this may occur is because the compression ratio varies depending on the design file. Since the configuration file size varies due to compression there may be insufficient padding at the end of the configuration file. This issue can result in a configuration failure, as indicated by the nSTATUS pin transitioning low near the end of configuration. The error occurs because the CONF_DONE signal is released by the FPGA before the EPC2 device expects it to be released</p>	<p>For assistance implementing the work around, please contact Altera Technical Support at www.altera.com/mysupport, and click “Create New Service Request”.</p>

Design Flow Issues

Verification

Issue	Workaround
<p>If you are using IP Toolbench to generate simulation models for Altera IP Megacore® functions, you will get an error if support for the Stratix device family is not installed.</p>	<p>Install support for the Stratix device family.</p>
<p>If you are using IP Toolbench to generate simulation models for Altera IP Megacore® functions, and you do not turn on Generate Simulation Model in the Set Up Simulation Model dialog box during setup, you will get an error when you launch the simulation using Modelsim.</p>	<p>Turn on Generate Simulation Model in the Set Up Simulation Model dialog box and regenerate the Megacore® .</p>

Issue	Workaround
Incremental routing may fail for nodes assigned to the SignalTap II Logic Analyzer if you have turned on any of the Physical Synthesis Fitter optimizations, such as Perform physical synthesis for combinational logic or Perform register duplication or Perform register retiming .	

Integrated Synthesis (VHDL and Verilog HDL)

Issue	Workaround
Version 6.0 SP1	
In the Quartus II software version 6.0 and earlier, when an inverted cone of logic drove a bidir pin, the inversion was incorrectly removed.	Recompile your design with the Quartus II software version 6.0 SP1 or later.
In the Quartus II software version 6.0 and earlier, the Quartus II Integrated Synthesis ignored the default value for an incomplete CASE statement if the CASE statement has overlapping conditions in the same CASE item.	Recompile your design with the Quartus II software version 6.0 SP1 or later.

Issue	Workaround
Version 6.0 and earlier	
<p>When a VHDL or Verilog design specifies a RAM, there are a few cases in which the read-during-write behavior of the RAM will differ between the original design and the hardware implementation and no warning will be given. The following examples illustrate this behavior:</p> <p>The first case occurs when a RAM in a lower-level module directly drives a set of registers in an upper-level module. To work around this problem, move the registers to the lower-level module.</p> <p>The second case occurs when there is combinational logic between a RAM and a set of registers, and the design specifies the write operation of the RAM will occur before the read operation. To work around this problem, remove the logic between the RAM and the registers.</p> <p>The third case is the same as the second case, with the exception that the design specifies the read operation of the RAM will occur before the write operation, and the read address of the RAM is registered. To get around this problem, either remove the logic between the RAM and the registers, or set the Automatic RAM Replacement option to Off.</p>	<p>The workaround for each case is shown immediately following the example.</p>

Verilog HDL Integrated Synthesis

Issue	Workaround
<p>Beginning with the Quartus II software version 5.1, implicit or explicit declarations inside unnamed generate blocks are no longer visible outside the generate block.</p>	<p>Declare the object outside the generate block. You can also add a name to the generate block and refer to the object with a hierarchical name.</p>

Issue	Workaround
<p>A Verilog HDL design that compiles successfully in earlier versions fails in the Quartus II software version 5.1 with the message “Formal port <port_name> must be connected to a structural net expression.”</p>	<p>The Verilog language requires that a module instance output port be connected to a net, and not to a reg variable or to a constant. Previous versions of the Quartus II software did not enforce this restriction. Change the variable connected to the module instance output port to a wire datatype.</p>
<p>A Verilog design that compiles successfully in earlier versions fails in the Quartus II software version 5.0 with the message “Error: Verilog HDL or VHDL error at <filename(line)>: object "<pin_name>" declared in a List of Port Declarations cannot be redeclared within the Module Body”</p>	<p>Remove the declaration in the module body. Ports must be completely specified in the Verilog 2001 list of ports declaration, including where necessary the direction, width, net or variable type, and whether the port is signed or unsigned.</p>

SignalTap II

Issue	Workaround						
<p>Version 6.0</p>							
<p>Under certain circumstances, you will receive an error saying “Invalid MEX file...” when you run the SignalTap II Logic Analyzer within the MATLAB Release 14 Service Pack 3 Version 7.1 software.</p>	<p>Use one of the following versions of the MATLAB software:</p> <table border="0" data-bbox="824 1115 1377 1224"> <tr> <td>Release 14 original release</td> <td>Version 7</td> </tr> <tr> <td>Release 14 Service Pack 1</td> <td>Version 7.0.1</td> </tr> <tr> <td>Release 14 Service Pack 2</td> <td>Version 7.0.4</td> </tr> </table>	Release 14 original release	Version 7	Release 14 Service Pack 1	Version 7.0.1	Release 14 Service Pack 2	Version 7.0.4
Release 14 original release	Version 7						
Release 14 Service Pack 1	Version 7.0.1						
Release 14 Service Pack 2	Version 7.0.4						
<p>Version 5.1 SP2 and earlier</p>							
<p>In SignalTap II, nodes dropped in from the Node Finder are always sorted and inserted in descending order, for example, foo [3], foo [2], foo [1], foo [0]. If this is the incorrect order, you can select the LSB on Top, MSB on Bottom option. In version 5.1, negative ranges are now allowed in Verilog HDL, however negative numbers are inserted in the reverse order, for example, foo [3], foo [2], foo [1], foo [0], foo [-3], foo [-2], foo [-1].</p>							

SOPC Builder Issues

Issue	Workaround
Version 6.0	
<p>The Avalon Interface Specification incorrectly describes the behavior for <code>address</code> and <code>burstcount</code> during burst transfers. The Avalon Interface Specification states: “The start of a write burst is similar to the start of a fundamental master write transfer. The master port asserts <code>address</code>, <code>writedata</code>, <code>write</code>, and <code>byteenable</code> (if present) in addition to <code>burstcount</code>. ... This is the only time that the Avalon switch fabric captures <code>burstcount</code> and <code>address</code>; the master port can deassert them through the remainder of the burst.”</p>	<p>During Avalon master transfers, assert constant values on <code>address</code> and <code>burstcount</code> for the duration of the burst.</p>
<p>If multiple masters control a slave that asserts <code>endofpacket</code>, both masters will see the asserted <code>endofpacket</code>. This may cause problems in systems where masters take action upon <code>endofpacket</code>.</p>	<p>Use <code>endofpacket</code> only in the case that a single master of the asserting slave will take action on the <code>endofpacket</code>.</p>
Version 5.1 SP2 and earlier	
<p>Back-to-back burst transfers from a master to a slave that has a different burst count or bandwidth may fail.</p>	<p>Wait until the slave has finished the read burst before starting a write burst.</p>
<p>Under some circumstances, the automatic addressing feature does not function correctly.</p>	<p>Assign the base address for the component manually.</p>
<p>The setting of the Dual-Port Access option , in the Legacy On-Chip Memory wizard is always shown as “Off” regardless of setting.</p>	<p>Always set the Dual-Port Access option to your desired setting before clicking Finish in the wizard.</p>
<p>Under some circumstances, the SOPC Builder does not display correctly on systems in which the graphics card uses hardware acceleration.</p>	<p>Turn off, or reduce the level of hardware acceleration.</p>
<p>In SOPC Builder, Avalon Masters that address more than 32 bits of slave address space do not issue warning.</p>	<p>Redesign your system to avoid giving masters greater than 32 bits of address space.</p>
<p>SOPC Builder fails to open on UNIX when invoked from the MegaWizard Plug-In Manager.</p>	<p>Open SOPC Builder by clicking SOPC Builder on the Quartus II Tools menu.</p>

Issue	Workaround
You may see random display errors, such as streaks and blotches, in the SOPC Builder GUI.	Lower the Hardware Acceleration setting on the Troubleshooting tab of the Advanced Display Settings dialog box in your Display Settings control panel. There is a known incompatibility between the current Java Runtime Environment (JRE) and certain laptop graphics drivers.
When creating a component with the SOPC Builder Component Editor, you must not choose a component name that exactly matches the HDL file name or the top-level module name. If the names are the same, SOPC Builder will generate an error during system generation. This problem will be fixed in a future version of SOPC Builder.	Using the SOPC Builder Component Editor, rename the component to a different name. In the SOPC Builder table of active components, add the newly-named component to your system, and delete the old component.
If the Quartus II software is installed in a directory that has space characters in its name, the SOPC Builder software will not run.	Install the Quartus II software in a directory that does not have space characters in the path.
The SOPC Builder and Nios II Software Development Kit shell may “hang” and become unresponsive if you run either program while the Frisk antivirus software is running.	Turn off the Dynamic Virus Checking feature of the Frisk software before running SOPC Builder or the Nios II SDK shell.

EDA Integration Issues

Issue	Workaround
Version 6.0	
When using Formal Verification, if you recompile the design without changing the source files, the Formal Verification database generated by the Quartus II software will not contain information about Quartus II synthesis optimizations. This can lead to mismatches and/or other issues in the Formal Verification tool.	Delete the <code><project>\db</code> directory and recompile the design.
The ModelSim software may fail to simulate a design if Glitch Filtering is turned on in the EDA Simulation Settings page and the <code>+nospecify</code> option is passed to the ModelSim vsim command.	Remove the <code>+nospecify</code> option from the ModelSim vsim command.

Issue	Workaround
If you add or change a component in a Library Mapping File (.lmf), the Quartus II software does not recognize the changes upon the next compilation.	Delete the project database (db) directory and recompile.
Running a simulation using NC-Sim version 5.5 or later with files generated with the Quartus II software version earlier than 6.0 causes you to receive the following warning message from ncelaboration: "ncelab: *W,CUNOTB: component instance is not fully bound"	Add the <code>-relax</code> or <code>-lib_binding</code> option to your elaboration command.
Version 5.1 SP2 and earlier	
Timing simulation with the Synopsys VCS MX software is not supported in the Quartus II software versions 5.1 and later.	
You cannot perform RTL simulation of the SerialLite and RLDRAM IP MegaCores in 3 rd party simulators using the NativeLink integration feature.	Perform simulation manually as described in the User Guide for the MegaCore you are using.
FIFO Partitioner instances can only be simulated in 3 rd party simulators using the original VHDL source files from the quartus/libraries/megafunctions/ directory, and NativeLink integration is not supported.	Perform simulation manually as described in the FIFO Partitioner User Guide available from the Literature page of the Altera web site.
The current version of the Quartus II software allows you to select the Synplicity Amplify software as a physical optimization tool. However, this setting is for an automated mode called ATOPS, which is currently not supported by the Amplify software.	Contact Synplicity for the support schedule for the Amplify software ATOPS mode.
NativeLink support does not work with versions of Mentor Graphics Precision RTL Synthesis Software earlier than version 2003b due to a change in the Precision project interface.	

Simulation Model Changes

altera_mf Models

Model	Changes
altsyncram	<ul style="list-style-type: none"> 'X' or don't care is shown at the output port during the simultaneous read and write at the same address only if the byteena port is asserted. Old data is output instead in the same scenario if the byteena port is not asserted. Previously, old data would be output at times regardless of whether the byteena port is asserted.
scfifo	<ul style="list-style-type: none"> Added support for parameter USE_EAB. The behavior for FIFO is changed when USE_EAB is set to "off". When this parameter is set to "off", the output of the FIFO will power up to low as its initial state and the latencies in write and clear request to FIFO output are reduced. The default value of this parameter is "on." This applies only to Stratix, Stratix II, Stratix GX, Stratix II GX, Hardcopy Stratix, Hardcopy II, Cyclone, and Cyclone II devices.
dcfifo	<ul style="list-style-type: none"> DCFIFO low latency mode allows the data size to be lpm_numwords instead of lpm_numwords - 1. The "wrfull" is asserted when lpm_numwords of writes has occurred.
altlvds_tx	<ul style="list-style-type: none"> Added parameter "outclock_multiply_by" which determines whether to multiply the frequency of tx_outclock. This parameter can have only 1 or 2 as legal value. Setting this parameter to 2 multiplies the frequency by 2. The default value of this parameter is 1. Added parameter "coreclock_divide_by" which determines whether to divide the frequency of tx_coreclock. Setting this parameter to 1 divides the frequency by half value. This parameter can only have 1 or 2 as legal value. The default value of this parameter is 2. Fixed byte order problem in the flexible-lvds transmitter. Fixed incorrect simulation output for x1 and x2 mode when inputs are registered for Stratix, Stratix II, Stratix GX, Stratix II GX, Hardcopy Stratix, Hardcopy II, Cyclone and Cyclone II device families.

Model	Changes
altp11	<ul style="list-style-type: none"> Fixed incorrect simulation result when user specifies a small ratio of output clock frequency to the input clock frequency. Added a parameter “port_scanclk” which determines the port connectivity of “scanclk” port. If the port_scanclk parameter is specified as “PORT_USED”, the input signal on scanclk is used in the simulation. If “PORT_CONNECTIVITY” is specified, the scanclk is used based on its port connectivity. If “PORT_UNUSED” is specified, the input signal to scanclk port is ignored.
altmult_accum	<ul style="list-style-type: none"> Fixed incorrect saturation result if saturation is turned on and there is no saturation overflow. This is applicable for StratixII devices only.

Notes:

- Major changes to Altera Primitives simulation models since Quartus II 5.1
 - Added new primitives CLKLOCK, TRI, LUT_INPUT, LUT_OUTPUT, DFF, DFFE, SRFF, SRFFE, JKFF, JKFFE, TFF, TFFE, LATCH, ALT_INBUF, ALT_IOBUF, ALT_OUTBUF & ALT_OUT_BUF_TRI.
 - All new and existing primitives have been relocated to new ALTERA_PRIMITIVES library.

ALTERA_PRIMITIVES.V (HD) & ALTERA_PRIMITIVES_COMPONENTS.VHD are located in the **quartus\eda\sim_lib** library.

- Only the LCELL primitive remains in the ALTERA_MF library.
- Simulation PLI function `convert_hex2ver.dll` has been replaced by Verilog task `convert_hex2ver`, located in the ALTERA_MF.V library.
- The ModelSim software gives the following warning when **altera_mf** or **220models** megafunction models are compiled with the -87 option:

```
*** Warning (vcom-1148) Condition in IF GENERATE must
be static
```

You can safely ignore this warning because under the 1987 rules, the constant is not considered to be static because of the initialization from the function call.

- RAM Megafunction models only support HEX format for all other EDA simulators. Manually convert MIF format to HEX first in the Quartus II software.
- The ModelSim software gives the following warning when **altera_mf** or **220models** megafunction models are compiled with the -87 option:

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- RAM Megafunction models support only the HEX format for all other EDA simulators. Manually convert MIF format to HEX first in the Quartus II software.

Latest Known Quartus II Software Issues

For known software issues after publication of this version of the *Quartus II Software Release Notes*, please look for information in the **Quartus II Latest Known Issues** section of the Altera Support Find Answers Database at the following URL:

[http://answers.altera.com/altera/index.jsp?/Topics/Support Solutions/Known Issues/Software/Quartus II](http://answers.altera.com/altera/index.jsp?/Topics/Support/Solutions/Known%20Issues/Software/Quartus%20II)

Revision History

Revision	Description
1.0	Initial Release

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