



Quartus II Device Support Release Notes

June 2006

Quartus II version 6.0 Service Pack 1

This document provides late-breaking information about device support in this version of the Altera® Quartus® II software. For information about memory, disk space, and system requirements, refer to the **readme.txt** file in your `\altera\quartus<version number>` directory. For information about New Features, EDA Tool version support, and existing and resolved software issues, refer to the *Quartus II Software Release Notes*.

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Device Support & Pin-Out Status

This section contains information about the status of support in the Quartus II software for the devices listed.

Full Device Support

Full compilation, simulation, timing analysis, and programming support is now available for the following new devices and device packages:

Devices with Full Support

Device Family	Devices	
Cyclone® II	EPC8AF256	EP2C15AF256
	EP2C15AF484	EP2C20AF256
	EP2C20AF484	
MAX® II	EPM240F100	EPM240M100
	EPM570F100	EPM570M100
	EPM570M256	EPM1270M256

Advance Device Support

Compilation, simulation, and timing analysis support is provided for the following devices that will be released in the near future. Although the Compiler generates pin-out information for these devices, it does not generate programming files for them in this release.

Devices with Advance Support

Device Family	Devices	
None		

Timing Models

This section contains a summary of timing model status in the current version of the Quartus II software.

Preliminary Timing Models

The following table shows the devices with preliminary timing models in the current version of the Quartus II software:

Devices with Preliminary Timing Models

Device Family	Device	
HardCopy [®] II	HC210	HC210W
	HC220	HC230
	HC240	
Stratix [®] II GX	EP2SGX30	EP2SGX60
	EP2SGX90	EP2SGX130

Final Timing Models

The following table lists the devices with final timing models that are available in the current version of the Quartus II software:

Devices with Final Timing Models

Device Family	Device	Timing Models Final in Quartus II Version Number
Cyclone	EP1C3	3.0 SP1
	EP1C4	4.0
	EP1C6	3.0
	EP1C12	3.0 SP1
	EP1C20	3.0
Cyclone II	EP2C5	6.0
	EP2C8	5.1 SP2
	EP2C20	5.1 SP2
	EP2C35	5.1 SP2
	EP2C50	6.0
	EP2C70	5.1 SP2
MAX II	EPM240	5.0
	EPM1270	5.0
	EPM570	5.0 SP1
	EPM2210	5.0 SP1
Stratix	EP1S10	4.1
	EP1S20	4.1
	EP1S25	4.1
	EP1S30	4.1
	EP1S40	4.1
	EP1S60	4.1
	EP1S80	4.1
Stratix II	EP2S15	5.0 SP1
	EP2S30	5.0
	EP2S60	5.0
	EP2S90	5.0 SP1
	EP2S130	5.0 SP1
	EP2S180	5.1
Stratix GX	EP1SGX10	4.1
	EP1SGX25	4.1
	EP1SGX40	4.1

The current version of the Quartus II software also includes final timing models for the ACEX[®] 1K, APEX[®] 20K, APEX 20KE, APEX 20KC, APEX II,

FLEX[®] 6000, FLEX 10K, FLEX 10KA, FLEX 10KE, and MAX 7000S device families. Timing models for these device families became final in versions earlier than version 4.0.

Power Models

This section contains a summary of power model status for recent devices in the current version of the Quartus II software.

Device Family	Power Model Status
Stratix	Final – 5.1
Stratix GX	Final – 5.1
Stratix II	Final – 6.0
Stratix II GX	Preliminary
Cyclone	Final – 5.1
Cyclone II	Final – 6.0
MAX 3000A	Final – 5.1
MAX 7000AE	Final – 5.1
MAX 7000B	Final – 5.1
MAX II	Final – 5.0 SP1
HardCopy II	Preliminary

Changes in Device Support

HardCopy II Floorplan Change for HC240

This issue affects the HardCopy II HC240 device. The physical location information for the HCell arrays has been updated. Some HCell locations from previous versions of the Quartus II software may be invalid. All HC240 designs must be recompiled in the Quartus II software version 6.0 SP1 or later to validate the HCell locations.

Cyclone II Memory Interface Speed

This change affects Cyclone II devices. The maximum speed of DDR and DDR2 memory interfaces on Cyclone II C8 and I8 speed grade devices is increased from 125 MHz to 133 MHz, except for the devices in 240-pin PQFP packages. The change does not apply to devices in 240-pin PQFP packages.

Updated IBIS Models

This change affects Cyclone, Cyclone II, and Stratix II devices. The IBIS models have been updated to improve accuracy. This change does not affect the Quartus II timing models or timing reports.

Cyclone II Pin-out Change for EP2C20Q240

This issue affects Cyclone II EP2C20 devices in the Q240 package. In the Quartus II software versions 5.1, 5.1 SP1, 5.1 SP2, and 6.0, the Fitter would not allow assignment of DQ signals in some legal placements, when using x18 groups. This error is corrected so that all legal placements are supported.

Error in PowerPlay Early Power Estimator File for Memory Blocks

This issue affects Cyclone II, Stratix II, Stratix II GX, and HardCopy II devices. In the Quartus II software versions 5.1 SP1, 5.1 SP2, and 6.0, the design summary file generated by the Quartus II software for the PowerPlay Early Power Estimator spreadsheet could contain an error when a memory block uses a read enable, write enable, or clock enable input signal connected to a constant value. This error could cause the Early Power Estimator spreadsheet to report an inaccurate result regarding the expected dynamic power consumption of the memory block. This error is corrected in the Quartus II software version 6.0 SP1.

Cyclone II LVDS Phase Issue

This issue affects Cyclone II devices. In the Quartus II software version 6.0, LVDS receiver interfaces that use a PLL in source-synchronous mode may not be configured for the appropriate PLL phase shift for reliable operation. To ensure the correct PLL phase shift, the `altlvds` MegaWizard Plug-In has been updated to add a new option, **Align clock to center of data window at capture point**. To update affected LVDS receiver interfaces to use the correct PLL phase using the MegaWizard Plug-In Manager, turn on the **Align clock to center of data window at capture point** option in the MegaWizard Plug-In, and click **Finish** to regenerate the megafunction files. To update affected LVDS receiver interfaces without using the MegaWizard Plug-In Manager, apply the parameter setting `USE_NO_PHASE_SHIFT = OFF` to the affected `altlvds` megafunctions in the design. You must recompile and perform timing analysis on your design after making these changes. New LVDS interfaces created using the `altlvds` MegaWizard Plug-In the Quartus II software versions 6.0 SP1 and later use the correct setting automatically.

DDR and DDR2 Memory Interface Timing Issue

This issue affects Cyclone II, Stratix II, Stratix II GX, and HardCopy II devices. Designs that use Altera's DDR & DDR2 SDRAM Controller Compiler version 3.4.0 with the DDR & DDR2 SDRAM Timing Wizard (DTW) version 6.0 are affected. Designs that use the two-PLL implementation using DQS hardware are affected; one-PLL implementations and two-PLL implementations without DQS hardware are not affected. Under the specified conditions, the DTW version 6.0 may generate incorrect memory interface timing constraints. Affected users should run the DTW version 6.0 SP1 or later to generate the correct timing constraints.

Stratix II GX Transmitter Specifications

This change affects Stratix II GX devices. The transmitter specifications are updated to support an expanded V_{OD} range and minimum data rate for the C5 speed grade. The detailed specifications are documented in the *Stratix II GX Device Handbook*.

Stratix II GX Mixed Protocol Support

This change affects Stratix II GX devices. Mixed protocols and data rates are supported in the same GXB Transceiver Quad, with some restrictions. The capabilities and restrictions are documented in the *Stratix II GX Device Handbook*.

PLL Reconfiguration Issue

This issue affects Stratix, Stratix GX, HardCopy Stratix, Stratix II, Stratix II GX, and HardCopy II devices. The issue affects designs that use the PLL reconfiguration feature. For any PLL reconfiguration changes to take effect properly, the `Areset` signal must be asserted, depending on the type of reconfiguration. For more information, see the Errata documents for the affected device families. In the Quartus II software version 6.0, the `altpll_reconfig` megafunction added state machine logic to generate the needed `Areset` pulse. However, in some cases this `Areset` pulse was generated too early, causing the reconfiguration to fail. In the Quartus II software version 6.0 SP1, the state machine logic added into the `altpll_reconfig` is removed to yield behavior similar to that in the Quartus II software version 5.1. Refer to the Errata documents for the correct method to resolve this issue.

Revision History

Revision	Description
1.0	Initial Release

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