



# Quartus II Software Release Notes

July 2007

Quartus II software version 7.1 Service Pack 1

This document provides late-breaking information about the following areas of this version of the Altera® Quartus® II software. For information about memory, disk space, and system requirements, refer to the **readme.txt** file in your `\altera\<version number> \quartus` directory. For information about device support in this version of the Quartus II software, along with the latest information about timing and power models, refer to the *Quartus II Device Support Release Notes* on the Altera website at <http://www.altera.com/literature/lit-qts.jsp>.

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## New Features & Enhancements

The Quartus II software version 7.1 includes the following new features and enhancements:

- Advanced support for Arria GX devices: EP1AGX20F780, EP1AGX35F780, EP1AGX50F1152, EP1AGX50F780, EP1AGX60F1152, EP1AGX60F780, and EP1AGX90F1152.
- Advanced support for these Cyclone III devices: EP3C5E144 and EP3C5F256.
- Advanced support for these Stratix III devices: EP3SL50F484, EP3SL50F780, EP3SE80F780, EP3SE80F1152, EP3SL110F780, and EP3SL110F1152.
- Full support for these Cyclone III devices: EP3C25F324, EP3C25F256, EP3C25E144, and EP3C25Q240.
- Full support for this HardCopy II device: HC210WF484.

## EDA Interface Information

The current version of the Quartus II software supports the following EDA tools.

### Supported EDA Tools

Synthesis Tools	Version	NativeLink Support
Synplicity Synplify & Synplify Pro	8.8.0.4*	✓
Mentor Graphics Precision RTL Synthesis	2006a2*	✓
Mentor Graphics LeonardoSpectrum	2006b*	✓
Magma Design Automation PALACE	2.4	✓
Synopsys Design Compiler FPGA	2005.09	
Synopsys FPGA Compiler II	3.8	✓
Synopsys Design Compiler	2004.12-SP4	
Celoxica DK Design Suite	5	
Simulation Tools	Version	NativeLink Support
Mentor Graphics ModelSim	6.1g	✓
Mentor Graphics ModelSim-Altera	6.1g	✓
Cadence NC-Sim (UNIX)	5.83-p003	✓
Synopsys VCS / VCS MX	Y-2006.06	✓
Aldec Active-HDL	7.2 SP1	✓
Formal Verification Tools (Equivalence Checking)	Version	NativeLink Support
Cadence Encounter Conformal	6.2	
Synopsys Formality	2005.09	
Chip Level Static Timing Analysis	Version	NativeLink Support
Synopsys PrimeTime	Z-2006.12	✓
Board Level Static Timing Analysis	Version	NativeLink Support
Mentor Graphics TAU	3.5.01	
Board Level Symbol/Pin-out Management	Version	NativeLink Support
Mentor Graphics I/O Designer	Library Update 2005.1 V03	

\*Please contact the synthesis tool vendor for a version of their software that supports Arria GX.

## Changes to Software Behavior

This section documents instances in which the behavior and default settings of this release of the Quartus II software have been changed from earlier releases of the software.

Items listed in the following table represent cases in which the behavior of the current release of the Quartus II software is different from a previous version.

Description	Workaround
<b>Version 7.1 SP1</b>	
If you instantiated the alt2gxb megafunction for the (OIF) CEI PHY interface protocol, there is an update that exists that will lower jitter.	To reduce jitter, reopen the existing alt2gxb MegaWizard, and in the <b>General</b> tab, select <b>(OIF) CEI PHY Interface in Which protocol will you be using?</b> The <b>CEI</b> tab appears in the MegaWizard. On the <b>CEI</b> tab, turn on <b>Use central clock divider to improve transmitter jitter</b> .
<b>Version 7.1</b>	
If you select a signal to be tapped that cannot be found in the netlist, the Quartus II software will give a critical warning and proceed with compilation. This is a change of behavior from version 6.1 in which compilation would stop with an error message.	To remove the warnings, remove non-existent nodes from the SignalTap II Logic Analyzer. To revert to the behavior of version 6.1 and earlier, you can promote all critical warnings to error messages in the Messages section of the <b>Options</b> dialog box.
The altlvds_tx megafunction shows the actual phase shift of the tx_outclock generated instead of the core clock frequency. This change is only a change in the information that is displayed, and does not change the actual implementation.	

Description	Workaround
<p>PLLs in Stratix II and Cyclone II devices now have a new parameter, <code>sim_gate_lock_device_behavior</code> that is OFF by default. This new parameter uses a fixed, internal value of 7 to simulate the gate lock feature. If the value is set to ON, you can simulate the actual device behavior for gated lock using the parameter value <code>gate_lock_counter</code>, as you could in earlier versions of the Quartus II software.</p>	
<p>The Quartus II software version 7.1 Power Analyzer enhances the accuracy of the maximum static power estimate for Stratix II and Stratix II GX devices. The maximum static power drawn from the VCCPD power supply for Stratix II and Stratix II GX devices utilizing maximum power characteristics increases in the Power Analyzer power estimate by at most 15mW (depending on the device size.)</p>	

Description	Workaround
<p>The Quartus II software version 7.1 issues the error:  “Error (10621): VHDL Use Clause error at &lt;location&gt;: more than one Use Clause imports a declaration of simple name "&lt;name&gt;" -- none of the declarations are directly visible.”</p> <p>However, the Quartus II software version 7.0 and earlier did not issue the error for the same design.</p> <p>This changed behavior arises when a design imports overloaded subprograms with the same signature from different packages such as STD_LOGIC_UNSIGNED and STD_LOGIC_SIGNED. Both these packages define binary operations on STD_LOGIC_VECTOR arguments. Earlier versions of the software incorrectly favored the first imported declaration.</p>	<p>Remove one of the conflicting Use Clauses. For example, use either STD_LOGIC_SIGNED or STD_LOGIC_UNSIGNED, but not both.</p>
<p>By default, the PowerPlay Power Analyzer will use statistical or vectorless estimation techniques to derive signal activities for signals for which simulation data or specific power toggle rates are unavailable. This is true for all MAX II, 90nm device families, and 65nm device families.</p> <p>Prior to the Quartus II software version 7.1, vectorless estimation did not analyze signal activities of nodes in sequential feedback loops. In the Quartus II software version 7.1, vectorless estimation has been updated to perform preliminary analysis on these nodes. Note that this behavior results in an increased dynamic power estimate for circuits with sequential feedback loops when vectorless estimation is used to calculate the signal activities.</p>	

Description	Workaround
<p>The format for Conversion Setup Files (.cof) has changed. The element defined below (in DTD syntax) has been introduced:</p> <pre data-bbox="250 426 797 785"> &lt;!ELEMENT hex_block (hex_filename,hex_addressing, hex_offset)&gt; &lt;!ELEMENT hex_filename (#PCDATA)&gt; &lt;!ELEMENT hex_addressing (#PCDATA)&gt; &lt;!--hex_addressing value is either relative or absolute --&gt; &lt;!ELEMENT hex_offset (#PCDATA)&gt; </pre> <p>In addition the following elements have been deprecated:</p> <pre data-bbox="250 942 761 1157"> &lt;!ELEMENT bottom_boot_block (bottom_boot_filename,bottom_ addressing)&gt; &lt;!ELEMENT main_block (main_filename, main_addressing)&gt; </pre>	
<p>Adaptive Equalization in Stratix II GX transceivers has been disabled.</p>	<p>Disable the use of Adaptive Equalization in the design, and contact Altera Technical Support at <a href="http://www.altera.com/mysupport">www.altera.com/mysupport</a> and click “Create New Service Request.”</p>

Description	Workaround
<p>A key change in SOPC Builder version 7.1 is the new file format for storing system design data. Previously, SOPC Builder used a proprietary file format (PTF) to store system designs, while SOPC Builder version 7.1 uses an industry-standard XML file format for data storage. By convention, these files are given the extension <b>.sopc</b>. When you open an SOPC Builder system created in a previous version of the tools, you are asked to upgrade the system to the new format. Click <b>More Information</b> in that dialog box for details on migrating your projects and the changes in SOPC Builder file formats.</p>	
<p><b>Version 6.1</b></p>	
<p>A minor change has been made to the power breakdown between I/O power and Core power in the PowerPlay Power Analyzer report. The total power dissipated on the device and the total current drawn from each voltage supply are unaffected. I/O routing power refers to the power dissipated by device core routing resources that are driven by input I/O cells. In Quartus II software versions 6.0 and 6.0 SP1, I/O routing power was reported on the PowerPlay Power Analyzer Summary report section as I/O power rather than core dynamic power. For a typical design, the net change is less than 2% of power from I/O Power to Core Dynamic Thermal Power Dissipation in the Summary report section of the PowerPlay Power Analyzer. Also, the Core Dynamic Thermal Power Dissipation by Clock Domain report section did not enumerate the I/O routing power.</p>	

<p>Designs that contain a user-edited Memory Initialization File (<b>.mif</b>) that compile successfully in earlier versions of the Quartus II software may fail with the error "File &lt;filename&gt;.mif contains illegal syntax at line &lt;num&gt;" in the Quartus II 6.1 software. These Memory Initialization Files contain illegal syntax. Illegal Memory Initialization Files were ignored by previous releases of the software.</p>	<p>Correct the syntax of the Memory Initialization File by referring to the Memory Initialization File syntax description in the Quartus II Help, or create a new Memory Initialization File with the Quartus II software.</p>
<p>You may receive the following warnings when you use the <code>write_sdc</code> command in the TimeQuest Timing Analyzer:</p> <p>"Warning: Ignored assignment <code>create_generated_clock</code>"</p> <p>"Warning: Collection filter Positional argument &lt;source_objects&gt; with value [get_nodes Pll_Inst\ altpll_component\ pll\ clk\[0\]] requires type (port pin reg kpr net ), but found type node."</p> <p>You receive these warnings because the <code>create_clock</code> or <code>create_generated_clock</code> assignments are ignored by the TimeQuest Timing Analyzer when using <code>get_nodes</code> collections. This issue is most likely to occur when using a Synopsys Design Constraints File (<b>.sdc</b>) generated from the Quartus II software version 6.0 or 6.0sp1 using the <code>write_sdc</code> command.</p>	<p>Change the <code>get_nodes</code> command to use one of the following commands: <code>get_ports</code>, <code>get_pins</code>, <code>get_nets</code>, <code>get_registers</code>, or <code>get_keepers</code>.</p>

<b>Version 6.0 SP1</b>	
In the Quartus II software version 6.0 and earlier, when you created a receiver-only instance of the alt2gxb megafunction, a CMU PLL was created that has pll_inclk and pll_locked ports. These ports prevented the combination of two receiver-only implementations at different data rates in the same quad.	In the Quartus II software version 6.0 SP1, a CMU PLL is no longer created when you create a receiver-only instance. You must recreate the megafunction instance with the <b>MegaWizard Plug-In Manager</b> or manually remove the pll_inclk and pll_locked ports from the wrapper file.
<b>Version 6.0</b>	
The TimeQuest Timing Analyzer's <b>QSF2SDC</b> conversion utility cannot properly convert all Classic Timing Analyzer timing assignments. The results from the TimeQuest Timing Analyzer may also be different from the Classic Timing Analyzer due to other default behavior differences.	The <b>QSF2SDC</b> conversion utility is considered a guide to help reduce the time to switch to the TimeQuest analyzer, and it is not intended to make the TimeQuest analyzer a plug-in replacement for the Quartus II Classic Timing Analyzer. You should review all converted SDC constraints for correctness and completeness. Refer to the <i>Switching To the TimeQuest Timing Analyzer</i> chapter in the Quartus II Software Handbook for more information.
For designs that target Stratix II GX devices, that use the alt2gxb megafunction in a transmitter-only configuration, the loop_filter_resistor_control value was not correctly written to the megafunction instance.	Use the MegaWizard Plug-In Manager in the Quartus II software version 6.0 to generate a new instance of the alt2gxb megafunction.
If you created a Verilog Quartus Mapping File (.vqm) for a design containing the alt2gxb megafunction in its XAUI configuration with the Quartus II software version 5.1 SP2 or earlier, the setting for <b>Force Signal Detect</b> was incorrectly set to false.	You should regenerate the alt2gxb instantiation in a XAUI configuration using the Quartus II software version 6.0.
Beginning in the 6.0 release, the Quartus II Parallel Flash Loader megafunction (altparallel_flash_loader) erases flash memory blocks before programming them.	No action is required.

<p>Beginning in the 6.0 release, Quartus II integrated synthesis handles bidirectional pins differently. For example if <code>bidir1</code> and <code>bidir2</code> are declared as <code>inouts</code>, the assignment <code>bidir1 &lt;= bidir2</code> creates a directional connection in which data flows from <code>bidir2</code> to <code>bidir1</code>. In the Quartus II software version 5.1 and earlier, a bidirectional connection was created.</p>	<p>If your design requires that data flow in both directions, you must directly connect the bidirectional pins together without using an assignment statement. Assignment statements always produce a unidirectional data flow.</p>
<p>The method the Quartus II NativeLink interface uses to locate other EDA tools changed in this release. You might receive a message indicating that the tool cannot be found when you launch it through the NativeLink interface.</p>	<p>You must specify the path to the EDA tool program file on the <b>EDA Tool Options</b> page of the <b>Options</b> dialog box, or with the <code>set_user_command</code> Tcl command.</p>
<p><b>Version 5.1 SP2 and earlier</b></p>	
<p>Beginning with version 5.1, implicit or explicit declarations inside unnamed <code>generate</code> blocks are no longer visible outside the <code>generate</code> block.</p>	<p>Declare the object outside the <code>generate</code> block. You can also add a name to the <code>generate</code> block and refer to the object with a hierarchical name.</p>

<p>The following primitives now use a new library instead of the <b>altera_mf</b> library:</p> <p>CARRY          CARRY_SUM          CASCADE          CLKLOCK          EXP          GLOBAL          LUT_INPUT          LUT_OUTPUT          ROW_GLOBAL          TRI          SOFT          OPNDRN          DFF          DFFE          DFFEA          JKFF          JKFFE          DFFEAS          LATCH          SRFF          SRFFE          TFF          TFFE          ALT_INBUF          ALT_IOBUF          ALT_OUTBUF          ALT_OUTBUF_TRI</p>	<p>To perform functional simulations in Verilog HDL, you must use the <b>altera_primitives.v</b> library located in the &lt;Quartus II installation directory&gt;\eda\sim_lib directory. For VHDL, you must use the <b>altera_primitives.vhd</b> library located in the &lt;Quartus II installation directory&gt;\eda\sim_lib directory. The VHDL component declaration file is located in the <b>altera_primitives_components.vhd</b> library in the &lt;Quartus II installation directory&gt;\eda\sim_lib directory.</p>
<p>Designs compiled with the Quartus II software version 5.0 and earlier could fail their boundary-scan test (BST) if the test expected all input buffers to be active after device configuration. Under some circumstances, unused input buffers are disabled by the Quartus II software to minimize power usage in Stratix II, Cyclone II, and MAX II device families.</p>	<p>Beginning in version 5.0 Service Pack 1, the Quartus II software supports the <b>always_enable_input_buffers</b> option to prevent unused input buffers from being disabled during configuration.</p>
<p>In the Quartus II software version 5.0 and later, you can assign the <b>Allow XOR Gate Usage</b> logic option to individual nodes and entities. In previous versions, you could apply this logic option only to the entire design (that is, it was a global logic option).</p>	

<p>In the Quartus II software versions 5.0, 5.1, 6.0, and 6.1, if your Quartus II Settings File (.qsf) contains an error, you cannot compile the project until the error has been corrected. In previous versions, a warning message was displayed and compilation continued. In the Quartus II software version 6.1, a different error message from previous versions is generated.</p>	
<p>In the Quartus II software version 5.0 and later, the <code>\altera\qdesigns&lt;version number&gt;\ll_makefile</code> directory has been replaced by the <code>\altera\qdesigns&lt;version number&gt;\logiclock_makefile</code> directory.</p>	
<p>The altgxb megafunction has been updated in the Quartus II software version 5.0. Any Stratix GX project that used the altgxb megafunction and was archived with the <b>Include functions from system libraries</b> option turned on will not compile correctly.</p>	<p>You must delete the <b>altgxb.tdf</b> file that is included in the project archive, and recompile your design.</p>
<p>The following megafunctions have clear box models that contain assignments that are not stored in the Quartus Settings File (.qsf) and are not written out to a Verilog Quartus Mapping File (.vqm):</p> <ul style="list-style-type: none"> <li>altdqs</li> <li>altdq</li> <li>altddio_bidir</li> <li>altddio_out</li> <li>altddio_input</li> <li>atlvds_rx</li> <li>atlvds_tx</li> <li>altufm_i2c</li> <li>dcfifo</li> <li>alt2gxb_reconfig</li> </ul>	<p>Do not save your atom netlist file as a Verilog Quartus Mapping file if you are using these megafunctions.</p>
<p>When you are using formal verification tools with a design that contains LogicLock regions that was compiled with the Quartus II software version 3.0 or earlier, under certain circumstances when you open the design in the Quartus II software version 4.0 and later, the LogicLock regions will not be handled properly.</p>	<p>Redefine the LogicLock regions in the Quartus II software version 4.0 or later to eliminate the errors.</p>

# Known Issues & Workarounds

## General Quartus II Software Issues

Issue	Workaround
<b>Version 7.1 SP1</b>	
<p>If you are using the alt2gxb megafunction with the specifications below, the alt2gxb megafunction does not generate reference clock divider for the design:</p> <ul style="list-style-type: none"> <li>• Protocol is set to <b>Basic</b>.</li> <li>• The data rate is set to a value in MHz that, after converted to picoseconds, would generate a floating point value.</li> <li>• The equation <math>\text{data rate} / (2 * \text{input clock frequency})</math> generates a value of 2, 2.5 and 12.5 for data rate lower or equal to 3125 MHz designs and generated a value of 4, 5 and 12.5 for designs with data rate more than 3125 MHz..</li> </ul>	<p>In order to generate refclk divider for these designs, manually add the parameter <code>enforce_refclk_divider</code> with the value <code>true</code> to the alt2gxb megafunction instantiation in the wrapper generated by alt2gxb MegaWizard.</p>
<b>Version 7.1</b>	
<p>During Analysis &amp; Synthesis, the memory transformation power optimization may be controlled by the <code>optimize_power_during_synthesis</code> Quartus II Settings File (.qsf) variable and the parameter <code>low_power_mode</code>. During Place &amp; Route the optimization may be controlled by the <code>optimize_power_during_fitting</code> setting. This setting may be applied globally or on a per-entity basis.</p>	
<p>If you open the <b>Print</b> dialog box or the <b>Page Setup</b> dialog box in the Quartus II software, and if you use an HP Business Inkjet 1200 series printer, the Quartus II software may produce an unexpected error.</p>	<p>If you have this printer, Altera recommends updating to the latest version of the drivers, available for free download from the HP website.</p>

Issue	Workaround
<p>When using a PLL in source-synchronous mode to compensate a bus of input signals, the Quartus II software incorrectly sets the I/O delay chain to 0 for only one of the bits in the bus, instead of all bits in the bus. This setting can result in I/O timing violations and skew between the bits in the bus, especially when the source-synchronous mode is not used properly. This issue affects designs using PLLs in source-synchronous mode that target Cyclone II, Cyclone III, HardCopy II, Stratix II, Stratix II GX, and Stratix III devices. This issue also affects designs using altlvds megafunctions that target Cyclone II and Cyclone III devices.</p>	<p>Manually make delay chain assignments of 0 for all bits in a bus being compensated by the PLL in source-synchronous mode, and correctly use the source-synchronous mode (for example, ensure clock and data are edge aligned at the pins using timing constraints, and use a phase-shift of -180 degrees to center the clock in the data window at the I/O input register).</p>
<p>The node names in the RTL Viewer and the Technology Map Viewer do not always match. These node names are internally created nodes. If any assignment on these nodes is necessary, Altera recommends that you use the node name in the Technology Map Viewer rather than the name in the RTL Viewer.</p>	<p>The driver source or fan-out destination or destinations for the node might have a matching name. The source or destination can be found by using the <b>Filter</b> command in the RTL Viewer or the Technology Map Viewer.</p>
<p>The <code>set_operation_conditions</code> command may not properly update delays in certain types of combinational loops.</p>	<p>The use of combinational loops should be avoided. However, to obtain correct delays in combinational loops, delete and re-create the timing netlist, and specify the timing corner in the <b>Create Timing Netlist</b> dialog box on the Netlist menu in the TimeQuest Timing Analyzer, or the <code>-model</code> option to <code>create_timing_netlist</code> in Tcl. The <code>set_operating_conditions</code> command can also be used before the first call to <code>update_timing_netlist</code> after creating or recreating the netlist.</p>
<p>The timing analysis for the soft-CDR support is not supported in the Quartus II software version 7.1. Appropriate timing constraints are not yet automatically generated by the TimeQuest timing analyzer, and the TimeQuest analyzer reports failures for the path from the recovered clock to the core registers.</p>	<p>Manually create the timing constraints if you want timing analysis performed on your soft-CDR design.</p>

Issue	Workaround
<p>The SignalTap II Logic Analyzer occasionally exits unexpectedly when you follow these steps:</p> <ol style="list-style-type: none"> <li>1. Maximize the window and rename the instance.</li> <li>2. Close the window, and open the SignalTap II Logic Analyzer again. The <b>Close</b> button is not visible.</li> <li>3. Create a new Vector Waveform File (<b>.vwf</b>) and then close it.</li> <li>4. Detach the SignalTap II window.</li> </ol>	<p>To avoid this error, follow these steps:</p> <ol style="list-style-type: none"> <li>1. You can click <b>Close</b> on the File menu to close the window or right-click the tab and click <b>Close</b>.</li> <li>2. Resize or maximize the Quartus II window, or detach and reattach the window and the <b>Close</b> button reappears.</li> </ol>
<p>The Resource Property Editor, Chip Planner, or both may crash after closing the TimeQuest Timing Analyzer.</p>	<p>Don't close the TimeQuest analyzer before using the Resource Property Editor, Chip Planner, or both.</p>
<p>If you use an OpenCore Plus license and designs or IP cores that contain high-speed I/O, such as LVDS or transceiver blocks; or if you partition a design that contains atoms to merge, it can cause a no fit.</p>	<p>To avoid this issue, turn off Incremental Compilation:</p> <ol style="list-style-type: none"> <li>1. Click <b>Settings</b> on the Assignments menu.</li> <li>2. In the <b>Settings</b> dialog box, select <b>Incremental Compilation</b> under <b>Compilation Process Settings</b> in the <b>Category</b> list.</li> <li>3. Under <b>Incremental compilation</b>, select <b>Off</b>.</li> </ol>
<p>In the alt2gxb MegaWizard Plug-In Manager, when you select the <b>Channel interface</b> option under <b>Dynamic Reconfiguration Settings</b>, a new page, <b>Reconfig 2</b>, appears with table with a list of ports you can check to add those ports to the design. Sometimes the wizard turns off a port you just turned on and you are unable to add that port to the design.</p>	<p>Manually add the port to the wrapper in three places: the module declaration section, the port declaration section, and the connection section. In the module declaration, add the port name between the parenthesis module <code>design_name(..., port_name, ...)</code>. In the port declaration section, add the port name and width after the module declaration as <code>input [1:0] port_name;</code> for a bus and <code>input port_name;</code> for a wire. In the connection section, users need to add <code>.port_name(port_name)</code>, after <code>alt2gxb alt2gxb_component(</code> and before <code>// synopsys translate_off</code>. Users also need to remove the line <code>.port_name()</code>, between <code>// synopsys translate_off</code> and <code>// synopsys translate_on</code>.</p>

Issue	Workaround
<p>If you change the I/O standard in the <b>Group</b> list in the Pin Planner and a bus of pins, and then run Analysis &amp; Synthesis, the I/O standard is not updated.</p>	<p>Either run <b>quartus_map</b> again or manually change the Quartus II Settings File (<b>.qsf</b>) assignment to that of each member of the bus (for example, <code>&lt;my name&gt;[0] = "&lt;assignment&gt;"</code>).</p>
<p>For all 6G basic modes, when a configuration is using the local clock divider setting of <b>2</b> or <b>4</b>, the maximum effective data rate is <math>6375 / 2</math> or <math>6375 / 4</math>. The alt2gxb megafunction currently does not allow users to set the data rate to <b>6375</b> and local clock divider setting to <b>2</b> or <b>4</b> in certain modes.</p>	<p>Set the local clock divider to 1 and set the data rate within the range allowed by the wizard, and then continue with the wizard as usual and click Finish to generate the design wrapper. Then open the wrapper in any text editor and adjust the values of these eight parameters: <code>cmu_pll_inclock_period</code>, <code>rx_cru_inclock_period</code>, <code>rx_data_rate</code>, <code>tx_data_rate</code>, <code>rx_data_rate_remainder</code>, <code>tx_data_rate_remainder</code>, <code>rx_cru_pre_divide_by</code>, and <code>tx_refclk_divide_by</code>. The <code>cmu_pll_inclock_period</code> and <code>rx_cru_inclock_period</code> settings must be the same and they are equal to the inclock period in ps. The <code>rx_data_rate</code> and <code>tx_data_rate</code> settings must also be the same and they should be set to effective data rate multiplied by the local clock divider setting in Mbps. They also must be integers and the remainders are set by modifying the <code>rx_data_rate_remainder</code> and <code>tx_data_rate_remainder</code> settings in bps. The <code>tx_refclk_divide_by</code> and <code>rx_cru_pre_divide_by</code> parameters set the local clock divider. They must have the same value and should be set to 2 or 4.</p>

Issue	Workaround
<p>Designs containing external memory interfaces created using the altmempy megafunction or memory controllers such as DDR, DDR2, and DDR3 may produce the following error if the design partition containing the memory interface is set to <b>Post-Fit</b> in the <b>Netlist Type</b> option:</p> <pre> "Internal Error: Sub-system: FSAC, File: /quartus/fitter/fsac/fsac_titan _dqs_util.cpp, Line: 1840 IO_CLOCK_DIVIDER atom found with no DQ GROUP association." </pre>	<p>Do not use the <b>Post-Fit</b> partition type for the partition containing the memory interface.</p>
<p>In the <b>.flexlmrc</b> file in your home directory on UNIX, if a stray newline character is inserted in a license specification, all Quartus II tools crash (including the flexlm tools <b>lmutil</b> and <b>lmgrd</b>).</p>	
<p>When you instantiate a transceiver channel and enable adaptive equalization in the alt2gxb megafunction, the <code>fixedclk</code> signal is missing.</p>	<p>Manually edit the Verilog Design File (<b>.v</b>) or VHDL Design File (<b>.vhd</b>) produced by the MegaWizard Plug-In Manager, to add a new top-level 1-bit input signal with the name <code>fixedclk</code>. Connect <code>fixedclk</code> to a signal of the same name in the alt2gxb megafunction. The <code>fixedclk</code> port on the alt2gxb component must be moved above the port instantiation list that reads</p> <pre> // synopsys translate_off </pre> <p>Or, you can enable adaptive equalization in the MegaWizard Plug-In Manager, and click Channel Interface to open the <b>Reconfig2</b> page in the MegaWizard. However, this action exposes the full width of all used ports, which makes it more difficult to connect the alt2gxb megafunction.</p>
<p>The alt2gxb megafunction does not support the <b>Generate a netlist for synthesis area and timing estimation</b> option with adaptive equalization enabled.</p>	

Issue	Workaround
<p>When recompiling a design with the Triple-Speed Ethernet MegaCore Function, the Triple-Speed Ethernet core is generated, and it adds itself to the list of Quartus II design files. If you receive a pre-compiled design that contains a Triple-Speed Ethernet core (for instance, any TSE_SGDMA example design), delete the previously-added <b>tse_mac.v</b> file.</p>	
<p>When you use the altmemphy megafunction to create a QDRII memory interface, the design may get a no-fit in the Quartus II software due to an over use of global signals.</p>	<p>Apply the following assignment to your project:</p> <pre>set_instance_assignment -name GLOBAL_SIGNAL OFF -to *dqs_delayed2</pre>
<p>When a top-level port is declared as inout, but used only in the input direction (that is, only the input buffer is used), then the PrimeTime Verilog Output File (<b>.vo</b>) contains a stratixiii_io_obuf or cycloneiii_io_obuf atom instance driving the inout port to constant 1. As a result, PrimeTime does not report paths from the inout port.</p>	<p>Change the type of the port from inout to input in the original design and recompile the design, or edit the Verilog Output File by finding the stratixiii_io_obuf or cycloneiii_io_obuf atom instances that drive the inout port, and for each of the instances found, replace V<sub>CC</sub> with GND on the OE pin connection.</p>
<p>The <b>prev_cmp_&lt;revision name&gt;.qmsg</b> file, which contains messages from the previous compilation for use with the <b>Hide Previous Compilation Messages</b> command, is placed in the project main directory.</p>	<p>You can safely delete the <b>prev_cmp_&lt;revision name&gt;.qmsg</b> file, if you don't need to use the <b>Hide Previous Compilation Messages</b> command in the Messages window. It is not a required file for the project.</p>
<p>Altera recommends that all soft-CDR channels driven by a PLL are within a distance of 25 SERDES rows (including the unbonded SERDES) from that PLL.</p>	

Issue	Workaround
<p>When using the Quartus II software version 7.1 to edit an altmemphy variation generated with the Quartus II software version 6.1 or 7.0, you will see errors reported by the Quartus II synthesis reporting that modules cannot be declared more than once if you had previously added all the altmemphy source files to your project. This occurs because the generated source files have changed in 7.1, and you now have a mix of source files from 7.1 and 6.1/7.0 in your project.</p>	<p>Delete the <b>.v.vhd</b> source files that match the pattern “*alt_mem_phy*” and remove them from your project file list before editing the altmemphy variation.</p>
<p>For designs which include multiple altmemphy instances and use dedicated clock outputs, the input clock timing constraints are not created correctly.</p>	<p>Create the input clock timing constraints manually with an Synopsys Design Constraints File (<b>.sdc</b>) script that creates a clock on the input of each of the PLLs inside the altmemphy megafunction instantiations, and add this file to the project before the SDC File scripts that constrain the altmemphy instances.</p> <pre data-bbox="815 1054 1377 1297"> #Example SDC   create_clock -period     &lt;ref_clock_period_in_ns&gt;     &lt;node_name_of_pll1_inclk&gt; create_clock -period   &lt;ref_clock_period_in_ns&gt;   &lt;node_name_of_pll2_inclk&gt; </pre>

Issue	Workaround
<p>The altdio_in and altdio_bidir megafunction behavioral models (under altera_mf – both Verilog and VHDL) show incorrect behavior for the Stratix device family (including Stratix GX and Hardcopy Stratix devices) and the Stratix II device family (Stratix GX and Hardcopy II devices) when the sclr or sset port is used.</p> <p>They incorrectly show the behavior as if the design targeted Stratix III devices. When designing with Stratix III devices in the altdio_in and altdio_bidir Double Data Rate megafunctions, when the synchronous clear or synchronous preset is asserted, it synchronously clears or presets the inputs as well as the resynchronization register. But for all other families, the synchronous clear/preset should not affect the resynchronization latch.</p>	<p>Run atom simulation models to get the correct behavior.</p>
<p>The Design Assistant shows that a violation occurred in a WYSIWYG primitive, but the warnings should be suppressed.</p>	<p>Suppress all Design Assistant warnings for WYSIWYG components.</p>
<p>When using adaptive equalization in the alt2gxb_reconfig megafunction, reconfig_mode_sel must be set to either 0111 or 1000. You must wait for at least 2 cycles after changing reconfig_mode_sel to these values before activating the adaptive equalization soft IP via the write_all strobe.</p>	
<p>For designs that include multiple instantiations of the altmemphy megafunction, or High Performance DDR Controllers, and have the <b>Use dedicated PLL outputs to drive memory clock</b> option set, the timing analysis for the DQS vs CK and Address/command paths may be incorrect. This will be visible by a setup or hold margin on these paths that is greater than a full cycle, and a corresponding negative margin on the other side.</p>	<p>Contact Altera Technical Support at <a href="http://www.altera.com/mysupport">www.altera.com/mysupport</a> and click “Create New Service Request.”</p>

Issue	Workaround
<p>When you launch documentation (PDF and HTML files) from the MegaWizard Plug-In Manager, the MegaWizard uses the <b>Web browser</b> option in the <b>Internet Connectivity</b> page of the Quartus II <b>Options</b> dialog box. The MegaWizard will sometimes use a setting from a previous version of the Quartus II software than the present version. This can lead to errors if the web browser does not exist on your machine.</p>	<p>Manually edit the WEB_BROWSER variable in the <b>quartus2.ini</b> file and remove the reference to the non-existent web browser.</p>
<p>When simulating an altmemphy QDRII Stratix III-generated variation, the functionality of the byte enable signal is correct only for 9-bit-wide QDRII memories.</p>	<p>To simulate correctly for 8-, 18-, or 36-bit wide memories, disconnect the connection of the byte enable signals between the variation and the memory model, and tie the byte enable input to the memory model low.</p>
<p>When compiling an altmemphy QDRII Stratix III-generated variation where you have enabled the Dynamic Parallel On-Chip Termination option in the altmemphy MegaWizard Plug-In Manager, the Quartus II software crashes with the following error message:</p> <pre>Internal Error: Sub-system: FSAC, File: /quartus/fitter/fsac/fsac_titan _dqs_config_op.cpp, Line: 557 dqs_config_cell != 0</pre>	<p>Disable the <b>Dynamic Parallel On-Chip Termination</b> option in the altmemphy MegaWizard Plug-In Manager, and regenerate the variation before recompiling in Quartus II software.</p>
<p>The following cores may fail to run when the PERL5LIB environment variable is set:</p> <ul style="list-style-type: none"> <li>• ED8B10B Encoder/Decoder</li> <li>• POS-PHY Level 4</li> <li>• Rapid IO</li> <li>• SerialLite II</li> </ul>	<p>Unset the PERL5LIB environment variable, and restart the Quartus II software.</p>
<p><b>Version 6.1</b></p>	
<p>When you use the altparallel_flash_loader megafunction in Quartus II software version 6.0 and earlier, the design may not compile successfully.</p>	<p>Regenerate the altparallel_flash_loader megafunction with the current version of the Quartus II software.</p>

Issue	Workaround
<p>If <b>Export version-compatible database</b> in the <b>Compilation Process Settings</b> page is turned on, using the <b>Check &amp; Save All Netlist Changes</b> command causes an Internal Error during the database export phase of the fit.</p>	<p>Turn off <b>Export version-compatible database</b> in the <b>Compilation Process Settings</b> page before using the <b>Check &amp; Save All Netlist Changes</b> command.</p>
<p>You may get one or more messages "Error: Can't generate programming files for project because design file "&lt;name&gt;" is encrypted. It does not have license file support that allows generation of programming files" from the Assembler when compiling a design that is using Altera IP with the OpenCore Plus evaluation feature when your design has VHDL source files that have the construct "use work.all;".</p>	<p>The errors are reported for IP source files that were added to your project by IP Toolbench, but which are not actually used during compilation. Remove the files listed in the error messages from your project file list and recompile the design.</p>
<p>Running the PowerPlay Power Analyzer directly following an ECO fit results in an Internal Error.</p>	<p>Run the Classic Timing Analyzer (quartus_tan) or the TimeQuest Timing Analyzer (quartus_sta) before you run the PowerPlay Power Analyzer (quartus_pow).</p>

Issue	Workaround
<p>The Quartus II software version 6.1 may run out of memory when Formal Verification is turned on and you are using the Quartus II Integrated Synthesis flow. This happens only when Quartus II Integrated Synthesis extracts finite state machines from the design.</p>	<p>To avoid the out of memory issue in the Quartus II software version 6.1, turn off state machine extraction and rerun synthesis. To turn off state machine extraction, use the following settings in the Quartus II project:</p> <pre>set_global_assignment -name EXTRACT_VERILOG_STATE_MACHINES OFF set_global_assignment -name EXTRACT_VHDL_STATE_MACHINES OFF</pre> <p>You can also use the Quartus II GUI:</p> <ol style="list-style-type: none"> <li>1. On the Assignments menu, click <b>Settings</b>.</li> <li>2. Select <b>Analysis &amp; Synthesis Settings</b>, and click <b>More Settings</b>.</li> <li>3. Turn off <b>Extract Verilog State Machines</b> and <b>Extract VHDL State Machines</b>.</li> </ol>
<p>When a design contains IP that is evaluated using the OpenCore Plus hardware evaluation feature, the Quartus II software produces a sequence of Info messages beginning with Info: Elaborated megafunction instantiation "pzdyqx:nabboc".</p>	<p>These messages can be safely ignored.</p>
<p>When viewing a web page or PDF from a MegaWizard, the MegaWizard may try to launch a web browser other than that which is specified on the <b>Internet Connectivity</b> page in the <b>Options</b> dialog box. Instead of using the currently defined web browser, the MegaWizard is using a web browser defined by a previous version of the Quartus II software. If the browser does not exist, you may receive the following error:</p> <pre>"Problem opening web browser for &lt;path&gt;/&lt;user_guide_name&gt;"</pre>	<p>Manually edit the <b>quartus2.ini</b> file and ensure that all instances of the <b>WEB_BROWSER</b> variable point to a valid web browser installation.</p>

Issue	Workaround
<b>Version 6.0 SP1</b>	
Running multiple instances of the Quartus II software using the same Quartus Project File (.qpf) may cause unpredictable results or may cause the Quartus II software to crash.	Altera recommends that you not open multiple instances of the Quartus II software using the same project.
<b>Version 6.0</b>	
In the classic Timing Analyzer, when a clock (base or derived) is assigned to an internal register, then data paths to and from the register are not analyzed for clock setup and clock hold analysis.	First, analyze the design with the clock settings assigned to the internal registers. Then remove the clock settings from the internal registers and perform a second analysis, checking only paths to and from those registers. The other resolution is to use the TimeQuest Timing Analyzer instead of the classic Timing Analyzer.
If you change an I/O primitive assignment or an altera_attribute assignment, or any assignment made in a Verilog HDL or VHDL design file, the assignment may not be applied to the design database correctly in the next compilation.	Delete the <project>\db directory and recompile the design.
The <b>SignalProbe</b> dialog box may take a long time to open, so it appears that the Quartus II software is “hanging.” The delay is dependent upon the size of the netlist and the number of device pins.	Do not open the <b>SignalProbe</b> dialog box while a compilation is in progress.
The TimeQuest Timing Analyzer erroneously analyzes paths to the asynchronous data pins of registers (that is, the adata pin) during a recovery/removal analysis.	Apply the set_false_path command from the asynchronous data signal’s source port or register to declare these paths as false paths.
If you change the type of a parameter setting in the Quartus II Settings File (.qsf) or a Block Design File (.bdf) and recompile your design, your change appears to have no effect. The type of a parameter is denoted by appending a prefix such as “B” (binary), “D” (decimal). For example, B“10101” represents the binary string “10101”, but D“10101” represents the decimal number 10101.	Delete the <project>\db directory and recompile the design.

Issue	Workaround
<b>Version 5.1 SP2 and earlier</b>	
Due to a limit of the Windows operating system, path names longer than 229 characters can cause an internal error in the Quartus II software.	Make sure that all path names do not exceed 229 characters. This limitation applies to UNIX and Linux installations also.
When you are using the Chip Editor to delete the connections in carry chains, the destination node must be in a legal location for the carry chain. If this is not the case, you will not be able to undo the operation or any prior operations.	Perform the following steps: 1. Delete the <b>Remove-Chain</b> command in the Change Manager. 2. Move the node back to its legal position. 3. Recreate the chain in the Resource Property editor. 4. Move the node to the desired position.
If your design contains illegal pin assignments, and you open the Resources window in the Pin Planner, the Quartus II software may crash.	Remove any illegal pin location assignments before opening the Resources window.
If you make a single-point CUT=ON assignment to a node, and then override it with a point-to-point CUT=OFF assignment on a specific path, the OFF assignment will not be honored.	
You may receive a "License not found..." error if the path to the license file contains non-ASCII characters.	Change or remove any non-ASCII characters from the license file path.
During a SignalProbe™ compilation, you might receive warning message(s) similar to the following example: "Routing constraints for signal <signal_name> seem to be causing unresolvable routing congestion. The constraints for the signal were removed."	The Compiler issues these warnings when it is unable to retain the routing constraints from a previous compilation because those routing resources were needed by the SignalProbe signal routing.

Issue	Workaround
There is no distinction between output ports and bidirectional ports in AHDL Function Prototypes; instead, all ports listed after the RETURNS keyword are treated as output ports. As a result, if you specify a bidirectional port in a logic function's Function Prototype Statement and do not connect the port to a top-level bidirectional pin or to other logic in the design where you instantiate the logic function, an error can occur.	Connect the port to a top-level bidirectional pin or to other logic in the design.
Context-sensitive Help is not available for some items in the Quartus II software.	To locate Help on those items, click <b>Search</b> on the Help menu, and type the name of the item.
The Classic Timing Analyzer does not recognize non-PLL clock signals when using any PLL megafunction.	Make clock settings assignments to all non-PLL clocks.
The Waveform Editor does not allow you to create a bus with nodes that are nonconsecutive members of a bus.	Create buses only with nodes that are consecutive members of a bus. Or, use the <b>Group</b> command on the Edit menu to create groups of arbitrary nodes.
If you are using the altcam, altclklock, altlvds_rx, or altlvds_tx megafunctions, the equations shown in the Equations Section of the Compilation Report are not complete.	To view the complete equations for any of these megafunctions, use the Equations window of the Timing Closure Floorplan.
The Quartus II software does not support design file names with more than one extension. For example, you cannot use the file name <b>file.eda.edif</b> .	Use design file names with only one extension.
If you install the Quartus II software for PCs on a UNIX server that exports shares with the Samba software version 1.9.18p10, you may experience problems accessing project files that are also on the network.	Altera recommends using version 1.9.16p11 or 2.0 of the Samba software.
If you make assignments to reserve pins as a group or with group notation (debug [7..0] ), the Quartus II software does not correctly generate simulation output files, and you receive a warning message saying "Unsupported data type in the top-level module."	Reserve the pins using single-name notation (for example, debug [7] , debug [6] , and so on).

Issue	Workaround
Do not change the file permissions (such as changing “read-only” to “read and write”) of Quartus II Settings File (.qsf) and Quartus II Project File (.qpf) while a Quartus II project is open.	Close the Quartus II project before making changes to the file permissions.
Node names containing numbers greater than $2^{31}-1$ (2147483647) will cause an Internal Error in the Quartus II software.	Do not use node names containing large numbers.
Occasionally the Programmer does not allow you to use a MAX 7000AE Programmer Object File (.pof) with a MAX 7000AE device. This error sometimes occurs after a compatible MAX 7000B device is used with the MAX 7000AE POF.	Do not switch between compatible MAX 7000B and MAX 7000AE devices when a MAX 7000AE POF is loaded, or reload the MAX 7000AE POF.
Routing back-annotation may fail if the back-annotated locations do not match the location assignments in the Quartus II Settings File (.qsf) or if the location assignments are missing. This problem can occur if you change devices, or if you remove some location assignments by using the <b>Assignment Editor</b> on the Assignments menu or by manually editing the Quartus II Settings File.	If you experience a “no fit” or an Internal Error while using routing back-annotation, delete the Routing Constraints File (.rcf) and back-annotate the design again after a successful compilation.
Occasionally, the Quartus II software may crash or hang with no error message immediately upon opening a project.	Delete the Quartus II Workspace File (.qws) <i>&lt;project name&gt;.qws</i> from the project directory. If the problem persists, delete the <i>&lt;project directory&gt;\db</i> directory and recompile the design.
When you are setting phase shift and duty cycle values for clock signals using the altpll megafunction, some combinations of settings may result in values that cannot be synthesized exactly. Under certain circumstances, the Quartus II software attempts to synthesize the phase shift parameter before the duty cycle parameter.	You should first select values for the parameter (phase shift or duty cycle) that is most important for your design.
During compilation or simulation, the Quartus II software may “hang” and not proceed to the next module if a menu or modal dialog box is open at the time the current module finishes running.	Close any open menus or modal dialog boxes before the compilation or simulation reaches the next stage.

Issue	Workaround
Running individual Quartus II software executables ( <b>quartus_map</b> , <b>quartus_fit</b> , and so on) from within the Quartus II Tcl Console may cause the Quartus II software to crash.	Run individual executables either from within the Quartus II scripting shell ( <b>quartus_sh</b> ) or directly at a command prompt.
The time shown in the Status window may not agree with the processing times reported in the Compilation Report. This difference is due to differences in how the times are calculated during processing.	
If you type a name in the entity column of the Assignment Editor that differs from an existing name only by case, the Assignment Editor's "auto-completion" feature always uses the existing name.	Type the new entity name in another application, such as a text editor, copy it to the clipboard, and paste the name from the clipboard into the Assignment Editor.
Altera recommends that you do not use node or entity names that differ only by case if you are using the Quartus II Simulator or Waveform Editor.	
Under certain circumstances, a design that uses <b>Virtual Pin</b> assignments may fail to fit after back-annotation. This situation occurs because the clock signals chosen automatically for the first compilation do not match those chosen for the second compilation.	Manually assign your clock signals, using <b>Virtual Pin Clock</b> assignments before the first compilation, or use Advanced Back-Annotation to explicitly write out the virtual clock assignments before the second compilation.
If you use the <code>dcfifo</code> or <code>scfifo</code> megafunctions in an AHDL design, you may receive an error message similar to "The parameter <code>LPM_WIDTHU</code> has been set to an invalid value..."	Either remove the <code>LPM_WIDTHU</code> parameter arguments from your AHDL <code>dcfifo</code> or <code>scfifo</code> megafunction instantiation, or explicitly set the <code>LPM_WIDTHU</code> parameter to <code>ceil(log2(LPM_NUMWORDS))</code> .
Do not open, change permissions, or delete the <code>/&lt;project directory&gt;/db</code> directory or any file therein while any Quartus II executable is running.	
If you are using the IP Toolbench and add a user library, the Quartus II software may add a backslash (\) to the end of the library file name. The Quartus II user interface ignores this trailing backslash.	

Issue	Workaround
<p>Support for non-decimal radix numbers (such as hexadecimal) used as constants in the <code>lpm_constant</code>, <code>lpm_compare</code>, and <code>lpm_add_sub</code> megafunctions is limited to values that can be represented by 31 bits or fewer.</p>	<p>For values that require more than 31 bits, use decimal radix only.</p>
<p>Under certain circumstances, back-annotation of routing in unreserved LogicLock regions can cause unsatisfiable routing constraints for signals going to clock and clock-enable ports of LABs. This can occur when other portions of the design are not back-annotated, and the Fitter populates empty LCELLs in the back-annotated LogicLock region during subsequent compilations.</p> <p>For example, assume that on the initial compilation, LogicLock region L contains register A, which uses the CLK1 and ENA1 ports of a LAB. When the design is recompiled, the Fitter may place register B, which is not part of region L, and uses the SLOAD input, in the same LAB as register A (assuming that the LAB has sufficient empty space to accommodate it).</p> <p>The LAB control signal generation block does not allow use of both ENA1 and SLOAD in the same LAB; therefore, register A must use the CLK0 and ENA0 ports, rather than CLK1 and ENA1. To avoid a no-route situation, the Fitter will ignore the routing constraints for the clock and enable signals, and re-route the signals using the appropriate control signal multiplexing for the CLK0 and ENA0 ports of the LAB. The Fitter picks the most appropriate routing and, in the majority of cases, the circuit's timing is not adversely affected. When the Fitter is forced to ignore routing constraints, info messages of the form "Info: Can't route signal &lt;name&gt; to atom &lt;name&gt;" are displayed to inform the user; the appearance of such messages is not a cause for alarm.</p>	<p>This situation can be avoided entirely by marking all LogicLock regions as Reserved, thereby preventing the Fitter from placing new items in a region. The tradeoff, of course, is that should a Reserved LogicLock region be under-utilized, the Fitter will be unable to place other logic items in the unused portion of the region.</p>

## Platform-Specific Issues

### Windows Platforms Only

Issue	Workaround
<b>Version 7.1</b>	
<p>The Quartus II software may crash with an internal error if you have set any number in the range 10000 – 11000 in the Message ID box of the Advanced Message Settings dialog box from the Analysis &amp; Synthesis page of the Settings dialog box.</p>	<p>Open your <i>&lt;project&gt;.qsf</i> file in a text editor and add the following assignment to it:  <code>set_global_assignment -name HDL_MESSAGE_OFF &lt;number&gt;</code>            Where <i>&lt;number&gt;</i> is the original message number.</p>
<p>On the Windows 2000 platform, the altlvds and the alt2gxb megafunctions fail to open the MegaWizard Plug-In Manager.</p>	
<b>Version 6.1</b>	
<p>After you commit any ECO changes, the detached Resource Property Editor displays old property values. This problem only happens on the currently displayed node.</p>	<p>Relocate the node into Resource Property Editor after you detach the Resource Property Editor.</p>
<p>If the Quartus II software is installed on a network drive, Windows is unable to start the JTAG server service because it does not have rights to read from the network drive (services run before users are logged in). If this service is not running, it is not possible for other computers to use JTAG cables on this machine. Occasionally it is not be possible for the Quartus II software to use JTAG cables attached to the same machine.</p>	<p>You can either install the Quartus II software locally or run <i>&lt;full-path-to&gt;/jtagserver --install &lt;username&gt; &lt;password&gt;</i> to specify the username and password that Windows should use when running the JTAG server service.</p>

Issue	Workaround
<p>The installation of the USB Blaster is not successful for Quartus II software version 6.1 because a file is missing.</p>	<p>To update the driver:</p> <ol style="list-style-type: none"> <li>1. Attach the USB Blaster to the USB port.</li> <li>2. In the Control Panel, double-click <b>System</b>, and then click the <b>Hardware</b> tab. Click <b>Device Manager</b>.</li> <li>3. Open the Universal Serial Bus controllers and right-click Altera USB-Blaster 32, and click <b>Update Driver</b>.</li> <li>4. In the Hardware Update wizard, select <b>Install from a list or specific location (Advanced)</b> and click <b>Next</b>. (For Windows 2000, you must select <b>Search for a suitable driver for my device</b> and then select <b>Specify a location</b> and click <b>Next</b>.)</li> <li>5. Browse for the new driver location and click <b>Next</b> (or <b>OK</b> for Windows 2000).</li> <li>6. You may be asked to reselect the location of the driver again if there is a previous driver existing in the system. If you are using Windows 2000, you must select <b>Install one of the other drivers</b>, and then select the path to the new driver again. If you are using Windows XP, you can directly select from the list of drivers and select the new driver path.</li> <li>7. Install the driver. If the system still asks for <b>FTD2XX.sys</b>, your selection was incorrect. You should be asked for <b>FTDIBUS.sys</b>.</li> </ol>
<b>Version 6.0</b>	
<p>If you are running the Quartus II software on the Windows XP64 operating system, the software may “hang” when the Text Editor is opened.</p>	<p>You must end the <b>quartus.exe</b> process in the Process tab of the Windows Task Manager, delete all the files in your <b>%TEMP%</b> directory, and restart the Quartus II software.</p>
<p>If you are running the Quartus II software on the Windows XP64 operating system with a USB Software Guard, you may receive a message that there is no license found.</p>	<p>You must install the Sentinel driver for the Software Guard by browsing to the <b>quartus/drivers/sentinel/win_xp64</b> directory when asked for the location of the driver.</p>

Issue	Workaround
<b>Version 5.1 SP2 and earlier</b>	
<p>The introduction of Microsoft Security Update MS05-026 prevents the proper display of Quartus II Help across a network.</p>	<p>To properly display HTML Help files, you must access them from a local PC. If you are unable to access Help files locally, go to Microsoft Knowledge Base Article 896054 (<a href="http://support.microsoft.com/?kbid=896054">support.microsoft.com/?kbid=896054</a>) for more information about possible workarounds.</p>
<p>The keyboard accelerators (underlines) for Alt+ key combinations do not appear in the Quartus II user interface until the Alt key is pressed the first time.</p>	<p>This behavior is a Windows 2000 user-specified preference. To change to the previous behavior, follow these steps:</p> <ol style="list-style-type: none"> <li>1. On the Start menu, click <b>Control Panel</b>.</li> <li>2. Click <b>Display properties</b>.</li> <li>3. Click the <b>Appearance</b> tab.</li> <li>4. Click <b>Effects</b>.</li> <li>5. Turn off <b>Hide underlined letters for keyboard navigation until I press the Alt key</b>.</li> </ol>
<p>If you use Windows 2000 as a software server to serve the Quartus II software to a client computer running Windows XP, running the Quartus II software on the Windows 2000 server at the same time clients are running the Quartus II software, will cause the Quartus II software on the server to crash.</p>	<p>Do not run the Quartus II software on the Windows 2000 server.</p>
<p>You cannot access the web-based PowerPlay Early Power Estimator on the Altera web site if you have installed Windows XP SP2 because the service pack blocks the active content. email tech huat 4.2</p>	<p>Refer to the Altera Knowledge Database on the Altera website for more information on enabling your browser to access the PowerPlay Early Power Estimator spreadsheets.</p>
<p>Some dialog box title bar text is not displayed correctly when the Quartus II software is installed on a computer running the Chinese version of Windows XP.</p>	<p>Change the font in the <b>Active Title Bar</b> section of the <b>Windows Appearance</b> Control Panel.</p>
<p>If you do not have Administrator privileges when you install the Quartus II software, certain features of the software, particularly the online Help, will not work properly, for example:</p> <ul style="list-style-type: none"> <li>• Software guards (parallel and USB)</li> <li>• Programming with JTAG server</li> </ul>	<p>Altera recommends that you have Administrator privileges when installing the Quartus II software.</p>

Issue	Workaround
<p>Under certain circumstances, the Quartus II installation program may crash or you may receive an error message immediately upon launching the installation program.</p>	<p>Reinstall the <b>stdole32.tlb</b> file from the original Windows distribution disks. To reinstall the file, type the appropriate command at a command prompt. (Note: the command must be typed on one line.)</p> <p><b>Windows 2000:</b> &lt;CD-ROM drive letter&gt;:\i386\expand.exe stdole32.tl_ %SystemRoot%\System32\stdole32.tlb &lt;Enter&gt;</p> <p><b>Windows XP:</b> &lt;CD-ROM drive letter&gt;:\i386\expand.exe stdole32.tl_ %SystemRoot%\System32\stdole32.tlb &lt;Enter&gt;</p>
<p>If the full, hierarchical name of an instance exceeds 247 characters, it may not be displayed properly in the Quartus II user interface. This problem occurs most often with EDIF netlist files generated by other EDA synthesis tools.</p>	<p>Limit the full, hierarchical instance name to fewer than 247 characters if possible.</p>
<p>If you are running the Quartus II software from a network server, the Quartus II software will not run properly on the client computer if you share the <b>\quartus\bin</b> directory.</p>	<p>You must share the <b>\quartus</b> directory, not the <b>\quartus\bin</b> directory.</p>
<p>The Quartus II software is not compatible with the MATLAB web server.</p>	<p>Turn off the MATLAB web server in the <b>Services Control Panel</b> on the Start menu before running the Quartus II software.</p>
<p>Under some circumstances, the Quartus II splash screen appears and the Quartus II icon appears in the Taskbar, but the graphical user interface does not appear. Under other circumstances, the user interface appears but windows and/or toolbars do not appear correctly.</p>	<p>The registry settings controlling the position of the Quartus II windows may have become corrupted. If the user interface appears, click the <b>Reset All</b> button on the <b>Toolbars</b> page of the <b>Customize</b> dialog box, or, if the user interface does not appear, type the following command at a command prompt: quartus -reset_desktop &lt;Enter&gt;</p>

Issue	Workaround
<p>If you install the stand-alone Quartus II Programmer and the Quartus II software, and then uninstall either one, the Programmer may report "JTAG Server -- internal error code 82 occurred" when you click the <b>Add Hardware</b> button in the <b>Hardware Setup</b> dialog box on the Edit menu. This error occurs because uninstalling the software has disabled the JTAG Server service.</p>	<p>Manually restart the JTAG Server service by locating the <b>jtagserver.exe</b> program and at a command prompt for that directory, type <code>jtagserver --install &lt;Enter&gt;</code></p>
<p>If you choose to uninstall a previous version of the Quartus II software during installation, and there is a "locked" file or directory, the installation program will not reboot the computer as is necessary to successfully complete the installation.</p>	<p>Exit from the installer and reboot the computer manually after the removal of the previous version is complete, before completing the installation of the new version.</p>
<p>During installation of the Quartus II software, when you insert the ModelSim-Altera CD-ROM, a Windows Explorer window may appear. S</p>	<p>Close the Windows Explorer window before proceeding with the installation.</p>

**Solaris & Linux**

Issue	Workaround
<p><b>Version 6.1</b></p>	
<p>Using the Cut, Copy, and Paste features in the TimeQuest SDC File Editor may cause the software to hang, close unexpectedly, or both.</p>	<p>Instead of using these features in the TimeQuest SDC File Editor, use an external text editor if these features are necessary.</p>
<p>Under some circumstances, your web browser software may fail to launch correctly from the IP MegaStore MegaWizard Plug-In Manager. The web browser defined in the MegaWizard Plug-In Manager for the IP MegaStore inherits the environment settings from the Quartus II software. Specifically, the LD_LIBRARY_PATH environment variable may contain entries that conflict with web browsers such as FireFox, preventing them from starting correctly.</p>	<p>Edit the script that launches the web browser to make sure the Quartus II directories are the last entries in the LD_LIBRARY_PATH variable.</p>

Issue	Workaround
<b>Version 6.0</b>	
<p>When using the TimeQuest Timing Analyzer Graphical User Interface, occasionally when sourcing a script or generating several report panels in rapid succession (for example, the “Macros” in the Task pane), the user interface may not display any report data at all, or the report data may be old or incomplete. On Linux, the GUI may crash completely. This is due to UNIX file systems not synchronizing between when the user interface reads the report file while the report panels are being generated. The problem is worse with large reports and on slow file systems (for example across a slow network).</p>	<p>Generate only one individual report panel at a time manually from the GUI. This gives the TimeQuest analyzer a chance to finish generating the report panel before the GUI reads and displays it.</p>
<p>Performing any operation on a flash memory connected to a MAX II device used in a Parallel Flash Loader configuration scheme may cause the Quartus II software to crash with an internal error.</p>	<p>Use a Windows-based computer to configure devices used in a Parallel Flash Loader configuration scheme.</p>
<p>While any shortcut menu is open from an undocked dockable window, if you right-click in the title bar, then all activity in the title bar (left-click and drag, right click context menu, 'X' close button) stops working.</p>	<p>Display a shortcut menu again and perform any action except right-clicking in the title bar to restore normal operation.</p>
<b>Version 5.1 SP2 and earlier</b>	
<p>If the operating system crashes, and the file system in \$TMP is rebuilt automatically, the data in the \$TMP/Mw_&lt;user ID&gt; file is corrupted, the Quartus II software may fail to start correctly.</p>	<p>Delete the \$TMP/Mw_&lt;user ID&gt; file and restart the Quartus II software.</p>
<p>If you are using the Exceed X server software for Windows while running the Quartus II software, the font size may be larger than the line height. This problem occurs most often if you installed the Exceed software while running at a screen resolution greater than 1024 × 768.</p>	<p>Reinstall the Exceed software while running at a screen resolution of 1024 × 768. You can then switch back to your normal, higher resolution setting.</p>
<p>Under some circumstances, there may be editor windows listed on the Window menu that you cannot see.</p>	<p>To display the hidden windows, click <b>Cascade</b> on the Window menu.</p>

Issue	Workaround
You cannot launch the AXD Debugger software from within the Quartus II software.	Launch the AXD Debugger software from outside the Quartus II software.
Under some circumstances, the Internet connectivity features of the Quartus II software are not functional.	Specify the full path to your web browser software on the <b>Internet Connectivity</b> page of the <b>Options</b> dialog box. If you access the Internet through a proxy server, you must also specify the address of the proxy server and its port number.
Under some circumstances you cannot access the Quartus II online Help in the user interface.	To access Help, type <code>hh quartus.chm</code> <Return> at a command prompt.
If you are accessing the Quartus II software through one of the following versions of the Hummingbird Exceed software (6.2, 7.0, 7.1, or 8.0) and have any Microsoft Office application or Internet Explorer open, the Quartus II user interface may start very slowly.	Contact Hummingbird Software at <b>www.hummingbird.com</b> for a patch for the Exceed software.
The stand-alone Quartus II Programmer and SignalTap <sup>®</sup> II programs are not available on Solaris and Linux workstations.	

**Linux Only**

Issue	Workaround
<b>Version 7.1</b>	
On the SUSE Linux platform, the Quartus II software opens in the lower right side of the screen, even after you re-position it.	Set the environment variable <code>QUARTUS_MWWM</code> to the value <code>allwm</code> .
<b>Version 7.0</b>	
When you are running the Quartus II software on Red Hat Enterprise Linux 4.0 and using the GNOME desktop, you may receive an internal error when you create a LogicLock region, and then use the <b>Add Path</b> dialog box to add a node for the source name with the Node Finder, and then click <b>Cancel</b> in the <b>Add Path</b> dialog box.	Do not click <b>Cancel</b> in the <b>Add Path</b> dialog box after you add a node for the source name with the Node Finder.

Issue	Workaround
<b>Version 6.0</b>	
The Quartus II software may crash with a core dump if you close the Quartus II software while a properties dialog box is open from any link in Help.	Do not open the properties dialog box on any link in Help.
When you are running the Quartus II software on Red Hat Enterprise Linux 4.0 and using the KDE 3.3 desktop, the Quartus II software may 'hang' when a graphical tool such as the Chip Editor or Pin Planner displays a tooltip when you select an element to edit.	Set the environment variable <code>cui_disable_tooltips = 1</code> to disable tooltips.
Your programming hardware is not shown in the <b>Add Hardware</b> dialog box when running under Red Hat Enterprise Linux 64.	Only the EthernetBlaster is supported for programming on 64-bit platforms.
<b>Version 5.1 SP2 and earlier</b>	
If you run a remote Linux desktop session in a Windows client such as Exceed, depending on your configuration, the SignalTap II Logic Analyzer may be unstable and could crash with a segmentation fault.	Use an Xterm window to access the Quartus II software instead of a remote desktop session.
If the MasterBlaster download cable is not listed in the <b>Available hardware items</b> list in the <b>Hardware Settings</b> tab of the <b>Hardware Setup</b> dialog box, but it is connected properly, you may not have read/write permission for the serial ( <code>dev/ttySx</code> ) port to which the MasterBlaster cable is connected.	Have a system administrator assign read/write permission for the appropriate port. This change can be accomplished by adding you to the "uucp" group, or by giving read/write permission for the serial port to everyone, using the following command: <code>chmod o+rw /dev/ttySx</code> where <i>x</i> is the serial port affected.
If you are using the ReflectionX X-server software as your display on a Linux workstation, the Quartus II software may hang and a white box may appear.	Set the <code>QUARTUS_MWWM</code> environment variable to <code>allwm</code> and then start the Quartus II software without the splash screen by typing the following commands at a command prompt: <code>setenv QUARTUS_MWWM allwm &lt;Return&gt;</code> <code>quartus -no_splash &lt;Return&gt;</code>

Issue	Workaround
Under certain circumstances, the Quartus II software may not start properly.	On a system with a static IP address, ensure that the <b>/etc/hosts</b> file has an entry for the host name of the machine on which you are running. For example, if the workstation is named “orange,” there should be an entry in <b>/etc/hosts</b> with the IP address of the “orange” workstation as shown below: <pre>&lt;IP address of orange&gt; orange</pre> In addition, the network configuration (hostname, DHCP host name, DNS search path, and domain names) must be correct or the Quartus II software will abort on startup.
If you are running the Quartus II software version 4.0 and later using VNC software, the Quartus II software may terminate unexpectedly whenever you open any file or browse any directory from within the Quartus II software.	Make sure your VNC server software is version 3.3.4 or later.
If you are running the Quartus II software under Red Hat Linux 8.0, you may experience substantial degradation of compilation times if your design files are located on a separate server from the Quartus II software.	Make sure that the operating system kernel is upgraded to the latest available. If you are using a NetApps server, refer to the following document for more information: <a href="http://www.netapp.com/tech_library/ftp/3183.pdf">www.netapp.com/tech_library/ftp/3183.pdf</a>

## Device Family Issues

### Cyclone, Stratix & Stratix GX

Issue	Workaround
<b>Version 6.0</b>	
The method used to report power for clock networks is different between the Quartus II PowerPlay Power Analyzer and the PowerPlay Early Power Estimator (EPE). The Quartus II PowerPlay analyzer reports the power for the resource (pin or PLL) that drives the network, while the EPE reports the power in the Clock Network section of the spreadsheet.	No action is necessary.

Issue	Workaround
<b>Version 5.1 SP2 and earlier</b>	
<p>When you use a Routing Constraints File (.rcf) to control fitting after performing Routing Back-Annotation, your timing analysis results may change slightly due to parasitic and other effects. Any change will be very small.</p>	

**Cyclone III and Stratix III**

Issue	Workaround
<b>Version 7.1 SP1</b>	
<p>There is an issue with designs that target Stratix III and Cyclone III devices and that use the altpll_reconfig megafunction to reconfigure a PLL that has its output counters rotated (for example, the Quartus II Fitter modifies PLL clk[0] output to use counter C2 instead of C0 to improve clock routability). In these cases, any reconfiguration changes to the output counters yield incorrect results. This issue does not affect PLL phase reconfiguration, which is through a different interface and does not use the altpll_reconfig megafunction.</p>	<p>Prevent the Quartus II software from rotating PLL output counters by applying the following instance assignment to any affected PLLs:</p> <pre style="margin-left: 40px;">set_instance_assignment -name PRESERVE_PLL_COUNTER_ORDER ON -to &lt;PLL_node_name&gt;</pre> <p>Note that this workaround also prevents the Quartus II software from trying to improve clock routability and may result in fitting problems.</p> <p>Once you migrate to a later version of the Quartus II software that resolves this issue, you must remove the workaround assignment so that it does not negatively affect your design.</p>
<b>Version 7.1</b>	
<p>The altpll and altlvds megafunction instantiations have PLL clock names that change whenever any parameters are modified, and possibly between different releases of the Quartus II software. As a result, any timing constraints (or other assignments) made to the PLL clock names may become invalidated when the PLL name changes. The Quartus II software reports these constraints as ignored constraints.</p>	<p>In the Quartus II software version 7.1 and earlier, ensure that any timing constraints or other assignments made to PLL clocks are also modified after making any changes to altpll or altlvds megafunction instantiations. In addition, also ensure timing constraints and other assignments are migrated correctly between different versions of the Quartus II software.</p>

Issue	Workaround
<p>Location and other assignments made to the altpll megafunction name and intended only for the PLL WYSIWYG are also applied to logic cells created by the altpll megafunction. As a result, you may see errors indicating PLL assignments do not apply to logic cell nodes.</p>	<p>Make assignments intended only for the PLL on the PLL WYSIWYG name only and not on the higher-level altpll hierarchy name.</p>
<p>If you make <b>Fast Output Register</b> and <b>Fast Output Enable Register</b> assignments to I/O pads with differential I/O standards, it can in some cases cause a no fit.</p>	<p>Make the <b>Fast Output Register</b> or <b>Fast Output Enable Register</b> assignment to the registered node driving the differential I/O pad, instead of making the assignment to the I/O pad.</p>
<p>While compiling a PLL design in AHDL that targets Cyclone III or Stratix III devices, uses a scanc1kena port, and has the PLL reconfiguration option enabled, the Quartus II software produces the following error:</p> <pre>Error: Symbolic name "scanc1kena" must be port of megafunction, macrofunction, primitive, or state machine "altpll_component"</pre>	<p>Use VHDL or Verilog instead of AHDL.</p>

**Stratix and Stratix GX**

Issue	Workaround
<p><b>Version 6.0</b></p>	
<p>The Quartus II PowerPlay Power Analyzer reports PLL, XGMII state machine, GXB transceiver, and I/O pin power as contributors to the power reported for High Speed Transceiver blocks. However, the PowerPlay Early Power Estimator (EPE) spreadsheet reports this power in a “High Speed Transceiver Blocks” section as well as an entry in the “Clock Networks” section. Similarly, the PLL, SERDES blocks, and I/O pins of an LVDS block are reported in the PowerPlay Power Analyzer, and as entries in the Clock Networks and HSDI sections of the EPE spreadsheet.</p>	

Issue	Workaround
<b>Version 5.1 SP2 and earlier</b>	
<p>If you use the altddio_bidir or alt_dqs megafunction and connect any data port directly to VCC or GND, the Quartus II software version 3.0 SP1 and later will insert an additional logic element in the circuit path.</p>	

**Stratix II GX, Arria GX, and HardCopy II**

Issue	Workaround
<b>Version 7.1</b>	
<p>When using Nativelink to perform an RTL simulation of a VHDL design that instantiates an altmemphy megafunction and targets either Stratix II GX, Arria GX, or Hardcopy II device, compilation of the design in the simulator fails as the device-specific simulation libraries needed by the design are compiled after the design files in the auto-generated simulation script.</p>	<p>Edit the <b>simulation/modelsim/&lt;project name&gt;_run_msim_rtl_vhdl.do</b> file and move the following lines:</p> <pre>vlib vhdl_libs/stratixii vmap stratixii vhdl_libs/stratixii vcom -work stratixii {&lt;QUARTUS_ROOTDIR&gt;/eda/sim_lib/stratixii_atoms.vhd} vcom -work stratixii {&lt;QUARTUS_ROOTDIR&gt;/eda/sim_lib/stratixii_components.vhd}</pre> <p>After the lines that compile the libraries of your selected device:</p> <pre>vlib vhdl_libs/&lt;device_family&gt; vmap stratixiigx vhdl_libs/&lt;device_family&gt; vcom -93 -work stratixiigx {&lt;QUARTUS_ROOTDIR&gt;/eda/sim_lib/&lt;device_family&gt;_atoms.vhd} vcom -93 -work stratixiigx {&lt;QUARTUS_ROOTDIR&gt;/eda/sim_lib/&lt;device_family&gt;_components.vhd}</pre> <p>Where &lt;device_family&gt; is either stratixiigx, arriagx, or hardcopyii.</p>

**Stratix**

Issue	Workaround
Designs compiled for Stratix EP1S40ES devices must be recompiled for the EP1S40 device before programming.	
Stratix PLL simulation models have been enhanced to handle jitter on the input clock. This enhancement has the unintended side effect that functional simulations for LVDS designs using cascaded PLLs may be incorrect by one clock cycle.	Altera recommends that you perform Timing Simulation to display the correct behavior in the Quartus II Simulator or in other EDA Simulators.

**Stratix II**

Issue	Workaround
<b>Version 7.1</b>	
Designs with the <code>altmemphy</code> megafunction that target Stratix II devices may not meet timing on the <code>resynchronization</code> and <code>postamble</code> paths in a default compilation.	Place the registers manually on the <code>resynchronization</code> and <code>postamble</code> paths close to the I/O pins. Some designs may require additional modification. Contact Altera Technical Support at <a href="http://www.altera.com/mysupport">www.altera.com/mysupport</a> and click “Create New Service Request.”
<b>Version 6.0 and earlier</b>	
An intermittent read failure has been detected on Stratix II M4K RAMs due to a software configuration error for designs compiled with Quartus II software version 5.0 SP1 and earlier.	This issue has been resolved in the Quartus II software 5.0 Service Pack 2 and Quartus II software version 5.1. To learn more about this issue, refer to the Stratix II Errata on the Altera website.
Due to changes in the <code>altlvds_tx</code> and <code>altlvds_rx</code> megafunctions in the Quartus II software version 5.0, user-created timing assignments to the megafunctions are changed. The megafunctions now make most timing assignments automatically.	Check your assignments to make sure that the Quartus II software implemented them correctly.
The Quartus II software version 5.0 does not support programming file generation for some Stratix II devices when M-RAM blocks are used in some memory modes, and if the <code>STRATIXII_MRAM_COMPATIBILITY</code> option is turned off.	For more information about programming file support for Stratix II devices, refer to the <i>Stratix II FPGA Family Errata Sheet</i> , which is available on the Altera website.

Issue	Workaround
The Quartus II software version 4.2 and later supports programming file generation for EP2S60 ES devices, but only for designs where the M-RAM memory is not used.	For more information about programming file support for Stratix II devices, refer to the <i>Stratix II FPGA Family Errata Sheet</i> , which is available on the Altera website.
Back-annotating some designs targeted to a Stratix II device with the <b>Demote cell assignments to</b> option set to <b>LABs</b> may prevent the design from fitting.	Back-annotate the design with <b>Demote cell assignments to</b> turned off.

**Stratix GX**

Issue	Workaround
<b>Version 6.0</b>	
Timing simulation performed in the Quartus II software on designs that use the altgxb megafunction in Stratix GX devices is not accurate on the rx_clkout and rx_out outputs. The simulation is functionally correct, but the relative timing delays between the signals are not accurate.	Perform your timing simulation in another tool such as ModelSim.

**Stratix II GX**

Issue	Workaround
<b>Version 6.0</b>	
The latency of alt2gxb megafunction simulations on Stratix II GX is not accurate in comparison to the device. This is due to approximation used in the Quartus II simulation in modeling the analog portion of the hardware. The latency on the digital portion is within the range of a few clock cycles of the device. The latency is an exact match with the hardware when input vectors are carefully made and do not contain any race conditions.	The Stratix II GX handbook has specified latency range information. The latency information from Quartus II simulations is a good approximation.

Issue	Workaround
<p>You may receive an error message saying "The Quartus II software could not combine the following GXB REFCLK divider(s)..." when performing incremental compilation on a Stratix II GX design. These error messages result from two causes:</p> <ol style="list-style-type: none"> <li>1. You are trying to combine multiple alt2gxb megafunctions and they are not in the same partition.</li> <li>2. You are using multiple alt2gxb megafunctions that use a calibration block, and are not in the same partition.</li> </ol>	<ol style="list-style-type: none"> <li>1. Place all alt2gxb megafunctions in the same partition.</li> <li>2. There is only one calibration block in the device. You should enable the calibration block for one instance of the alt2gxb megafunction only, and disable the calibration block for the other instances.</li> </ol>

**Arria GX**

Issue	Workaround
<b>Version 7.1</b>	
<p>The altmult_accum MegaWizard Plug-In Manager incorrectly disables the accum_sload port and rounding/saturation for Arria GX.</p>	<p>Target either Stratix II or Stratix II GX devices in the altmult_accum MegaWizard to get the full feature set.</p>

**Stratix III**

Issue	Workaround
<b>Version 7.1</b>	
<p>When using an altmemphy QDRII Stratix III-generated variation, the functionality of the byte enable signal is correct only for 9-bit-wide QDRII memories.</p>	<p>To simulate correctly, disconnect the connection of the byte enable signals between the variation and the memory mode, and tie the byte enable input to the memory model low.</p>
<p>The Design Assistant may report excessively conservative Clock Rule Warnings for some MegaCore designs that target Stratix III devices.</p>	

Issue	Workaround
When compiling an altmemphy QDR II Stratix III—generated variation where you have enabled the <b>Dynamic Parallel On-Chip Termination</b> option in the altmemphy MegaWizard Plug-In Manager, you get an Internal Error in the Quartus II software.	Disable the <b>Dynamic Parallel On-Chip Termination</b> option in the altmemphy MegaWizard Plug-In Manager, and regenerate the variation before re-compiling in Quartus II software.
The default value for the core voltage for Stratix III -4L devices has changed from 1.1V to 0.9V.	If you want to change the core voltage to 1.1V, select <b>1.1V</b> in the <b>Core supply voltage</b> list in the <b>Voltage</b> page under <b>Operating Settings and Conditions</b> in the <b>Settings</b> dialog box.
If a design that targets Stratix III devices uses LVDS RX in an I/O row, half-rate DDR on the TX pins of the same I/O row cannot be used. As a result, DQ pins of a DDR memory interface cannot be used together with LVDS RX in any Horizontal I/O row.	
Help does not include information about the fbmimic bidir port, which is available for the altpll megafunction. If the design targets a Stratix III device and if you are using ZERO_DELAY_BUFFER setting on the OPERATION_MODE parameter, you can set the USING_FBMIMICbIDIR_PORT parameter to ON.	

Issue	Workaround
<p>When generating the altmemphy QDRII design for a Stratix III device, the address and command default parameters are set incorrectly, which causes incorrect simulation behavior.</p>	<p>After generating the altmemphy QDRII design, set the following values inside the top level file <code>&lt;VARIATION_NAME&gt;.v/vhd</code>, when instantiating the altmemphy megafunction.</p> <p>For VHDL:</p> <pre>VARIATION_NAME_alt_mem_phy_sii_inst : VARIATION_NAME_alt_mem_phy_sii  GENERIC MAP (      ADDR_CMD_2T_EN =&gt; 0,      ADDR_CMD_ADD_1T =&gt; "TRUE",</pre> <p>For Verilog:</p> <pre>defparam  VARIATION_NAME_alt_mem_phy_sii_inst.ADDR_CMD_2T_EN = 0,  VARIATION_NAME_alt_mem_phy_sii_inst.ADDR_CMD_ADD_1T = "TRUE",</pre> <p>A side effect of carrying out this simulation workaround is that the TimeQuest Timing Analyzer reports an error in the Synopsys Design Constraints File (<code>.sdc</code>) when you compile it in the Quartus II software.</p>
<p>The altmemphy <code>reset_request_n</code> output is undriven for Stratix III VHDL variations only. This issue affects only implementations where this signal is needed to derive additional resets.</p>	<p>Generate your altmemphy variation in Verilog HDL.</p>

Issue	Workaround
<p>When you use an altmemphy QDR II Stratix III variation generated in VHDL, the design fails to calibrate in simulation. Calibration fails because data is never written to the memory because the data masking mechanism is incorrect due to wrong polarity of the byte enables during calibration.</p>	<p>In the file <code>&lt;VARIATION_NAME&gt;_alt_mem_phy_siii.vhd</code>, replace the following text:</p> <pre>seq_be &lt;= not seq_be_n;</pre> <p>with this text:</p> <pre>seq_be &lt;= seq_be_n;</pre>
<p><b>Version 6.1</b></p>	
<p>Stratix III designs with PLLs originally generated for Stratix II give errors during the Quartus II functional simulation netlist generation step.</p>	<p>Regenerate the PLL for the Stratix III design.</p>
<p>The assignments generated for the altmemphy megafunction, in the <code>&lt;variation_name&gt;_pin_assignments.tcl</code> file, assume that the top-level pin names match the pins on the altmemphy variation. Using different names for your top level pins, including using single bit signals instead of one-bit busses, will result in incorrect behavior.</p>	<p>Use the Assignment Editor to change the assignments to match the top-level pin names in your design.</p>

**Cyclone**

Issue	Workaround
<p>Altera recommends that the frequency of the external clock output of the PLLs be limited to 312 MHz.</p>	
<p>The operating frequency range of the Cyclone PLL has been changed. In the Quartus II software version 3.0 and earlier, the range was 300 MHz to 800 MHz. In version 3.0 Service Pack 1 and later, that range changed to 500 MHz to 1000 MHz because of concerns about jitter at frequencies below 500 MHz. Because of this change, the minimum input frequency is now 15.625 MHz (previously 15 MHz) and the minimum output frequency is also 15.625 MHz (previously 9.38 MHz).</p>	<p>Recompile your design after installing the current version of the Quartus II software.</p>

Issue	Workaround
The PLL lock circuit does not function correctly for PFD (Phase Frequency Detector) frequencies below 200 MHz when the temperature is below -20°C.	If operation at temperatures below -20°C is required, choose a higher input frequency and clock division (N) factor such that the PFD input frequency is higher than 200 MHz.

### Cyclone II

Issue	Workaround
<b>Version 5.1 SP2 and earlier</b>	
A write error has been detected on Cyclone II M4K RAMs when using dual ports and dual clocks for designs compiled with Quartus II software version 5.0 SP1 and earlier.	A software workaround is available to address this issue in the Quartus II software version 5.0 SP2 and Quartus II software version 5.1. To learn more, refer to the Cyclone II Errata on the Altera website
If your design uses dual-port, dual-clock memory with a Memory Initialization File (.mif) and you have set the CYCLONE_SAFE_WRITE parameter in the altsyncram megafunction to RESTRUCTURE, any changes to the Memory Initialization File contents will be ignored if you have Smart Compilation turned on.	
Back-annotating some designs targeted to a Cyclone II device with the <b>Demote cell assignments to</b> option set to <b>LABs</b> may prevent the design from fitting.	Back-annotate the design with <b>Demote cell assignments to</b> turned off.

### Cyclone III

Issue	Workaround
<b>Version 7.1</b>	
If you create a new project, select an EP3C25 device for the Cyclone III device family, then set the configuration mode to Fast Passive Parallel in the <b>Configuration</b> tab of the <b>Device and Pin Options</b> dialog box, compilation fails because the auto EPROM selection picks an EPC4 device for the Cyclone III device family.	Select a different configuration mode, or if you want to use Fast Passive Parallel, turn off the <b>Use configuration device</b> option in the <b>Configuration</b> tab.

Issue	Workaround
<p>If you instantiate an <code>altserial_flash_loader</code> megafunction for a Cyclone III device and try to compile it, the Quartus II software fails in the Fitter.</p>	<p>In the <b>Dual-Purpose Pins</b> tab in the <b>Device and Pin Options</b> dialog box, set the pins as <b>Use as regular I/O</b>.</p>
<p>When configuring Cyclone II devices through JTAG, two products may exhibit incorrect behavior: In-System Sources and Probes and the SignalTap II power-up triggering feature.</p> <p>For In-System Sources and Probes, the initial value of a few source ports may be stuck at a low level when they are specified to be high after the JTAG configuration.</p> <p>For the SignalTap II power-up triggering feature, certain trigger condition configuration data may be stuck at an incorrect value after the JTAG configuration. Consequently, it may affect how the SignalTap II Logic Analyzer arms the acquisition.</p>	<p>Configure the device without using the JTAG mode, such as using the Passive Serial mode.</p>
<p>For Cyclone III devices, the Quartus II software may give an internal error if fan-outs are generated to I/O cells that have a location index of 4 or greater.</p>	<p>Fan-out lines may not be generated to these I/O cells.</p>

**HardCopy II**

Issue	Workaround
<p><b>Version 6.0</b></p>	
<p>A HardCopy II design that contains latches with preset or clear signals and a constant (VCC or GND) data, may cause the HardCopy II Revision Compare tool to report a difference in the timing constraints because of a difference in which signal is considered the enable for the latch.</p>	<p>No workaround is necessary, and you can safely ignore the warning.</p>

Issue	Workaround
When migrating a design from Stratix II to HardCopy II, the Revision Compare tool can report differences between the two revisions because of different packing of fast I/O registers because additional packing can be performed on HardCopy II devices that cannot be performed on Stratix II devices.	Either accept the additional packing, and ignore the reported differences or disable Fast I/O assignments on the nodes reported by the Revision Compare tool.
Under certain circumstances, the HardCopy II Companion Revision Comparison tool may report a mismatch in Memory Initialization Files (.mif) between the Stratix II and HardCopy II revisions.	Manually compare the Memory Initialization Files to determine if they are functionally equivalent.
Under certain circumstances, you may receive the following error message when migrating your Stratix II design that contains RAM blocks to HardCopy II: "Error: Source file <file> in directory <dir> was compiled at <time> and saved at <time>. The problem reported for the file is: Only in HardCopy II (<design>)."	Turn off the <b>Auto RAM Block Balancing</b> option for your Stratix II design and recompile the design. Then proceed with the migration process.
<b>Version 5.1 SP2 and earlier</b>	
The HardCopy II Companion Revision Comparison tool can be too strict and produce false positives. That is, it flags certain netlist block differences as functionality differences when they do not actually produce different behavior in silicon. The following example illustrates this behavior: <ul style="list-style-type: none"> <li>The Companion Revision Comparison tool considers a global assignment of &lt;NONE&gt; to be different from "" (null), and reports a difference.</li> </ul>	In each of these cases, the functionality of the two revisions is the same in silicon, but you must manually verify that the functionality is the same. You can use the block names listed in the Companion Revision Report to locate to the Resource Property Editor to verify the functionality
PCI core designs compiled with versions of the PCI Compiler earlier than 4.0.0 will cause numerous spurious differences to be reported in the Companion Revision Compare section of the Compilation Report, even though the source files are correct.	Recompile the PCI core with the PCI Compiler version 4.0.0 or later.

Issue	Workaround
You may receive Revision Comparison warnings about differing EDA tool settings if your project directory contains a Quartus II Defaults File (.qdf).	Delete the Quartus II Defaults File from your project directory.

**MAX II**

Issue	Workaround
<b>Version 7.1</b>	
The program_done bit is not being programmed when a Serial Vector Format File (.svf) is used to program for EPM1270, EPM1270G, and EPM2210G devices.	The Serial Vector Format File can be modified to fix the issue. Contact Altera Technical Support at <a href="http://www.altera.com/mysupport">www.altera.com/mysupport</a> and click “Create New Service Request.”

**EPC2 Configuration Devices**

Issue	Workaround
<b>Version 6.0</b>	
When using the EPC2 configuration device to configure an Altera FPGA using a compressed configuration bit stream, you may encounter a configuration failure due to the CONF_DONE error checking feature. The failure mode occurs when the FPGA releases the CONF_DONE signal outside the acceptable time window. The reason this may occur is because the compression ratio varies depending on the design file. Since the configuration file size varies due to compression there may be insufficient padding at the end of the configuration file. This issue can result in a configuration failure, as indicated by the nSTATUS pin transitioning low near the end of configuration. The error occurs because the CONF_DONE signal is released by the FPGA before the EPC2 device expects it to be released.	For assistance implementing the workaround, contact Altera Technical Support at <a href="http://www.altera.com/mysupport">www.altera.com/mysupport</a> , and click “Create New Service Request”.

## Design Flow Issues

### Verification

Issue	Workaround
<b>Version 6.0 and earlier</b>	
If you are using IP Toolbench to generate simulation models for Altera IP Megacore <sup>®</sup> functions, you will get an error if support for the Stratix device family is not installed.	Install support for the Stratix device family.
If you are using IP Toolbench to generate simulation models for Altera IP Megacore <sup>®</sup> functions, and you do not turn on <b>Generate Simulation Model</b> in the <b>Set Up Simulation Model</b> dialog box during setup, you will get an error when you launch the simulation using ModelSim.	Turn on <b>Generate Simulation Model</b> in the <b>Set Up Simulation Model</b> dialog box and regenerate the Megacore <sup>®</sup> .

### Integrated Synthesis (VHDL and Verilog HDL)

Issue	Workaround
<b>Version 7.1 SP1</b>	
You receive the following unexpected error:  Internal Error: Sub-system: VRFX, File: /quartus/synth/vrfx/verific/ verilog/veriscope_elab.cpp, Line: 261 (VeriNode::ElaborationState()) - >GenerateScope() - >Declare(generated_object)	Your Verilog HDL design has unnamed generate blocks that contain declarations of the same name. To work around the unexpected error, name your generate blocks.
<b>Version 6.0 SP1</b>	
In the Quartus II software version 6.0 and earlier, when an inverted cone of logic drove a bidir pin, the inversion was incorrectly removed.	Recompile your design with the Quartus II software version 6.0 SP1 or later.

Issue	Workaround
<p>In the Quartus II software version 6.0 and earlier, the Quartus II Integrated Synthesis ignored the default value for an incomplete CASE statement if the CASE statement has overlapping conditions in the same CASE item.</p>	<p>Recompile your design with the Quartus II software version 6.0 SP1 or later.</p>
<p><b>Version 6.0 and earlier</b></p>	
<p>When a VHDL or Verilog design specifies a RAM, there are a few cases in which the read-during-write behavior of the RAM will differ between the original design and the hardware implementation and no warning will be given. The following examples illustrate this behavior:</p> <p>The first case occurs when a RAM in a lower-level module directly drives a set of registers in an upper-level module. To work around this problem, move the registers to the lower-level module.</p> <p>The second case occurs when there is combinational logic between a RAM and a set of registers, and the design specifies the write operation of the RAM will occur before the read operation. To work around this problem, remove the logic between the RAM and the registers.</p> <p>The third case is the same as the second case, with the exception that the design specifies the read operation of the RAM will occur before the write operation, and the read address of the RAM is registered. To get around this problem, either remove the logic between the RAM and the registers, or set the <b>Automatic RAM Replacement</b> option to <b>Off</b>.</p>	<p>The workaround for each case is shown immediately following the example.</p>

**Verilog HDL Integrated Synthesis**

Issue	Workaround
A Verilog HDL design that compiles successfully in earlier versions fails in the Quartus II software version 5.1 with the message "Formal port <port_name> must be connected to a structural net expression."	The Verilog language requires that a module instance output port be connected to a net, and not to a reg variable or to a constant. Previous versions of the Quartus II software did not enforce this restriction. Change the variable connected to the module instance output port to a wire datatype.
A Verilog design that compiles successfully in earlier versions fails in the Quartus II software version 5.0 with the message: "Error: Verilog HDL or VHDL error at <filename(line)>: object "<pin_name>" declared in a List of Port Declarations cannot be redeclared within the Module Body"	Remove the declaration in the module body. Ports must be completely specified in the Verilog 2001 list of ports declaration, including where necessary the direction, width, net or variable type, and whether the port is signed or unsigned.

**SOPC Builder Issues**

Issue	Workaround
<b>Version 7.1 SP1</b>	
When the parameter Allow Backpressure is enabled and the FIFO is empty, the HAL API altera_avalon_fifo_read_fifo() exits without waiting for incoming data.	If the parameter Allow Backpressure is enabled, use the macro IORD_ALTERA_AVALON_FIFO_DATA() to read from the FIFO in the user application instead of the HAL API altera_avalone_fifo_read_fifo().
<b>Version 7.1</b>	
Custom components created in versions of SOPC Builder earlier than 7.1 that have data widths that are not multiples of two and greater than 8 bits will not upgrade properly.	Import your custom logic into Component Editor and specify a data width that is at least eight bits wide and a multiple of two (8, 16, 32, 64, etc...) If you increase the width of your component to comply with these limits, the Quartus II software automatically removes any unused bits during synthesis.
When compiling new SOPC Builder designs, the Quartus II software may not locate new components created by the Component Editor in version 7.1.	Add all custom IP components to the Quartus II <b>Global libraries (all projects)</b> in the <b>Libraries</b> page and restart the SOPC Builder.

Issue	Workaround
SOPC Builder may not find new components created by the Component Editor in version 7.1.	Add all custom IP components to the Quartus II <b>Global libraries (all projects)</b> in the <b>Libraries</b> page and restart the SOPC Builder.
SOPC Builder does not find custom IP components that are added to the Quartus II project libraries in the <b>Libraries</b> page of the <b>Settings</b> dialog box in the Quartus II software.	Add custom IP components to <b>Global libraries (all projects)</b> in the <b>Libraries</b> page.
An Avalon-MM master connected through an Avalon-MM pipeline bridge or Avalon-MM clock crossing bridge to Avalon-MM slaves that use native addressing will fail if the bridge is wider than the master.	Do not connect a narrow Avalon-MM master to a wider Avalon-MM bridge if that master accesses an Avalon-MM slave that uses native addressing through the bridge.
For SOPC Builder systems using high performance DDR2 SDRAM, the I/O standard pin assignment script is not run automatically; as a result, bi-directional pins have the wrong I/O standard assigned. Ultimately, the Quartus II Fitter fails.	Run the I/O standard assignment script produced by the altmemphy megafunction manually before running the Quartus II Fitter.
The Component Editor in SOPC Builder does not support Verilog HDL design files (.v) that have multiple modules or VHDL design files (.vhd) with multiple entities.	Use only one module for each Verilog HDL design file and one entity for each VHDL design file.
During system generation, SOPC Builder deletes the HDL source files for tristate slave components.	Have a backup copy of the HDL for these components, and copy it into the project directory after generation.
While importing components with tristate slave interfaces, the Component Editor reverts interface settings to their default values.	After editing the signals and parameters of an interface, double-check all the settings.
If a module dependency loop is reported between the DMA controller and pipeline bridge, the resulting system may still be functional.	The system can be generated by holding down Ctrl and clicking the <b>Generate</b> button.

Issue	Workaround
<p>The generated system for SOPC Builder has reset signals wired incorrectly for Avalon Streaming components that have multiple clock interfaces.</p>	<p>To solve this issue:</p> <ol style="list-style-type: none"> <li>1. Use components with only one clock interface.</li> <li>2. After generation, comment out the line that incorrectly connects the component's reset input to the output of a reset synchronizer.</li> </ol> <p>The line to comment out is within the Avalon ST Sink component's abitrator block, named <code>&lt;component_name&gt;_&lt;interface_name&gt;_arbitrator</code></p> <p>It looks similar to:</p> <pre>assign &lt;sink component name&gt;_&lt;sink interface name&gt;_reset = &lt;source component name&gt;_&lt;source interface name&gt;_reset;</pre>
<p>SOPC Builder fails to launch on Solaris workstations because it refers to the Java Runtime Environment located in the wrong directory.</p>	<p>Contact Altera Technical Support at <a href="http://www.altera.com/mysupport">www.altera.com/mysupport</a> and click "Create New Service Request."</p>
<p><b>Version 7.0</b></p>	
<p>If a one-bit port on a VHDL component is defined as a <code>STD_LOGIC_VECTOR (0 downto 0)</code> the port width will be misinterpreted during SOPC Builder system generation.</p>	<p>Define all single-bit ports as <code>STD_LOGIC</code>.</p>
<p><b>Version 6.1</b></p>	
<p>Compiling an SOPC Builder design generates the following message:</p> <pre>"Warning: Found invalid timing assignments -- see Ignored Timing Assignments report for details."</pre> <p>SOPC Builder erroneously applies an invalid timing assignment as an embedded attribute in the HDL code it generates.</p>	<p>You can ignore these warnings for the SOPC Builder system.</p>

Issue	Workaround
<b>Version 6.0</b>	
<p>The Avalon Interface Specification incorrectly describes the behavior for <code>address</code> and <code>burstcount</code> during burst transfers. The Avalon Interface Specification states: “The start of a write burst is similar to the start of a fundamental master write transfer. The master port asserts <code>address</code>, <code>writedata</code>, <code>write</code>, and <code>byteenable</code> (if present) in addition to <code>burstcount</code>. ... This is the only time that the Avalon switch fabric captures <code>burstcount</code> and <code>address</code>; the master port can deassert them through the remainder of the burst.”</p>	<p>During Avalon master transfers, assert constant values on <code>address</code> and <code>burstcount</code> for the duration of the burst.</p>
<p>If multiple masters control a slave that asserts <code>endofpacket</code>, both masters will see the asserted <code>endofpacket</code>. This may cause problems in systems where masters take action upon <code>endofpacket</code>.</p>	<p>Use <code>endofpacket</code> only in the case that a single master of the asserting slave will take action on the <code>endofpacket</code>.</p>
<b>Version 5.1 SP2 and earlier</b>	
<p>Back-to-back burst transfers from a master to a slave that has a different burst count or bandwidth may fail.</p>	<p>Wait until the slave has finished the read burst before starting a write burst.</p>
<p>Under some circumstances, the automatic addressing feature does not function correctly.</p>	<p>Assign the base address for the component manually.</p>
<p>Under some circumstances, the SOPC Builder does not display correctly on systems in which the graphics card uses hardware acceleration.</p>	<p>Turn off, or reduce the level of hardware acceleration.</p>
<p>In SOPC Builder, Avalon Masters that address more than 32 bits of slave address space do not issue warning.</p>	<p>Redesign your system to avoid giving masters greater than 32 bits of address space.</p>
<p>SOPC Builder fails to open on UNIX when invoked from the <b>MegaWizard Plug-In Manager</b>.</p>	<p>Open SOPC Builder by clicking <b>SOPC Builder</b> on the Quartus II Tools menu.</p>

Issue	Workaround
You may see random display errors, such as streaks and blotches, in the SOPC Builder GUI.	Lower the <b>Hardware Acceleration</b> setting on the <b>Troubleshooting</b> tab of the <b>Advanced Display Settings</b> dialog box in your <b>Display Settings</b> control panel. There is a known incompatibility between the current Java Runtime Environment (JRE) and certain laptop graphics drivers.
When creating a component with the SOPC Builder Component Editor, you must not choose a component name that exactly matches the HDL file name or the top-level module name. If the names are the same, SOPC Builder will generate an error during system generation. This problem will be fixed in a future version of SOPC Builder.	Using the SOPC Builder Component Editor, rename the component to a different name. In the SOPC Builder table of active components, add the newly-named component to your system, and delete the old component.
The SOPC Builder and Nios II Software Development Kit shell may “hang” and become unresponsive if you run either program while the Frisk antivirus software is running.	Turn off the Dynamic Virus Checking feature of the Frisk software before running SOPC Builder or the Nios II SDK shell.

## EDA Integration Issues

Issue	Workaround
<b>Version 7.1</b>	
If your design contains WYSIWYG atoms, and you select another family in the Quartus II project, RTL Simulation using NativeLink results in errors.	If your design contains a clear box netlist generated for a specific device family, and you target a different device family in the Quartus II project, regenerate the clear box netlist for the correct device family. If your design contains IP, check IP documentation to verify whether it supports NativeLink simulation.
<b>Version 6.1</b>	
Active-HDL 7.1SP2 is unable to compile VHDL simulation model file <b>altera_mf.vhd</b> .	Contact Aldec and request the patch with the fix to this issue.

Issue	Workaround
<p>If there are virtual I/O pin assignments at the time of generating board-level timing files in the STAMP format, and if there is any other tool or format selected in any EDA tool category on the <b>EDA Tool Settings</b> page, you may receive an error when you run the EDA Netlist Writer.</p>	<p>If the design has virtual I/O pin assignments, and you want to generate board-level timing files in the STAMP format, then either remove the virtual I/O pin assignments from the Quartus II Settings File (<b>.qsf</b>) and recompile the design, or make sure the following is true before running <code>quartus_eda</code>: All tool and format settings in all categories are set to None with the exception of Board-Level timing analysis tool category. STAMP is selected as the EDA format in the <b>Board-Level Timing Analysis</b> tool category in the <b>Board-Level</b> page under <b>EDA Tool Settings</b>.</p> <p>Or, you can run the following command at a system command prompt:</p> <pre>quartus_eda --format=stamp -- board_timing &lt;project&gt; -c &lt;revision&gt;</pre>
<p><b>Version 6.0</b></p>	
<p>The ModelSim software may fail to simulate a design if <b>Glitch Filtering</b> is turned on in the EDA Simulation Settings page and the <code>+nospecify</code> option is passed to the ModelSim <b>vsim</b> command.</p>	<p>Remove the <code>+nospecify</code> option from the ModelSim <b>vsim</b> command.</p>
<p>If you add or change a component in a Library Mapping File (<b>.lmf</b>), the Quartus II software does not recognize the changes upon the next compilation.</p>	<p>Delete the project database (<b>db</b>) directory and recompile.</p>
<p><b>Version 5.1 SP2 and earlier</b></p>	
<p>FIFO Partitioner instances can only be simulated in 3<sup>rd</sup> party simulators using the original VHDL source files from the <b>quartus/libraries/megafunctions/</b> directory, and NativeLink integration is not supported.</p>	<p>Perform simulation manually as described in the FIFO Partitioner User Guide available from the Literature page of the Altera web site.</p>

Issue	Workaround
The current version of the Quartus II software allows you to select the Synplicity Amplify software as a physical optimization tool. However, this setting is for an automated mode called ATOPS, which is currently not supported by the Amplify software.	Contact Synplicity for the support schedule for the Amplify software ATOPS mode.
NativeLink support does not work with versions of Mentor Graphics Precision RTL Synthesis Software earlier than version 2003b due to a change in the Precision project interface.	

## Simulation Model Changes

### altera\_mf Models

Model	Changes
dcfifo_mixed_widths, dcfifo	<ul style="list-style-type: none"> <li>• Added parameter ADD_USEDW_MSB_BIT to support additional MSB bit for WRUSEDW and RDUSEDW ports.</li> <li>• Added parameter WRITE_ACLR_SYNCH to enforce data integrity when WRREQ is asserted.</li> </ul>
altlvds_rx	<ul style="list-style-type: none"> <li>• Added parameter INCLOCK_PHASE_SHIFT to support new phase shift.</li> <li>• Added data alignment support for flexible LVDS.</li> <li>• Added parameter BUFFER_IMPLEMENTATION to support buffer type as RAM, MUX, or LE.</li> <li>• Added x5, x7 and x9 mode for external PLL mode in flexible LVDS.</li> <li>• Added Soft CDR support for Stratix III LVDS.</li> </ul>
altlvds_tx	<ul style="list-style-type: none"> <li>• Added parameter INCLOCK_PHASE_SHIFT and OUTCLOCK_PHASE_SHIFT to support new phase shift.</li> <li>• Added x5, x7 and x9 mode for external PLL mode in flexible LVDS.</li> <li>• Added parameter USE_NO_PHASE_SHIFT in Cyclone II, Stratix II, and Stratix III flexible LVDS to add additional 90 degrees phase shift.</li> </ul>

<b>Model</b>	<b>Changes</b>
altpll	<ul style="list-style-type: none"> <li>• Added parameter WIDTH_PHASECOUNTERSELECT to control the width of PHASECOUNTERSELECT PORT.</li> <li>• Added parameter USING_FBMIMICBIDIR_PORT with FBMIMICBIDIR PORT.</li> </ul>
altmult_add	<ul style="list-style-type: none"> <li>• Added new 54 x 54 mode for Stratix III devices.</li> <li>• Changed default value for OUTPUT_ACLR from ACLR0 to ACLR3 .</li> <li>• Support extra multiplier latency mode for Stratix III devices.</li> </ul>

### Altera\_primitives

<b>Model</b>	<b>Changes</b>
ALT_BIDIR_BUF DLATCH	<ul style="list-style-type: none"> <li>• Added new primitives DLATCH and ALT_BIDIR_BUF.</li> </ul>

## Latest Known Quartus II Software Issues

For more information about known software issues, look for information in the **Quartus II Software Support** page at the following URL:

<http://www.altera.com/support/software/sof-quartus.html>

## Software Issues Resolved

This section list the numbers of the Customer Service Requests that were fixed or otherwise resolved in this version of the Quartus II software.

Customer Service Request Numbers Resolved in this Release				
10547582	10577885	10580630	10586223	10587497
10588840	10589524	10589609	10590548	10590977
10591001	10591559	10591711	10591815	10591822
10592390	10592422	10592715	10592935	10593134
10593198	10592901	10593286	10594650	10593605
10593817	10593828	10594083	10594341	10594409
10594641	10595049	10595119	10595180	10595623
10595630	10596122	10596629	10596661	10596843
10598327	10599107			

## Revision History

Revision	Description
1.0	Initial Release

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