



Quartus II Software Release Notes

September 2007

Quartus II software version 7.2

This document provides late-breaking information about the following areas of this version of the Altera® Quartus® II software. For information about memory, disk space, and system requirements, refer to the **readme.txt** file in your `\altera\<version number> \quartus` directory. For information about device support in this version of the Quartus II software, along with the latest information about timing and power models, refer to the *Quartus II Device Support Release Notes* on the Altera website at <http://www.altera.com/literature/lit-qts.jsp>.

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New Features & Enhancements

The Quartus II software version 7.2 includes the following new features and enhancements:

- The Quartus II software version 7.2 introduces support for Windows Vista (32-bit and 64-bit). The SOPC Builder tool will support Windows Vista in a future release of the Quartus II software.
- The Quartus II software supports multiprocessors to take advantage of dual and quad core computers.
- The TimeQuest Timing Analyzer now supports clock-as-data analysis.
- The **Report Timing** dialog box in the TimeQuest analyzer now produces a report with a new layout. This layout includes path summaries and details, tabbed information, new path statistics, and a new waveform view.
- You can now create Synopsys Design Constraints Files (.sdc) with the Quartus II Text Editor, and you can specify SDC timing constraints and exceptions.
- The Chip Planner can now display clock regions, and can show potential fan-ins and fan-outs between pins and clock regions.
- You can now make changes to DSP and RAM atoms with the Resource Property Editor.
- You can verify the legality of new and existing pin assignments with the live I/O check feature and view the results in the Live I/O Check Status window. Live I/O check verifies the pin assignments against a subset of the complete I/O assignment analysis rules.
- The State Machine Editor allows you to create graphic representations of state machines for use in your design. Creating state machines using the State Machine Editor allows you to describe complex control logic and state machines used, for example, in DSP processors, without the need for writing lengthy and complex Verilog HDL or VHDL source code. You can, however, generate a Verilog HDL or VHDL design file directly from the State Machine Editor with the **Generate HDL File** command.
- The SignalTap II Logic Analyzer now provides state-based trigger flow control, which allows you to organize trigger conditions into states based on a conditional flow that you define, and provides control of the acquisition buffer.
- Advanced I/O Timing now supports Cyclone III devices, and the Board Trace Model window of the Pin Planner is now available for both Stratix III and Cyclone III device families.
- The new **Insert Avalon-ST Adapters** command inserts an Avalon-ST adapter to connect a data source to a data sink of differing byte sizes in the SOPC Builder system.
- The new EPCS128 configuration device supports Arria GX, Cyclone, Cyclone II, Cyclone III, Stratix II, Stratix II GX, and Stratix III devices.

- Full support for these Arria GX devices: EP1AGX20CF484, EP1AGX20CF780, EP1AGX35CF484, EP1AGX35DF780, EP1AGX50CF484, EP1AGX50DF1152, EP1AGX50DF780, EP1AGX60CF484, EP1AGX60DF780, EP1AGX60EF1152, and EP1AGX90EF1152.
- Full support for these Cyclone III devices: EP3C5E144, EP3C5F256, EP3C5U256, EP3C10E144, EP3C10F256, EP3C10U256, EP3C25U256, EP3C55F484, EP3C55F780, EP3C55U484, EP3C120F484, and EP3C120F780.
- Full support for these Stratix III devices: EP3SL150F780 and EP3SL150F1152.
- Advanced support for these Cyclone III devices: EP3C16U256, EP3C16U484, EP3C40U484, and EP3C80U484.
- Advanced support for these Stratix III devices: EP3SL200F780, EP3SE260H780, and EP3SL340H1152.

EDA Interface Information

The current version of the Quartus II software supports the following EDA tools.

Supported EDA Tools

Synthesis Tools	Version	NativeLink Support
Synplicity Synplify & Synplify Pro	9.0	✓
Mentor Graphics Precision RTL Synthesis	2007a	✓
Mentor Graphics LeonardoSpectrum	2007a	✓
Synopsys Design Compiler FPGA	2005.09	
Synopsys FPGA Compiler II	3.8	✓
Synopsys Design Compiler	2004.12-SP4	
Magma Design Automation PALACE	2.4	✓
Celoxica DK Design Suite	5.0 SP2	
Simulation Tools	Version	NativeLink Support
Mentor Graphics ModelSim	6.1g	✓
Mentor Graphics ModelSim-Altera	6.1g	✓
Cadence NC-Sim (UNIX)	IUS 6.1	✓
Synopsys VCS / VCS MX	Y-2006.06-SP1	✓
Aldec Active-HDL	7.3	✓
Formal Verification Tools (Equivalence Checking)	Version	NativeLink Support
Cadence Encounter Conformal	7.1	
Chip Level Static Timing Analysis	Version	NativeLink Support
Synopsys PrimeTime	Z-2007.06	✓
Board Level Static Timing Analysis	Version	NativeLink Support
Mentor Graphics TAU	3.5.01	
Board Level Symbol/Pin-out Management	Version	NativeLink Support
Mentor Graphics I/O Designer	7.2	

Changes to Software Behavior

This section documents instances in which the behavior and default settings of this release of the Quartus II software have been changed from earlier releases of the software.

Items listed in the following table represent cases in which the behavior of the current release of the Quartus II software is different from a previous version.

Description	Workaround
Version 7.2	
<p>The Generate back-annotation data for time closure option in the Design Entry/Synthesis page under EDA Tool Settings in the Settings dialog box is no longer available.</p>	
<p>Constraining cells or routing causes problems for designs ported from the Quartus II software version 7.1 or 7.1 SP1 to the Quartus II software version 7.2, because location assignments to the following block types are incompatible:</p> <p>IOPAD IOIBUF IOOBUF FF DDIOOUTCELL DDIOOCELL PSEUDODIFFOUT CLKCTRL (if specified as X,Y,N instead of as a user string)</p>	<p>To prevent this incompatibility, remove the location assignments and the routing constraints.</p>
<p>For the alt2gxb megafunction, when adaptive equalization is activated for a specific channel, <code>rx_eqctrl</code> writes to that channel do not have any effect.</p>	
<p>In the Quartus II software version 7.2, there is no support for DQSB pins in Arria GX devices, but some Quartus II version 7.2 designs require DQSB pins.</p>	
<p>Programming file generation for DDR3 circuitry is disabled for designs containing DDR3 circuitry.</p>	

Description	Workaround
The Quartus II software no longer supports Synopsys Formality software.	
The Quartus II software no longer supports the Synopsys PrimeTime VHDL software.	Use the PrimeTime Verilog software to perform timing analysis for your design. To generate the PrimeTime Verilog files, select Verilog in the Format for output netlist list on the Timing Analysis page under EDA Tool Settings .
The TimeQuest Timing Analyzer supports clock-as-data analysis in the Quartus II software version 7.2, while previous versions of the Quartus II software did not. This results in the TimeQuest analyzer reporting new timing paths where the start point (from node) of the path is a clock node (the target of a create_clock or a create_generated_clock command. The Classic Timing Analyzer does not support clock-as-data analysis.	The behavior, which is correct, is documented in “The Quartus II TimeQuest Timing Analyzer” chapter in the <i>Quartus II Handbook</i> . You may need to modify your constraints to compensate for the clock-as-data analysis support if new timing violations are listed for your design, and you believe these violations are overly conservative for your design.
The functionality of the earlier TimeQuest SDC File Editor has been merged into the main Quartus II Text Editor. The Constraints menu from the earlier TimeQuest SDC File Editor is now located in the Quartus II Text Editor on the Edit menu on the Insert Constraints submenu.	
In the SignalTap II Logic Analyzer, power-up triggering is not supported when you enable the state-based trigger flow in the State-based Trigger Flow tab.	
In the SignalTap II Logic Analyzer, setting the Sample depth under Data in the Signal Configuration pane to zero is not supported in the Quartus II software version 7.2. When you compile the project with zero sample depth, you may see errors such as Error (10528): VHDL error at sld_signaltap.vhd(552): value “-1” is outside the target constraint range (0 to 2147483647)	

Description	Workaround
Starting in the Quartus II software version 7.0, when you use OC-12 with 155.52 Mhz inclock, the alt2gxb megafunction generates a design with incorrect data rate. The incorrect data rate is double of what you designed.	Starting in the Quartus II software version 7.2, when you use the SONET OC-12 protocol with the input clock frequency of 155.52 Mhz, refclk divider is generated by the alt2gxb megafunction in order to obtain the correct data rate.
The TimeQuest Timing Analyzer now performs multicorner timing analysis by default during full compilation. This behavior can be changed in the TimeQuest Timing Analyzer page in the Settings dialog box.	
Version 7.1 SP1	
If you instantiated the alt2gxb megafunction for the (OIF) CEI PHY interface protocol, there is an update that exists that will lower jitter.	To reduce jitter, reopen the existing alt2gxb MegaWizard, and in the General tab, select (OIF) CEI PHY Interface in Which protocol will you be using? The CEI tab appears in the MegaWizard. On the CEI tab, turn on Use central clock divider to improve transmitter jitter .
Version 7.1	
If you select a signal to be tapped that cannot be found in the netlist, the Quartus II software will give a critical warning and proceed with compilation. This is a change of behavior from version 6.1 in which compilation would stop with an error message.	To remove the warnings, remove non-existent nodes from the SignalTap II Logic Analyzer. To revert to the behavior of version 6.1 and earlier, you can promote all critical warnings to error messages in the Messages section of the Options dialog box.
The altlvds_tx megafunction shows the actual phase shift of the tx_outclock generated instead of the core clock frequency. This change is only a change in the information that is displayed, and does not change the actual implementation.	

Description	Workaround
<p>PLLs in Stratix II and Cyclone II devices now have a new parameter, <code>sim_gate_lock_device_behavior</code>, that is OFF by default. This new parameter uses a fixed, internal value of 7 to simulate the gate lock feature. If the value is set to ON, you can simulate the actual device behavior for gated lock using the parameter value <code>gate_lock_counter</code>, as you could in earlier versions of the Quartus II software.</p>	
<p>The Quartus II software version 7.1 Power Analyzer enhances the accuracy of the maximum static power estimate for Stratix II and Stratix II GX devices. The maximum static power drawn from the VCCPD power supply for Stratix II and Stratix II GX devices utilizing maximum power characteristics increases in the Power Analyzer power estimate by at most 15mW (depending on the device size.)</p>	

Description	Workaround
<p>The Quartus II software version 7.1 issues the error:</p> <pre>"Error (10621): VHDL Use Clause error at <location>: more than one Use Clause imports a declaration of simple name "<name>" -- none of the declarations are directly visible."</pre> <p>However, the Quartus II software version 7.0 and earlier did not issue the error for the same design.</p> <p>This changed behavior arises when a design imports overloaded subprograms with the same signature from different packages such as <code>STD_LOGIC_UNSIGNED</code> and <code>STD_LOGIC_SIGNED</code>. Both these packages define binary operations on <code>STD_LOGIC_VECTOR</code> arguments. Earlier versions of the software incorrectly favored the first imported declaration.</p>	<p>Remove one of the conflicting Use Clauses. For example, use either <code>STD_LOGIC_SIGNED</code> or <code>STD_LOGIC_UNSIGNED</code>, but not both.</p>

Description	Workaround
<p>The format for Conversion Setup Files (.cof) has changed. The element defined below (in DTD syntax) has been introduced:</p> <pre data-bbox="251 426 797 785"> <!ELEMENT hex_block (hex_filename,hex_addressing, hex_offset)> <!ELEMENT hex_filename (#PCDATA)> <!ELEMENT hex_addressing (#PCDATA)> <!--hex_addressing value is either relative or absolute --> <!ELEMENT hex_offset (#PCDATA)> </pre> <p>In addition the following elements have been deprecated:</p> <pre data-bbox="251 942 760 1155"> <!ELEMENT bottom_boot_block (bottom_boot_filename,bottom_ addressing)> <!ELEMENT main_block (main_filename, main_addressing)> </pre>	
<p>A key change since SOPC Builder version 7.1 is the new file format for storing system design data. Previously, SOPC Builder used a proprietary file format (PTF) to store system designs, while SOPC Builder version 7.1 uses an industry-standard XML file format for data storage. By convention, these files are given the extension .sopc. When you open an SOPC Builder system created in a previous version of the tools, you are asked to upgrade the system to the new format. Click More Information in that dialog box for details on migrating your projects and the changes in SOPC Builder file formats.</p>	

Description	Workaround
Version 6.1	
<p>A minor change has been made to the power breakdown between I/O power and Core power in the PowerPlay Power Analyzer report. The total power dissipated on the device and the total current drawn from each voltage supply are unaffected. I/O routing power refers to the power dissipated by device core routing resources that are driven by input I/O cells. In Quartus II software versions 6.0 and 6.0 SP1, I/O routing power was reported on the PowerPlay Power Analyzer Summary report section as I/O power rather than core dynamic power. For a typical design, the net change is less than 2% of power from I/O Power to Core Dynamic Thermal Power Dissipation in the Summary report section of the PowerPlay Power Analyzer. Also, the Core Dynamic Thermal Power Dissipation by Clock Domain report section did not enumerate the I/O routing power.</p>	
<p>Designs that contain a user-edited Memory Initialization File (.mif) that compile successfully in earlier versions of the Quartus II software may fail with the error "File <filename>.mif contains illegal syntax at line <num>" in the Quartus II 6.1 software. These Memory Initialization Files contain illegal syntax. Illegal Memory Initialization Files were ignored by previous releases of the software.</p>	<p>Correct the syntax of the Memory Initialization File by referring to the Memory Initialization File syntax description in the Quartus II Help, or create a new Memory Initialization File with the Quartus II software.</p>
Version 6.0 SP1	
<p>In the Quartus II software version 6.0 and earlier, when you created a receiver-only instance of the alt2gxb megafunction, a CMU PLL was created that has pll_inclk and pll_locked ports. These ports prevented the combination of two receiver-only implementations at different data rates in the same quad.</p>	<p>In the Quartus II software version 6.0 SP1, a CMU PLL is no longer created when you create a receiver-only instance. You must recreate the megafunction instance with the MegaWizard Plug-In Manager or manually remove the pll_inclk and pll_locked ports from the wrapper file.</p>

Description	Workaround
Version 6.0	
<p>The TimeQuest Timing Analyzer's QSF2SDC conversion utility cannot properly convert all Classic Timing Analyzer timing assignments. The results from the TimeQuest Timing Analyzer may also be different from the Classic Timing Analyzer due to other default behavior differences.</p>	<p>The QSF2SDC conversion utility is considered a guide to help reduce the time to switch to the TimeQuest analyzer, and it is not intended to make the TimeQuest analyzer a plug-in replacement for the Quartus II Classic Timing Analyzer. You should review all converted SDC constraints for correctness and completeness. Refer to the <i>Switching To the TimeQuest Timing Analyzer</i> chapter in the Quartus II Software Handbook for more information.</p>
<p>For designs that target Stratix II GX devices, that use the alt2gxb megafunction in a transmitter-only configuration, the loop_filter_resistor_control value was not correctly written to the megafunction instance.</p>	<p>Use the MegaWizard Plug-In Manager in the Quartus II software version 6.0 to generate a new instance of the alt2gxb megafunction.</p>
<p>If you created a Verilog Quartus Mapping File (.vqm) for a design containing the alt2gxb megafunction in its XAUI configuration with the Quartus II software version 5.1 SP2 or earlier, the setting for Force Signal Detect was incorrectly set to false.</p>	<p>You should regenerate the alt2gxb instantiation in a XAUI configuration using the Quartus II software version 6.0.</p>
<p>Beginning in the 6.0 release, the Quartus II Parallel Flash Loader megafunction (altparallel_flash_loader) erases flash memory blocks before programming them.</p>	<p>No action is required.</p>
<p>Beginning in the 6.0 release, Quartus II integrated synthesis handles bidirectional pins differently. For example if <code>bidir1</code> and <code>bidir2</code> are declared as <code>inouts</code>, the assignment <code>bidir1 <= bidir2</code> creates a directional connection in which data flows from <code>bidir2</code> to <code>bidir1</code>. In the Quartus II software version 5.1 and earlier, a bidirectional connection was created.</p>	<p>If your design requires that data flow in both directions, you must directly connect the bidirectional pins together without using an assignment statement. Assignment statements always produce a unidirectional data flow.</p>

Description	Workaround
The method the Quartus II NativeLink interface uses to locate other EDA tools changed in this release. You might receive a message indicating that the tool cannot be found when you launch it through the NativeLink interface.	You must specify the path to the EDA tool program file on the EDA Tool Options page of the Options dialog box, or with the <code>set_user_command</code> Tcl command.
Version 5.1 SP2 and earlier	
<p>The following primitives now use a new library instead of the altera_mf library:</p> <p>CARRY CARRY_SUM CASCADE CLKLOCK EXP GLOBAL LUT_INPUT LUT_OUTPUT ROW_GLOBAL TRI SOFT OPNDRN DFF DFFE DFFEAS JKFF JKFFE DFFEAS LATCH SRFF SRFFE TFF TFFE ALT_INBUF ALT_IOBUF ALT_OUTBUF ALT_OUTBUF_TRI</p>	To perform functional simulations in Verilog HDL, you must use the altera_primitives.v library located in the <i><Quartus II installation directory>\eda\sim_lib</i> directory. For VHDL, you must use the altera_primitives.vhd library located in the <i><Quartus II installation directory>\eda\sim_lib</i> directory. The VHDL component declaration file is located in the altera_primitives_components.vhd library in the <i><Quartus II installation directory>\eda\sim_lib</i> directory.
In the Quartus II software version 5.0 and later, you can assign the Allow XOR Gate Usage logic option to individual nodes and entities. In previous versions, you could apply this logic option only to the entire design (that is, it was a global logic option).	

Description	Workaround
<p>The following megafunctions have clear box models that contain assignments that are not stored in the Quartus Settings File (.qsf) and are not written out to a Verilog Quartus Mapping File (.vqm):</p> <ul style="list-style-type: none"> altdqs altdq altddio_bidir altddio_out altddio_input altlvds_rx altlvds_tx altufm_i2c dcfifo alt2gxb_reconfig 	<p>Do not save your atom netlist file as a Verilog Quartus Mapping file if you are using these megafunctions.</p>
<p>When you are using formal verification tools with a design that contains LogicLock regions that was compiled with the Quartus II software version 3.0 or earlier, under certain circumstances when you open the design in the Quartus II software version 4.0 and later, the LogicLock regions will not be handled properly.</p>	<p>Redefine the LogicLock regions in the Quartus II software version 4.0 or later to eliminate the errors.</p>

Known Issues & Workarounds

General Quartus II Software Issues

Issue	Workaround
Version 7.2	
<p>When using a PLL in source-synchronous mode to compensate a bus of input signals, the Quartus II software properly sets the I/O delay chain to 0 for all of the bits in the bus. This ensures that there is no skew between the bits in the bus.</p> <p>However, the Quartus II software version 7.1 incorrectly sets the I/O delay chain to 0 for only one of the bits in the bus, instead of all bits in the bus. This setting can result in I/O timing violations and skew between the bits, especially when the source-synchronous mode is not used properly.</p> <p>This issue affects designs using PLLs in source-synchronous mode that target Arria GX, Cyclone II, Cyclone III, HardCopy II, Stratix II, Stratix II GX, and Stratix III devices. This issue also affects designs using altlvds megafunctions that target Cyclone II and Cyclone III devices.</p>	<p>To make sure that the bus is properly compensated, the PLL Compensation assignment must be made to all input pins in the bus. You can make this assignment in the Assignment Editor.</p> <p>If no assignment is made, the Quartus II software selects all of the input pins that drive I/O registers that are clocked by the compensated output of the PLL as the compensation target. In contrast, the Quartus II software version 7.1 selects only one of the input pins as the compensation target.</p>
<p>Live I/O check may produce an error if reserved pin directions are changed while live I/O check is enabled.</p>	<p>Turn live I/O check off and back on again to remove the error.</p>

Issue	Workaround
<p>In the Quartus II software version 7.1 SP1, the Fitter report shows double the designed data rate when the following conditions are met:</p> <ul style="list-style-type: none"> You use PLL reconfiguration (Enable Channel and Transmitter PLL Reconfiguration on the Reconfig tab in the alt2gxb MegaWizard). Inclock frequency is above or equal to 100Mhz. If the data rate is below 3.125 Gbps and the data rate to inclock frequency ratio is 4, 5, 25, or if the data rate is above 3.125 Gbps and the data rate to inclock frequency ratio is 8, 10, or 25. 	<p>Turn on Channel internals and Enable Channel and Transmitter PLL Reconfiguration in the Reconfig tab so that the Reconfig Clks 1 tab appears. Then follow the instructions documented in the alt2gxb MegaWizard Reconfig Clks 1 tab to turn on Use clock [0/1/2/34] reference clock divider. Also refer to the <i>Stratix II GX Handbook</i> for instructions.</p>
<p>If you use the <code>set_operating_conditions</code> command or run a multicorner timing analysis in the TimeQuest Timing Analyzer on a post-map netlist after a full compilation, you may encounter an Internal Error or an unexpected exit.</p>	<p>Use the post-fit netlist after a full compilation, and use the post-map netlist after Analysis & Synthesis.</p>
<p>In the TimeQuest Timing Analyzer, you may ignore assignments created from a PLL output pin to an output port for the Set False Path, Set Max Delay, and Set Min Delay shortcut commands on the Unconstrained Output Port Paths panel, which is generated by clicking Report Unconstrained Paths.</p>	<p>Apply the Set False Path, Set Max Delay, or Set Min Delay commands manually, and use the pin name or the clock name as the source. Optionally, omit the -from name altogether if it is safe to do so.</p>
<p>In the TimeQuest Timing Analyzer, using the <code>derive_pll_clocks</code> command with the <code>-create_base_clocks</code> option erroneously creates a 1 GHz base clock for some GXB input ports.</p>	<p>Manually constrain the base clocks on affected GXB input ports prior to calling <code>derive_pll_clocks</code> with the <code>-create_base_clocks</code> option.</p>
<p>The Quartus II software unexpectedly exits when importing more than one partition containing JTAG logic.</p>	<p>Keep all JTAG logic within one imported partition, or define the logic in the top-level project instead of importing from another project.</p>
<p>The Quartus II software creates extra top-level pins with names ending in <code>_ae</code> when compiling a design with the SignalTap II Logic Analyzer enabled. This issue occurs only when removing pre-synthesis taps in the top-level partition.</p>	<p>Set the Netlist Type for the top-level partition to Source and recompile your design.</p>

Issue	Workaround
<p>Routing constraints are not compatible from the Quartus II software version 7.1 or 7.1 SP1 to version 7.2. The Quartus II software version 7.2 warns "Info: Error on line number <number> in Routing Constraints File".</p>	<p>No action is required, but you can remove the routing constraints to avoid the warning.</p>
<p>The alt2gxb megafunction does not generate reference clock divider for the design if you are using the alt2gxb megafunction with the following specifications:</p> <ul style="list-style-type: none"> • The Quartus II Fitter report in GXB Receiver Summary or GXB Transmitter Summary shows the transceiver is running at double the user specified data rate. This means the design created in previous version of the Quartus II software is missing a ref clock divider. • Protocol is set to Basic. • If the data rate is below 3.125 Gbps and the data rate to inclock frequency ratio is 4, 5, 25, or if the data rate is above 3.125 Gbps and the data rate to inclock frequency ratio is 8, 10, 25. 	<p>A refclk divider is generated by the alt2gxb megafunction starting in the Quartus II software version 7.2 in order to obtain the correct data rate. Rerun the alt2gxb MegaWizard and regenerate the atl2gxb megafunction.</p>
<p>When you compile a project with GXB and LVDS blocks and assigned pins, and click Generate Bottom-up Design Partition Scripts, the bottom-up scripts do not contain pin assignments from the top level.</p>	<p>If you use the Generate Bottom-up Design Partition Scripts command, you must manually copy pin locations for GXB and LVDS blocks into their lower-level scripts.</p>
<p>If your design targets a HardCopy II device and uses incremental compilation and a post-fit netlist, and some single port RAMs were packed together into a single physical dual-port RAM in the original compilation, the Quartus II Fitter may produce an internal error.</p>	<p>If this error occurs, in the Design Partitions window, select Post-Synthesis under Netlist Type for the incremental partition(s) that contain RAMs and are using post-fit netlists.</p>

Issue	Workaround
<p>When a Jam File (.jam) is used to program an EPCS64 or an EPCS128 device, the configuration step might fail with the error message: Error: JTAG ID code specified in JEDEC STAPL Format File does not match any valid JTAG ID codes for device.</p>	<p>You can safely ignore this error and attempt to program the EPCS device.</p>
<p>If your design has a transceiver implementing the CPRI protocol and you turn on Physical Synthesis, you may receive the error message:</p> <p>The Fitter was unable to successfully constrain the routing for Stratix II GX GXB atom implementing the CPRI protocol.</p>	<p>Turn off physical synthesis in the Physical Synthesis Optimizations page under Fitter Settings in the Settings dialog box.</p>

Issue	Workaround
<p>In the Quartus II software version 7.1 SP1, if the alt2gxb design is in double data mode, and the data rate to in-clock frequency ratio is 8 or 10, compiling a design with the alt2gxb MegaWizard creates a ref clock divider in the ref clock.</p>	<p>Regenerate the alt2gxb MegaWizard in the Quartus II software version 7.2, and compile the design to remove the ref clock divider. The compilation reports the same data rate in the report file.</p> <p>To retain the ref clock divider after regenerating the megafunction wrapper, change the value of the following parameter in the megafunction wrapper:</p> <pre>PLL_LEGAL_MULTIPLIER_LIST = DISABLE_4_5_MULT_IN_6G DISABLE_4_5_MULT_ABOVE_3125</pre> <p>If you use <code>DISABLE_4_5_MULT_IN_6G</code>, the alt2gxb megafunction generates a ref clock divider when the data rate to in-clock frequency ratio is 8 or 10 in double data mode GXB designs. This maintains the same behavior as in Quartus II 7.1 SP1.</p> <p>If you use <code>DISABLE_4_5_MULT_ABOVE_3125</code>, this value disables the ref clock divider when the data rate to in-clock frequency ratio is 8 or 10. This is the default behavior in the Quartus II software version 7.2.</p> <p>If you compile the design in the Quartus II software version 7.2 without regenerating the alt2gxb megafunction, the ref clock divider is retained as in the Quartus II software version 7.1 SP1.</p>
<p>Design security support is disabled in the Quartus II software version 7.2.</p>	<p>Contact Altera Technical Support at www.altera.com/mysupport, and click Create New Service Request.</p>
<p>Using Parallel Flash Loader IP optimized for speed adversely affects the CFI device programming time when using the EthernetBlaster download cable.</p>	<p>Use the USB Blaster or ByteBlaster II download cable instead of the EthernetBlaster Download Cable, or use the Parallel Flash Loader IP optimized for area instead of speed.</p>

Issue	Workaround
Version 7.1	
<p>On Windows, the following cores may fail to run when the PERL5LIB environment variable is set:</p> <ul style="list-style-type: none"> • 8B10B Encoder-Decoder • POS-PHY Level 4 • RapidIO • SerialLite II 	<p>Delete the PERL5LIB environment variable:</p> <ol style="list-style-type: none"> 1. Right-click My Computer and click Properties. 2. Click the Advanced tab, and then click Environment Variables. 3. Delete PERL5LIB under both User variables and System variables. 4. Restart the Quartus II software.
<p>During Analysis & Synthesis, the memory transformation power optimization may be controlled by the <code>optimize_power_during_synthesis</code> Quartus II Settings File (.qsf) variable and the parameter <code>low_power_mode</code>. During Place & Route the optimization may be controlled by the <code>optimize_power_during_fitting</code> setting. This setting may be applied globally or on a per-entity basis.</p>	
<p>If you open the Print dialog box or the Page Setup dialog box in the Quartus II software, and if you use an HP Business Inkjet 1200 series printer, the Quartus II software may produce an unexpected error.</p>	<p>If you have this printer, Altera recommends updating to the latest version of the drivers, available for free download from the HP website.</p>
<p>The node names in the RTL Viewer and the Technology Map Viewer do not always match. These node names are internally created nodes. If any assignment on these nodes is necessary, Altera recommends that you use the node name in the Technology Map Viewer rather than the name in the RTL Viewer.</p>	<p>The driver source or fan-out destination or destinations for the node might have a matching name. The source or destination can be found by using the Filter command in the RTL Viewer or the Technology Map Viewer.</p>

Issue	Workaround
<p>In the alt2gxb MegaWizard Plug-In Manager, when you select the Channel interface option under Dynamic Reconfiguration Settings, a new page, Reconfig 2, appears with table with a list of ports you can check to add those ports to the design. Sometimes the wizard turns off a port you just turned on and you are unable to add that port to the design.</p>	<p>Manually add the port to the wrapper in three places: the module declaration section, the port declaration section, and the connection section. In the module declaration, add the port name between the parenthesis module <code>design_name(..., port_name, ...)</code>. In the port declaration section, add the port name and width after the module declaration as <code>input [1:0] port_name;</code> for a bus and <code>input port_name;</code> for a wire. In the connection section, users need to add <code>.port_name(port_name)</code>, after <code>alt2gxb alt2gxb_component</code> (and before <code>// synopsys translate_off</code>). Users also need to remove the line <code>.port_name()</code>, between <code>// synopsys translate_off</code> and <code>// synopsys translate on</code>.</p>
<p>The prev_cmp_<revision name>.qmsg file, which contains messages from the previous compilation for use with the Hide Previous Compilation Messages command, is placed in the project main directory.</p>	<p>You can safely delete the prev_cmp_<revision name>.qmsg file, if you don't need to use the Hide Previous Compilation Messages command in the Messages window. It is not a required file for the project.</p>
<p>Altera recommends that all soft-CDR channels driven by a PLL are within a distance of 25 SERDES rows (including the unbonded SERDES) from that PLL.</p>	
<p>When you launch documentation (PDF and HTML files) from the MegaWizard Plug-In Manager, the MegaWizard uses the Web browser option in the Internet Connectivity page of the Quartus II Options dialog box. The MegaWizard will sometimes use a setting from a previous version of the Quartus II software than the present version. This can lead to errors if the web browser does not exist on your machine.</p>	<p>Manually edit the WEB_BROWSER variable in the quartus2.ini file and remove the reference to the non-existent web browser.</p>

Issue	Workaround
Version 6.1	
When you use the <code>altparallel_flash_loader</code> megafunction in Quartus II software version 6.0 and earlier, the design may not compile successfully.	Regenerate the <code>altparallel_flash_loader</code> megafunction with the current version of the Quartus II software.
If Export version-compatible database in the Compilation Process Settings page is turned on, using the Check & Save All Netlist Changes command causes an Internal Error during the database export phase of the fit.	Turn off Export version-compatible database in the Compilation Process Settings page before using the Check & Save All Netlist Changes command.
You may get one or more messages "Error: Can't generate programming files for project because design file "<name>" is encrypted. It does not have license file support that allows generation of programming files" from the Assembler when compiling a design that is using Altera IP with the OpenCore Plus evaluation feature when your design has VHDL source files that have the construct <code>"use work.all;"</code> .	The errors are reported for IP source files that were added to your project by IP Toolbench, but which are not actually used during compilation. Remove the files listed in the error messages from your project file list and recompile the design.
Running the PowerPlay Power Analyzer directly following an ECO fit results in an Internal Error.	Run the Classic Timing Analyzer (<code>quartus_tan</code>) or the TimeQuest Timing Analyzer (<code>quartus_sta</code>) before you run the PowerPlay Power Analyzer (<code>quartus_pow</code>).

Issue	Workaround
<p>The Quartus II software version 6.1 may run out of memory when Formal Verification is turned on and you are using the Quartus II Integrated Synthesis flow. This happens only when Quartus II Integrated Synthesis extracts finite state machines from the design.</p>	<p>To avoid the out of memory issue in the Quartus II software version 6.1, turn off state machine extraction and rerun synthesis. To turn off state machine extraction, use the following settings in the Quartus II project:</p> <pre>set_global_assignment -name EXTRACT_VERILOG_STATE_MACHINES OFF set_global_assignment -name EXTRACT_VHDL_STATE_MACHINES OFF</pre> <p>You can also use the Quartus II GUI:</p> <ol style="list-style-type: none"> 1. On the Assignments menu, click Settings. 2. Select Analysis & Synthesis Settings, and click More Settings. 3. Turn off Extract Verilog State Machines and Extract VHDL State Machines.
<p>When a design contains IP that is evaluated using the OpenCore Plus hardware evaluation feature, the Quartus II software produces a sequence of Info messages beginning with Info: Elaborated megafunction instantiation "pzdyqx:nabboc".</p>	<p>These messages can be safely ignored.</p>
<p>Version 6.0 SP1</p>	
<p>Running multiple instances of the Quartus II software using the same Quartus Project File (.qpf) may cause unpredictable results or may cause the Quartus II software to crash.</p>	<p>Altera recommends that you not open multiple instances of the Quartus II software using the same project.</p>
<p>Version 6.0</p>	
<p>In the classic Timing Analyzer, when a clock (base or derived) is assigned to an internal register, then data paths to and from the register are not analyzed for clock setup and clock hold analysis.</p>	<p>First, analyze the design with the clock settings assigned to the internal registers. Then remove the clock settings from the internal registers and perform a second analysis, checking only paths to and from those registers. The other resolution is to use the TimeQuest Timing Analyzer instead of the classic Timing Analyzer.</p>

Issue	Workaround
The TimeQuest Timing Analyzer erroneously analyzes paths to the asynchronous data pins of registers (that is, the <code>adata</code> pin) during a recovery/removal analysis.	Apply the <code>set_false_path</code> command from the asynchronous data signal's source port or register to declare these paths as false paths.
If you change the type of a parameter setting in the Quartus II Settings File (<code>.qsf</code>) or a Block Design File (<code>.bdf</code>) and recompile your design, your change appears to have no effect. The type of a parameter is denoted by appending a prefix such as "B" (binary), "D" (decimal). For example, B"10101" represents the binary string "10101", but D"10101" represents the decimal number 10101.	Delete the <code><project>\db</code> directory and recompile the design.
Version 5.1 SP2 and earlier	
Due to a limit of the Windows operating system, path names longer than 229 characters can cause an internal error in the Quartus II software.	Make sure that all path names do not exceed 229 characters. This limitation applies to UNIX and Linux installations also.
If you make a single-point CUT=ON assignment to a node, and then override it with a point-to-point CUT=OFF assignment on a specific path, the OFF assignment will not be honored.	
You may receive a "License not found..." error if the path to the license file contains non-ASCII characters.	Change or remove any non-ASCII characters from the license file path.
There is no distinction between output ports and bidirectional ports in AHDL Function Prototypes; instead, all ports listed after the RETURNS keyword are treated as output ports. As a result, if you specify a bidirectional port in a logic function's Function Prototype Statement and do not connect the port to a top-level bidirectional pin or to other logic in the design where you instantiate the logic function, an error can occur.	Connect the port to a top-level bidirectional pin or to other logic in the design.
Context-sensitive Help is not available for some items in the Quartus II software.	To locate Help on those items, click Search on the Help menu, and type the name of the item.

Issue	Workaround
The Classic Timing Analyzer does not recognize non-PLL clock signals when using any PLL megafunction.	Make clock settings assignments to all non-PLL clocks.
The Waveform Editor does not allow you to create a bus with nodes that are nonconsecutive members of a bus.	Create buses only with nodes that are consecutive members of a bus. Or, use the Group command on the Edit menu to create groups of arbitrary nodes.
If you are using the altcam, altclklock, altlvds_rx, or altlvds_tx megafunctions, the equations shown in the Equations Section of the Compilation Report are not complete.	To view the complete equations for any of these megafunctions, use the Equations window of the Timing Closure Floorplan.
The Quartus II software does not support design file names with more than one extension. For example, you cannot use the file name file.eda.edif .	Use design file names with only one extension.
If you install the Quartus II software for PCs on a UNIX server that exports shares with the Samba software version 1.9.18p10, you may experience problems accessing project files that are also on the network.	Altera recommends using version 1.9.16p11 or 2.0 of the Samba software.
If you make assignments to reserve pins as a group or with group notation (debug [7 . . 0]), the Quartus II software does not correctly generate simulation output files, and you receive a warning message saying "Unsupported data type in the top-level module."	Reserve the pins using single-name notation (for example, debug [7] , debug [6] , and so on).
Do not change the file permissions (such as changing "read-only" to "read and write") of Quartus II Settings File (.qsf) and Quartus II Project File (.qpf) while a Quartus II project is open.	Close the Quartus II project before making changes to the file permissions.
Node names containing numbers greater than 2 ³¹ -1 (2147483647) will cause an Internal Error in the Quartus II software.	Do not use node names containing large numbers.
Occasionally the Programmer does not allow you to use a MAX 7000AE Programmer Object File (.pof) with a MAX 7000AE device. This error sometimes occurs after a compatible MAX 7000B device is used with the MAX 7000AE POF.	Do not switch between compatible MAX 7000B and MAX 7000AE devices when a MAX 7000AE POF is loaded, or reload the MAX 7000AE POF.

Issue	Workaround
<p>Routing back-annotation may fail if the back-annotated locations do not match the location assignments in the Quartus II Settings File (.qsf) or if the location assignments are missing. This problem can occur if you change devices, or if you remove some location assignments by using the Assignment Editor on the Assignments menu or by manually editing the Quartus II Settings File.</p>	<p>If you experience a “no fit” or an Internal Error while using routing back-annotation, delete the Routing Constraints File (.rcf) and back-annotate the design again after a successful compilation.</p>
<p>Occasionally, the Quartus II software may crash or hang with no error message immediately upon opening a project.</p>	<p>Delete the Quartus II Workspace File (.qws) <project name>.qws from the project directory. If the problem persists, delete the \<project directory>\db directory and recompile the design.</p>
<p>When you are setting phase shift and duty cycle values for clock signals using the altpll megafunction, some combinations of settings may result in values that cannot be synthesized exactly. Under certain circumstances, the Quartus II software attempts to synthesize the phase shift parameter before the duty cycle parameter.</p>	<p>You should first select values for the parameter (phase shift or duty cycle) that is most important for your design.</p>
<p>During compilation or simulation, the Quartus II software may “hang” and not proceed to the next module if a menu or modal dialog box is open at the time the current module finishes running.</p>	<p>Close any open menus or modal dialog boxes before the compilation or simulation reaches the next stage.</p>
<p>Running individual Quartus II software executables (quartus_map, quartus_fit, and so on) from within the Quartus II Tcl Console may cause the Quartus II software to crash.</p>	<p>Run individual executables either from within the Quartus II scripting shell (quartus_sh) or directly at a command prompt.</p>
<p>The time shown in the Status window may not agree with the processing times reported in the Compilation Report. This difference is due to differences in how the times are calculated during processing.</p>	
<p>If you type a name in the entity column of the Assignment Editor that differs from an existing name only by case, the Assignment Editor’s “auto-completion” feature always uses the existing name.</p>	<p>Type the new entity name in another application, such as a text editor, copy it to the clipboard, and paste the name from the clipboard into the Assignment Editor.</p>

Issue	Workaround
Altera recommends that you do not use node or entity names that differ only by case if you are using the Quartus II Simulator or Waveform Editor.	
Under certain circumstances, a design that uses Virtual Pin assignments may fail to fit after back-annotation. This situation occurs because the clock signals chosen automatically for the first compilation do not match those chosen for the second compilation.	Manually assign your clock signals, using Virtual Pin Clock assignments before the first compilation, or use Advanced Back-Annotation to explicitly write out the virtual clock assignments before the second compilation.
If you use the <code>dcfifo</code> or <code>scfifo</code> megafunctions in an AHDL design, you may receive an error message similar to "The parameter <code>LPM_WIDTHU</code> has been set to an invalid value..."	Either remove the <code>LPM_WIDTHU</code> parameter arguments from your AHDL <code>dcfifo</code> or <code>scfifo</code> megafunction instantiation, or explicitly set the <code>LPM_WIDTHU</code> parameter to <code>ceil(log2(LPM_NUMWORDS))</code> .
Do not open, change permissions, or delete the <code><project directory>/db</code> directory or any file therein while any Quartus II executable is running.	
Support for non-decimal radix numbers (such as hexadecimal) used as constants in the <code>lpm_constant</code> , <code>lpm_compare</code> , and <code>lpm_add_sub</code> megafunctions is limited to values that can be represented by 31 bits or fewer.	For values that require more than 31 bits, use decimal radix only.

Issue	Workaround
<p>Under certain circumstances, back-annotation of routing in unreserved LogicLock regions can cause unsatisfiable routing constraints for signals going to clock and clock-enable ports of LABs. This can occur when other portions of the design are not back-annotated, and the Fitter populates empty LCELLs in the back-annotated LogicLock region during subsequent compilations.</p> <p>For example, assume that on the initial compilation, LogicLock region L contains register A, which uses the CLK1 and ENA1 ports of a LAB. When the design is recompiled, the Fitter may place register B, which is not part of region L, and uses the SLOAD input, in the same LAB as register A (assuming that the LAB has sufficient empty space to accommodate it).</p> <p>The LAB control signal generation block does not allow use of both ENA1 and SLOAD in the same LAB; therefore, register A must use the CLK0 and ENA0 ports, rather than CLK1 and ENA1. To avoid a no-route situation, the Fitter will ignore the routing constraints for the clock and enable signals, and re-route the signals using the appropriate control signal multiplexing for the CLK0 and ENA0 ports of the LAB. The Fitter picks the most appropriate routing and, in the majority of cases, the circuit's timing is not adversely affected. When the Fitter is forced to ignore routing constraints, info messages of the form "Info: Can't route signal <name> to atom <name>" are displayed to inform the user; the appearance of such messages is not a cause for alarm.</p>	<p>This situation can be avoided entirely by marking all LogicLock regions as Reserved, thereby preventing the Fitter from placing new items in a region. The tradeoff, of course, is that should a Reserved LogicLock region be under-utilized, the Fitter will be unable to place other logic items in the unused portion of the region.</p>

Platform-Specific Issues

Windows Platforms Only

Issue	Workaround
Version 7.2	
The SOPC Builder and Nios II IDE are not supported for Windows Vista. Also, ModelSim-Altera 6.1g that ships with the Quartus II software version 7.2 does not support Windows Vista.	
Version 7.1	
The Quartus II software may crash with an internal error if you have set any number in the range 10000 – 11000 in the Message ID box of the Advanced Message Settings dialog box from the Analysis & Synthesis page of the Settings dialog box.	Open your <i><project>.qsf</i> file in a text editor and add the following assignment to it: <pre>set_global_assignment -name HDL_MESSAGE_OFF <number></pre> Where <i><number></i> is the original message number.
On the Windows 2000 platform, the altlvds and the alt2gxb megafunctions fail to open the MegaWizard Plug-In Manager.	
Version 6.1	
If the Quartus II software is installed on a network drive, Windows is unable to start the JTAG server service because it does not have rights to read from the network drive (services run before users are logged in). If this service is not running, it is not possible for other computers to use JTAG cables on this machine. Occasionally it is not be possible for the Quartus II software to use JTAG cables attached to the same machine.	You can either install the Quartus II software locally or run <i><full-path-to>/jtagserver --install <username> <password></i> to specify the username and password that Windows should use when running the JTAG server service.
Version 6.0	
If you are running the Quartus II software on the Windows XP64 operating system with a USB Software Guard, you may receive a message that there is no license found.	You must install the Sentinel driver for the Software Guard by browsing to the quartus/drivers/sentinel/win_xp64 directory when asked for the location of the driver.

Issue	Workaround
Version 5.1 SP2 and earlier	
<p>The introduction of Microsoft Security Update MS05-026 prevents the proper display of Quartus II Help across a network.</p>	<p>To properly display HTML Help files, you must access them from a local PC. If you are unable to access Help files locally, go to Microsoft Knowledge Base Article 896054 (support.microsoft.com/?kbid=896054) for more information about possible workarounds.</p>
<p>The keyboard accelerators (underlines) for Alt+ key combinations do not appear in the Quartus II user interface until the Alt key is pressed the first time.</p>	<p>This behavior is a Windows 2000 and later Microsoft operating systems user-specified preference. To change to the previous behavior in Windows 2000 and XP, follow these steps:</p> <ol style="list-style-type: none"> 1. On the Start menu, click Control Panel. 2. Click Display properties. 3. Click the Appearance tab. 4. Click Effects. 5. Turn off Hide underlined letters for keyboard navigation until I press the Alt key.
<p>If you use Windows 2000 as a software server to serve the Quartus II software to a client computer running Windows XP, running the Quartus II software on the Windows 2000 server at the same time clients are running the Quartus II software, will cause the Quartus II software on the server to crash.</p>	<p>Do not run the Quartus II software on the Windows 2000 server.</p>
<p>You cannot access the web-based PowerPlay Early Power Estimator on the Altera web site if you have installed Windows XP SP2 because the service pack blocks the active content. email teck huat 4.2</p>	<p>Refer to the Altera Knowledge Database on the Altera website for more information on enabling your browser to access the PowerPlay Early Power Estimator spreadsheets.</p>
<p>Some dialog box title bar text is not displayed correctly when the Quartus II software is installed on a computer running the Chinese version of Windows XP.</p>	<p>Change the font in the Active Title Bar section of the Windows Appearance Control Panel.</p>

Issue	Workaround
<p>If you do not have Administrator privileges when you install the Quartus II software, certain features of the software, particularly the online Help, will not work properly, for example:</p> <ul style="list-style-type: none"> • Software guards (parallel and USB) • Programming with JTAG server 	<p>Altera recommends that you have Administrator privileges when installing the Quartus II software.</p>
<p>Under certain circumstances, the Quartus II installation program may crash or you may receive an error message immediately upon launching the installation program.</p>	<p>Reinstall the stdole32.tlb file from the original Windows distribution disks. To reinstall the file, type the appropriate command at a command prompt. (Note: the command must be typed on one line.)</p> <p>Windows 2000: <CD-ROM drive letter>:\i386\expand.exe stdole32.tl_%SystemRoot%\System32\stdole32.tlb <Enter></p> <p>Windows XP: <CD-ROM drive letter>:\i386\expand.exe stdole32.tl_%SystemRoot%\System32\stdole32.tlb <Enter></p>
<p>If the full, hierarchical name of an instance exceeds 247 characters, it may not be displayed properly in the Quartus II user interface. This problem occurs most often with EDIF netlist files generated by other EDA synthesis tools.</p>	<p>Limit the full, hierarchical instance name to fewer than 247 characters if possible.</p>
<p>If you are running the Quartus II software from a network server, the Quartus II software will not run properly on the client computer if you share the \quartus\bin directory.</p>	<p>You must share the \quartus directory, not the \quartus\bin directory.</p>
<p>The Quartus II software is not compatible with the MATLAB web server.</p>	<p>Turn off the MATLAB web server in the Services Control Panel on the Start menu before running the Quartus II software.</p>

Issue	Workaround
<p>Under some circumstances, the Quartus II splash screen appears and the Quartus II icon appears in the Taskbar, but the graphical user interface does not appear. Under other circumstances, the user interface appears but windows and/or toolbars do not appear correctly.</p>	<p>The registry settings controlling the position of the Quartus II windows may have become corrupted. If the user interface appears, click the Reset All button on the Toolbars page of the Customize dialog box, or, if the user interface does not appear, type the following command at a command prompt: <code>quartus -reset_desktop <Enter></code></p>
<p>If you install the stand-alone Quartus II Programmer and the Quartus II software, and then uninstall either one, the Programmer may report "JTAG Server -- internal error code 82 occurred" when you click the Add Hardware button in the Hardware Setup dialog box on the Edit menu. This error occurs because uninstalling the software has disabled the JTAG Server service.</p>	<p>Manually restart the JTAG Server service by locating the jtagserver.exe program and at a command prompt for that directory, type <code>jtagserver --install <Enter></code></p>
<p>If you choose to uninstall a previous version of the Quartus II software during installation, and there is a "locked" file or directory, the installation program will not reboot the computer as is necessary to successfully complete the installation.</p>	<p>Exit from the installer and reboot the computer manually after the removal of the previous version is complete, before completing the installation of the new version.</p>

Solaris & Linux

Issue	Workaround
Version 7.2	
<p>The Quartus II Interactive Tutorial is not available when you install the Altera Complete Design Suite on Solaris workstations from the Altera Complete Design Suite for UNIX and Linux version 7.2 DVD-ROM.</p>	<p>To install the Quartus II Interactive Tutorial for Solaris, install the Linux tutorial files from the Altera Complete Design Suite for UNIX and Linux version 7.2 DVD-ROM. From the top-level directory of the Quartus II installation (for example, /opt/altera72/quartus), use this command line, replacing <i><DVD></i> with the path to the DVD-ROM:</p> <pre>cat <DVD> /quartus/linux/help.gz <DVD>/tools/solaris/gzip -c -d <DVD>/tools/solaris/gtar xoUf - <enter>.</pre>
Version 6.1	
<p>Under some circumstances, your web browser software may fail to launch correctly from the IP MegaStore MegaWizard Plug-In Manager. The web browser defined in the MegaWizard Plug-In Manager for the IP MegaStore inherits the environment settings from the Quartus II software. Specifically, the LD_LIBRARY_PATH environment variable may contain entries that conflict with web browsers such as FireFox, preventing them from starting correctly.</p>	<p>Edit the script that launches the web browser to make sure the Quartus II directories are the last entries in the LD_LIBRARY_PATH variable.</p>
Version 6.0	
<p>While any shortcut menu is open from an undocked dockable window, if you right-click the title bar, then all activity in the title bar (left-click and drag, shortcut menu, 'X' close button) stops working.</p>	<p>Display a shortcut menu again and perform any action except right-clicking in the title bar to restore normal operation.</p>

Issue	Workaround
Version 5.1 SP2 and earlier	
If the operating system crashes, and the file system in \$TMP is rebuilt automatically, the data in the \$TMP/Mw_<user ID> file is corrupted, the Quartus II software may fail to start correctly.	Delete the \$TMP/Mw_<user ID> file and restart the Quartus II software.
If you are using the Exceed X server software for Windows while running the Quartus II software, the font size may be larger than the line height. This problem occurs most often if you installed the Exceed software while running at a screen resolution greater than 1024 × 768.	Reinstall the Exceed software while running at a screen resolution of 1024 × 768. You can then switch back to your normal, higher resolution setting.
You cannot launch the AXD Debugger software from within the Quartus II software.	Launch the AXD Debugger software from outside the Quartus II software.
Under some circumstances, the Internet connectivity features of the Quartus II software are not functional.	Specify the full path to your web browser software on the Internet Connectivity page of the Options dialog box. If you access the Internet through a proxy server, you must also specify the address of the proxy server and its port number.
Under some circumstances you cannot access the Quartus II online Help in the user interface.	To access Help, type hh <quartus dir>/common/help/quartus.chm <Return> at a command prompt.
If you are accessing the Quartus II software through one of the following versions of the Hummingbird Exceed software (6.2, 7.0, 7.1, or 8.0) and have any Microsoft Office application or Internet Explorer open, the Quartus II user interface may start very slowly.	Contact Hummingbird Software at www.hummingbird.com for a patch for the Exceed software.
The stand-alone Quartus II Programmer and SignalTap® II programs are not available on Solaris and Linux workstations.	

Linux Only

Issue	Workaround
Version 7.2	
Using the Quartus II software with Linux kernel 2.4 results in slower performance than Linux kernel 2.6.	For improved performance, use Red Hat Enterprise Linux 4 or later, which is a 2.6-based kernel.
Version 7.1	
On the SUSE Linux platform, the Quartus II software opens in the lower right side of the screen, even after you re-position it.	Set the environment variable QUARTUS_MWWM to the value allwm.
Version 7.0	
When you are running the Quartus II software on Red Hat Enterprise Linux 4.0 and using the GNOME desktop, you may receive an internal error when you create a LogicLock region, and then use the Add Path dialog box to add a node for the source name with the Node Finder, and then click Cancel in the Add Path dialog box.	Do not click Cancel in the Add Path dialog box after you add a node for the source name with the Node Finder.
Version 6.0	
The Quartus II software may crash with a core dump if you close the Quartus II software while a properties dialog box is open from any link in Help.	Do not open the properties dialog box on any link in Help.
Your programming hardware is not shown in the Add Hardware dialog box when running under Red Hat Enterprise Linux 64.	Only the EthernetBlaster is supported for programming on 64-bit platforms.
Version 5.1 SP2 and earlier	
If you run a remote Linux desktop session in a Windows client such as Exceed, depending on your configuration, the SignalTap II Logic Analyzer may be unstable and could crash with a segmentation fault.	Use an Xterm window to access the Quartus II software instead of a remote desktop session.

Issue	Workaround
<p>If the MasterBlaster download cable is not listed in the Available hardware items list in the Hardware Settings tab of the Hardware Setup dialog box, but it is connected properly, you may not have read/write permission for the serial (<code>dev/ttySx</code>) port to which the MasterBlaster cable is connected.</p>	<p>Have a system administrator assign read/write permission for the appropriate port. This change can be accomplished by adding you to the “uucp” group, or by giving read/write permission for the serial port to everyone, using the following command: <code>chmod o+rw /dev/ttySx</code> where <i>x</i> is the serial port affected.</p>
<p>If you are using the ReflectionX X-server software as your display on a Linux workstation, the Quartus II software may hang and a white box may appear.</p>	<p>Set the <code>QUARTUS_MWWM</code> environment variable to <code>allwm</code> and then start the Quartus II software without the splash screen by typing the following commands at a command prompt: <code>setenv QUARTUS_MWWM allwm <Return></code> <code>quartus -no_splash <Return></code></p>
<p>Under certain circumstances, the Quartus II software may not start properly.</p>	<p>On a system with a static IP address, ensure that the <code>/etc/hosts</code> file has an entry for the host name of the machine on which you are running. For example, if the workstation is named “orange,” there should be an entry in <code>/etc/hosts</code> with the IP address of the “orange” workstation as shown below: <code><IP address of orange> orange</code> In addition, the network configuration (hostname, DHCP host name, DNS search path, and domain names) must be correct or the Quartus II software will abort on startup.</p>
<p>If you are running the Quartus II software version 4.0 and later using VNC software, the Quartus II software may terminate unexpectedly whenever you open any file or browse any directory from within the Quartus II software.</p>	<p>Make sure your VNC server software is version 3.3.4 or later.</p>

Device Family Issues

Cyclone, Stratix & Stratix GX

Issue	Workaround
Version 6.0	
<p>The method used to report power for clock networks is different between the Quartus II PowerPlay Power Analyzer and the PowerPlay Early Power Estimator (EPE). The Quartus II PowerPlay analyzer reports the power for the resource (pin or PLL) that drives the network, while the EPE reports the power in the Clock Network section of the spreadsheet.</p>	<p>No action is necessary.</p>
Version 5.1 SP2 and earlier	
<p>When you use a Routing Constraints File (.rcf) to control fitting after performing Routing Back-Annotation, your timing analysis results may change slightly due to parasitic and other effects. Any change will be very small.</p>	

Cyclone III and Stratix III

Issue	Workaround
Version 7.2	
<p>For the smaller packages of Cyclone III and Stratix III devices, the Pin Planner may show DQS functionality on a pin, while the Quartus II software may not be able to use it as DQS with any DQ group in that package. In Stratix III devices, the DQS features of such pins may still be used for other purposes. For Cyclone III devices, these packages are affected:</p> <ul style="list-style-type: none"> • E144 in the EPC3C5, EPC3C10, EPC3C16 and EPC3C25 densities. <p>For Stratix III devices, these packages are affected:</p> <ul style="list-style-type: none"> • EP3SE50, package F484 • EP3SE80, package F780 • EP3SE110, package F780 • EP3SE260, package H780, package F1152 • EP3SL50, package F484 • EP3SL70, package F484 • EP3SL110, package F780 • EP3SL150, package F780 • EP3SL200, package F1152 • EP3SL340, package F1517, package H1152 	<p>Clicking Show DQ/DQS Pins in the Pin Planner shows the correct DQ/DQS groups without any unusable DQS pins.</p>
Version 7.1	
<p>Location and other assignments made to the altpll megafunction name and intended only for the PLL WYSIWYG are also applied to logic cells created by the altpll megafunction. As a result, you may see errors indicating PLL assignments do not apply to logic cell nodes.</p>	<p>Make assignments intended only for the PLL on the PLL WYSIWYG name only and not on the higher-level altpll hierarchy name.</p>

Stratix and Stratix GX

Issue	Workaround
Version 6.0	
<p>The Quartus II PowerPlay Power Analyzer reports PLL, XGMII state machine, GXB transceiver, and I/O pin power as contributors to the power reported for High Speed Transceiver blocks. However, the PowerPlay Early Power Estimator (EPE) spreadsheet reports this power in a “High Speed Transceiver Blocks” section as well as an entry in the “Clock Networks” section. Similarly, the PLL, SERDES blocks, and I/O pins of an LVDS block are reported in the PowerPlay Power Analyzer, and as entries in the Clock Networks and HSDI sections of the EPE spreadsheet.</p>	

Stratix

Issue	Workaround
<p>Designs compiled for Stratix EP1S40ES devices must be recompiled for the EP1S40 device before programming.</p>	

Stratix II

Issue	Workaround
Version 6.0 and earlier	
<p>Due to changes in the altlvds_tx and altlvds_rx megafunctions in the Quartus II software version 5.0, user-created timing assignments to the megafunctions are changed. The megafunctions now make most timing assignments automatically.</p>	<p>Check your assignments to make sure that the Quartus II software implemented them correctly.</p>
<p>The Quartus II software version 5.0 does not support programming file generation for some Stratix II devices when M-RAM blocks are used in some memory modes, and if the STRATIXII_MRAM_COMPATIBILITY option is turned off.</p>	<p>For more information about programming file support for Stratix II devices, refer to the <i>Stratix II FPGA Family Errata Sheet</i>, which is available on the Altera website.</p>

Issue	Workaround
Back-annotating some designs targeted to a Stratix II device with the Demote cell assignments to option set to LABs may prevent the design from fitting.	Back-annotate the design with Demote cell assignments to turned off.

Stratix GX

Issue	Workaround
Version 6.0	
Timing simulation performed in the Quartus II software on designs that use the altgxb megafunction in Stratix GX devices is not accurate on the rx_clkout and rx_out outputs. The simulation is functionally correct, but the relative timing delays between the signals are not accurate.	Perform your timing simulation in another tool such as ModelSim.

Stratix II GX

Issue	Workaround
Version 7.2	
<p>The VCS flag <code>-ntb_opts +check</code> can produce the following error when running Synopsys VCS simulation using stratixiigx_hssi_atoms.v (alt2gxb simulation library):</p> <pre>Error: Illegal array access.</pre> <p>This out-of-bound/illegal array access at time 0 happens at unused channels/blocks where default parameter values and initial values of ports are not consistent.</p>	Remove the <code>+check</code> option when compiling stratixiigx_hssi_atoms.v . The check is to report specifically out-of-bound or illegal array access (no other type of checking).
Stratix II GX post-fit compiler databases created in the Quartus II software version 7.1 are not backwards compatible with the Quartus II software version 7.2.	Rerun the Fitter after importing Stratix II GX projects compiled in the Quartus II software version 7.1.

Issue	Workaround
Version 6.0	
<p>The latency of alt2gxb megafunction simulations on Stratix II GX is not accurate in comparison to the device. This is due to approximation used in the Quartus II simulation in modeling the analog portion of the hardware. The latency on the digital portion is within the range of a few clock cycles of the device. The latency is an exact match with the hardware when input vectors are carefully made and do not contain any race conditions.</p>	<p>The Stratix II GX handbook has specified latency range information. The latency information from Quartus II simulations is a good approximation.</p>

Stratix III

Issue	Workaround
Version 7.2	
<p>The Quartus II software version 7.2 does not support Stratix III Error Detection.</p>	
<p>In the Quartus II software version 7.2, Stratix III devices do not support the following three primitives: ALT_OUTBUF_TRI_DIFF ALT_IOBUF_DIFF ALT_BIDIR_DIFF</p>	
<p>The Quartus II software version 7.2 may exit with an internal error for designs that use HALF_RATE_INPUT atoms in Stratix III devices that use speed grade C4L High Voltage (1100mv). The DATAIN to OUT2_DFF min delay is 1 ps larger than the max delay.</p>	<p>Select another speed grade or voltage.</p>
Version 7.1	
<p>The Design Assistant may report excessively conservative Clock Rule Warnings for some MegaCore designs that target Stratix III devices.</p>	

Issue	Workaround
If a design that targets Stratix III devices uses LVDS RX in an I/O row, you cannot use half-rate DDR on the TX pins of the same I/O row. As a result, you cannot use DQ pins of a DDR memory interface together with LVDS RX in any Horizontal I/O row.	

Cyclone

Issue	Workaround
Altera recommends that the frequency of the external clock output of the PLLs be limited to 312 MHz.	
The PLL lock circuit does not function correctly for PFD (Phase Frequency Detector) frequencies below 200 MHz when the temperature is below -20°C.	If operation at temperatures below -20°C is required, choose a higher input frequency and clock division (N) factor such that the PFD input frequency is higher than 200 MHz.

Cyclone II

Issue	Workaround
Version 5.1 SP2 and earlier	
A write error has been detected on Cyclone II M4K RAMs when using dual ports and dual clocks for designs compiled with Quartus II software version 5.0 SP1 and earlier.	A software workaround is available to address this issue in the Quartus II software version 5.0 SP2 and Quartus II software version 5.1. To learn more, refer to the Cyclone II Errata on the Altera website
If your design uses dual-port, dual-clock memory with a Memory Initialization File (.mif) and you have set the CYCLONE_SAFE_WRITE parameter in the altsyncram megafunction to RESTRUCTURE, any changes to the Memory Initialization File contents will be ignored if you have Smart Compilation turned on.	
Back-annotating some designs targeted to a Cyclone II device with the Demote cell assignments to option set to LABs may prevent the design from fitting.	Back-annotate the design with Demote cell assignments to turned off.

Cyclone III

Issue	Workaround
Version 7.2	
<p>The mode 2 DLL frequency range for Cyclone III devices is improved from 200-310 MHz to 200-350 MHz. Other modes are not changed. Other speed grades are not changed. No existing design will have worse timing and you do not need to run timing analysis again.</p>	
Version 7.1	
<p>If you create a new project, select an EP3C25 device for the Cyclone III device family, then set the configuration mode to Fast Passive Parallel in the Configuration tab of the Device and Pin Options dialog box, compilation fails because the auto EPROM selection picks an EPC4 device for the Cyclone III device family.</p>	<p>Select a different configuration mode, or if you want to use Fast Passive Parallel, turn off the Use configuration device option in the Configuration tab.</p>
<p>If you instantiate an altserial_flash_loader megafunction for a Cyclone III device and try to compile it, the Quartus II software fails in the Fitter.</p>	<p>In the Dual-Purpose Pins tab in the Device and Pin Options dialog box, set the pins as Use as regular I/O.</p>

HardCopy II

Issue	Workaround
Version 7.2	
<p>When compiling a HardCopy II design and using the HardCopy II Advisor to compare timing against the Stratix II FPGA flow, the timing for the I/Os may be different. This difference is because the FPGA compilation used Advanced I/O Timing, which is unsupported for HardCopy II devices, to get I/O delays.</p>	<p>When compiling the FPGA, disable Advanced I/O Timing by setting the Quartus II Settings File (.qsf) assignment ENABLE_ADVANCED_IO_TIMING to OFF or turn off Enable Advanced I/O Timing in the Timing Quest Timing Analyzer page in the Settings dialog box.</p>

Issue	Workaround
For HardCopy II devices, the default input delay chain settings for DQ may be too large, causing the input signals on the DQ pins to miss setup timing.	In the Delay Chain summary of the Resource section of the Fitter Report, view the default Pad to Input Register Delay setting (9, 10, 11, or 13). Then, in the Assignment Editor, add PAD_TO_INPUT_REGISTER_DELAY logic assignments to the DQ pins to set a smaller delay setting to meet setup timing.
Version 6.0	
A HardCopy II design that contains latches with preset or clear signals and a constant (VCC or GND) data, may cause the HardCopy II Revision Compare tool to report a difference in the timing constraints because of a difference in which signal is considered the enable for the latch.	No workaround is necessary, and you can safely ignore the warning.
Under certain circumstances, you may receive the following error message when migrating your Stratix II design that contains RAM blocks to HardCopy II: "Error: Source file <file> in directory <dir> was compiled at <time> and saved at <time>. The problem reported for the file is: Only in HardCopy II (<design>)."	Turn off the Auto RAM Block Balancing option for your Stratix II design and recompile the design. Then proceed with the migration process.
Version 5.1 SP2 and earlier	
PCI core designs compiled with versions of the PCI Compiler earlier than 4.0.0 will cause numerous spurious differences to be reported in the Companion Revision Compare section of the Compilation Report, even though the source files are correct.	Recompile the PCI core with the PCI Compiler version 4.0.0 or later.

EPC2 Configuration Devices

Issue	Workaround
Version 6.0	
<p>When using the EPC2 configuration device to configure an Altera FPGA using a compressed configuration bit stream, you may encounter a configuration failure due to the CONF_DONE error checking feature. The failure mode occurs when the FPGA releases the CONF_DONE signal outside the acceptable time window. The reason this may occur is because the compression ratio varies depending on the design file. Since the configuration file size varies due to compression there may be insufficient padding at the end of the configuration file. This issue can result in a configuration failure, as indicated by the nSTATUS pin transitioning low near the end of configuration. The error occurs because the CONF_DONE signal is released by the FPGA before the EPC2 device expects it to be released.</p>	<p>For assistance implementing the workaround, contact Altera Technical Support at www.altera.com/mysupport, and click Create New Service Request.</p>

Design Flow Issues**Verilog HDL Integrated Synthesis**

Issue	Workaround
<p>A Verilog HDL design that compiles successfully in earlier versions fails in the Quartus II software version 5.1 with the message "Formal port <port_name> must be connected to a structural net expression."</p>	<p>The Verilog language requires that a module instance output port be connected to a net, and not to a reg variable or to a constant. Previous versions of the Quartus II software did not enforce this restriction. Change the variable connected to the module instance output port to a wire datatype.</p>

SOPC Builder Issues

Issue	Workaround
Version 7.2	
<p>In a Nios II system, if you turn on Enable bursts for the Data master settings in the Nios II processor, data master burst reads of size > 1 from unassigned locations result in system lockup.</p>	<p>Avoid making data master reads from unassigned locations.</p>
<p>The gray drag boxes next to HDL file names in the Component Editor do not change the order of the files.</p>	<p>To change the order of the files, remove them and re-add them in the correct order.</p>
<p>If the first component added to a new SOPC Builder system is a custom component, it gets assigned the base address of 0xFFFFFFFF. Subsequent components also get assigned that base address.</p>	<p>Add a master such as Nios II to the system, and then click Assign Base Address on the System menu to correct the address assignments.</p>
<p>The Component Editor does not warn you about duplicate port names for custom instruction slave components.</p>	
<p>You may get a SEVERE: [Error.Other] Error writing cache error when SOPC Builder tries to cache components on Windows and the absolute path to the component is longer than the windows maximum file name size. The component loads after a short delay.</p>	<p>Move the component such that it's in a shorter path to shorten the load time.</p>
<p>When a latent-aware Avalon master does a read access to a nonexistent location, the Avalon bus fabric returns a dummy response so that the reading master does not stall. However, only a single response (readdatavalid pulse) is returned. If a burst read is done to a nonexistent location, the bursting master receives only the single response, and stalls while awaiting the remaining readdatavalid pulses.</p>	
<p>Component information such as the Component Display Name and Icon path may be lost if you edit a custom component in Component Editor.</p>	

Issue	Workaround
SOPC Builder generation may fail with Java errors when the system is generated from the command line using a Tcl script. These errors occur if no Xserver is running on your machine.	Set up an Xserver on your machine and regenerate the SOPC Builder system.
The SOPC Builder UI allows you to enter invalid values for arbitration shares, including very large numbers and negative numbers.	Before generating, manually check that arbitration share values are between 1 and 100, inclusive.
The SOPC Builder may generate errors regarding address span overlap when generating systems with bursting masters and wide data path widths of 32 bits or more.	Move the native addressing components farther apart so that base addresses won't overlap even if the span grows by a factor of 2 (or 4 if the data width is 128 bits).
Version 7.1 SP1	
When the parameter Allow Backpressure is enabled and the FIFO is empty, the HAL API altera_avalon_fifo_read_fifo() exits without waiting for incoming data.	If the parameter Allow Backpressure is enabled, use the macro IORD_ALTERA_AVALON_FIFO_DATA() to read from the FIFO in the user application instead of the HAL API altera_avalone_fifo_read_fifo().
Version 7.1	
Custom components created in versions of SOPC Builder earlier than 7.1 that have data widths that are not multiples of two and greater than 8 bits will not upgrade properly.	Import your custom logic into Component Editor and specify a data width that is at least eight bits wide and a multiple of two (8, 16, 32, 64, etc...) If you increase the width of your component to comply with these limits, the Quartus II software automatically removes any unused bits during synthesis.
An Avalon-MM master connected through an Avalon-MM pipeline bridge or Avalon-MM clock crossing bridge to Avalon-MM slaves that use native addressing will fail if the bridge is wider than the master.	Do not connect a narrow Avalon-MM master to a wider Avalon-MM bridge if that master accesses an Avalon-MM slave that uses native addressing through the bridge.
The Component Editor in SOPC Builder does not support Verilog HDL design files (.v) that have multiple modules or VHDL design files (.vhd) with multiple entities.	Use only one module for each Verilog HDL design file and one entity for each VHDL design file.
If a module dependency loop is reported between the DMA controller and pipeline bridge, the resulting system may still be functional.	The system can be generated by holding down Ctrl and clicking the Generate button.

Issue	Workaround
Version 7.0	
If a one-bit port on a VHDL component is defined as a <code>STD_LOGIC_VECTOR (0 downto 0)</code> the port width will be misinterpreted during SOPC Builder system generation.	Define all single-bit ports as <code>STD_LOGIC</code> .
Version 6.1	
<p>Compiling an SOPC Builder design generates the following message:</p> <pre> "Warning: Found invalid timing assignments -- see Ignored Timing Assignments report for details." </pre> <p>SOPC Builder erroneously applies an invalid timing assignment as an embedded attribute in the HDL code it generates.</p>	You can ignore these warnings for the SOPC Builder system.
Version 6.0	
The Avalon Interface Specification incorrectly describes the behavior for <code>address</code> and <code>burstcount</code> during burst transfers. The Avalon Interface Specification states: "The start of a write burst is similar to the start of a fundamental master write transfer. The master port asserts <code>address</code> , <code>writedata</code> , <code>write</code> , and <code>byteenable</code> (if present) in addition to <code>burstcount</code> This is the only time that the Avalon switch fabric captures <code>burstcount</code> and <code>address</code> ; the master port can deassert them through the remainder of the burst."	During Avalon master transfers, assert constant values on <code>address</code> and <code>burstcount</code> for the duration of the burst.
If multiple masters control a slave that asserts <code>endofpacket</code> , both masters will see the asserted <code>endofpacket</code> . This may cause problems in systems where masters take action upon <code>endofpacket</code> .	Use <code>endofpacket</code> only in the case that a single master of the asserting slave will take action on the <code>endofpacket</code> .
Version 5.1 SP2 and earlier	
Under some circumstances, the automatic addressing feature does not function correctly.	Assign the base address for the component manually.

Issue	Workaround
Under some circumstances, the SOPC Builder does not display correctly on systems in which the graphics card uses hardware acceleration.	Turn off, or reduce the level of hardware acceleration.
In SOPC Builder, Avalon Masters that address more than 32 bits of slave address space do not issue warning.	Redesign your system to avoid giving masters greater than 32 bits of address space.
SOPC Builder fails to open on UNIX when invoked from the MegaWizard Plug-In Manager .	Open SOPC Builder by clicking SOPC Builder on the Quartus II Tools menu.
When creating a component with the SOPC Builder Component Editor, you must not choose a component name that exactly matches the HDL file name or the top-level module name. If the names are the same, SOPC Builder will generate an error during system generation. This problem will be fixed in a future version of SOPC Builder.	Using the SOPC Builder Component Editor, rename the component to a different name. In the SOPC Builder table of active components, add the newly-named component to your system, and delete the old component.
The SOPC Builder and Nios II Software Development Kit shell may “hang” and become unresponsive if you run either program while the Frisk antivirus software is running.	Turn off the Dynamic Virus Checking feature of the Frisk software before running SOPC Builder or the Nios II SDK shell.

EDA Integration Issues

Issue	Workaround
Version 7.2	
When reporting timing, the Synopsys PrimeTime software issues an error message (UITE-461) that states that rise_edge or fall_edge cannot be satisfied, and assumes zero source latency for certain derived clocks.	Set variable timing_edge_specific_source_latency to false in the PrimeTime shell before reporting timing.
When you use NativeLink to simulate mixed HDL designs, Synopsys VCS MX shows the following errors and stops simulation: Error: VCS MX: sh: line 1: vhdlan: command not found Error: VCS MX: common elaboration failed	Set environment variable QUARTUS_INIT_PATH to the location of VCS MX executables before starting the Quartus II software.

Issue	Workaround
<p>Mentor Graphics ModelSim Altera Edition 6.1g and the ModelSim SE 6.1g software may run out of memory with an error on the Windows platform, when compiling or simulating a large post-fit netlist.</p>	<p>Use a 64-bit computer running the Linux operating system to compile and simulate the design. Contact Mentor Graphics for additional support.</p>
<p>Version 7.1</p>	
<p>If your design contains WYSIWYG atoms, and you select another family in the Quartus II project, RTL Simulation using NativeLink results in errors.</p>	<p>If your design contains a clear box netlist generated for a specific device family, and you target a different device family in the Quartus II project, regenerate the clear box netlist for the correct device family. If your design contains IP, check IP documentation to verify whether it supports NativeLink simulation.</p>
<p>Version 6.1</p>	
<p>If there are virtual I/O pin assignments at the time of generating board-level timing files in the STAMP format, and if there is any other tool or format selected in any EDA tool category on the EDA Tool Settings page, you may receive an error when you run the EDA Netlist Writer.</p>	<p>If the design has virtual I/O pin assignments, and you want to generate board-level timing files in the STAMP format, then either remove the virtual I/O pin assignments from the Quartus II Settings File (.qsf) and recompile the design, or make sure the following is true before running quartus_eda: All tool and format settings in all categories are set to None with the exception of Board-Level timing analysis tool category. STAMP is selected as the EDA format in the Board-Level Timing Analysis tool category in the Board-Level page under EDA Tool Settings. Or, you can run the following command at a system command prompt:</p> <pre>quartus_eda --format=stamp -- board_timing <project> -c <revision></pre>

Issue	Workaround
Version 6.0	
The ModelSim software may fail to simulate a design if Glitch Filtering is turned on in the EDA Simulation Settings page and the <code>+nospecify</code> option is passed to the ModelSim <code>vsim</code> command.	Remove the <code>+nospecify</code> option from the ModelSim <code>vsim</code> command.
If you add or change a component in a Library Mapping File (<code>.lmf</code>), the Quartus II software does not recognize the changes upon the next compilation.	Delete the project database (db) directory and recompile.
Version 5.1 SP2 and earlier	
FIFO Partitioner instances can only be simulated in 3 rd party simulators using the original VHDL source files from the quartus/libraries/megafunctions/ directory, and NativeLink integration is not supported.	Perform simulation manually as described in the FIFO Partitioner User Guide available from the Literature page of the Altera web site.
The current version of the Quartus II software allows you to select the Synplicity Amplify software as a physical optimization tool. However, this setting is for an automated mode called ATOPS, which is currently not supported by the Amplify software.	Contact Synplicity for the support schedule for the Amplify software ATOPS mode.
NativeLink support does not work with versions of Mentor Graphics Precision RTL Synthesis Software earlier than version 2003b due to a change in the Precision project interface.	

Memory Interfaces Issues

Issue	Workaround
Version 7.2	
<p>Automatic placement of the mimic path register in designs that contain ALTMEMPHY megafunctions may be sub-optimal.</p> <p>The DDR timing report shows a failing path from the CK memory clock output port to the mimic data metastable register. The Report DDR command in the TimeQuest Timing Analyzer labels this path as Mimic (Setup).</p>	<p>The destination register for this path needs to be placed manually:</p> <ol style="list-style-type: none"> 1. Make sure the mem_clk pins have been given location constraints. 2. Locate the destination register of the path by viewing the failing path in the TimeQuest analyzer and right-click Locate Path. Click Chip Planner. 3. Then find the mimic path register (its name ends in ...mimic_data_in_metastable) and drag it into a core register location, close to the mem_clk pin that drives it. 4. Recompile, and the path should now meet timing.
<p>If you have created a design partition for an ALTMEMPHY variation in your design, synthesis cannot remove any unused I/O OBUF primitives from the partition. This causes an error in the partition merge step in the form:</p> <pre>Error: Output port DATAOUT of DDIO_OUT primitive <primitive name> must drive input port I of I/O OBUF primitive.</pre> <p>One instance of this is the mem_odt pin on the ALTMEMPHY variation that is not used for DDR SDRAM.</p>	<p>Edit the ALTMEMPHY VHDL or Verilog variation file for which the design partition has been created, and remove the pin (named <i><primitive_name></i>) that is the source of the problem from the port definition. When you rerun synthesis, the logic associated with the unused pin is removed successfully.</p>
<p>If you have, in the same project, more than one ALTMEMPHY variation generated in different versions of the Quartus II software, you may see a Verilog syntax error reported by synthesis. This error is caused by a common file used by all ALTMEMPHY variations, that has changed from an earlier version of the Quartus II software.</p>	<p>Open all the variations in the ALTMEMPHY MegaWizard in the latest version of the Quartus II software and regenerate them.</p>

Issue	Workaround
<p>By default, a QDRII SRAM PHY generated with the ALTMEMPHY megafunction does not use the parallel on-chip termination feature of Stratix III devices for the mem_dqs (CQ), mem_dqsn (CQ#), and mem_dq (Q) input pins.</p>	<p>If you want to use this feature, turn on the Enable dynamic parallel on-chip termination (OCT) option on the PHY Settings tab in the ALTMEMPHY MegaWizard. The termination is enabled statically rather than dynamically as the option suggests.</p>
<p>Quartus II software version 7.1 designs that target Stratix III devices and that contain DDR SDRAM High Performance Controller, DDR2 SDRAM High Performance Controller, DDR3 SDRAM High Performance Controller, or ALTMEMPHY megafunction variations, may not pass Mapper or Fitter legality checks.</p>	<p>For each failing megafunction variation, re-generate it by going to the MegaWizard Plug-in Manager, selecting Edit an existing custom megafunction variation, selecting the megafunction file, and clicking Finish.</p>
<p>The ALTMEMPHY megafunction, when targeting Cyclone III devices, generates a PLL. The Quartus II software issues a warning regarding PLL compensation mode when the ALTMEMPHY megafunction is compiled, for example:</p> <pre>Critical Warning: PLL "<pll instance name>" input clock inclk[0] is not fully compensated because it is fed by a remote clock pin "Pin_V9"</pre> <p>The warning may be safely ignored.</p>	
<p>DDR3 SDRAM PHY variations generated with an ALTMEMPHY megafunction in the Quartus II software version 7.2 have a fixed short memory initialization sequence for reduced simulation time. This does not comply with the required reset and initialization procedure specified by JEDEC and may cause warnings from DDR3 SDRAM simulation models.</p>	

Issue	Workaround
<p>If you are simulating a VHDL instance of the ALTMEMPHY megafunction or the DDR or DDR2 SDRAM High Performance Controllers, and if your design targets either Cyclone III or Stratix III devices, you may receive an <code>Iteration limit reached</code> error message or <code>Failure: -- SIMULATION FAILED</code> message from the example testbench and you are then unable to correctly simulate your system.</p>	<p>If your Stratix III or Cyclone III VHDL simulations are not working with the ALTMEMPHY megafunction, you may have to apply a patch to the simulation model (<code><variation name>.vho</code>) of the PHY. For more information, visit the Knowledge Database at http://www.altera.com/support/kdb/kdb-index.jsp for the solution rd10012007_32.</p>
<p>For Stratix III devices, turning on the dynamic parallel on-chip termination (OCT) option in the ALTMEMPHY MegaWizard or DDR/DDR2 SDRAM High Performance Controller may result in an internal error in the Assembler.</p>	<p>Add the following lines to the Quartus II Settings File (<code>.qsf</code>) for your project:</p> <pre>set_instance_assignment -name D5_OCT_DELAY 0 -to mem_dqs set_instance_assignment -name D5_OCT_DELAY 0 -to mem_dqsn set_instance_assignment -name D5_OCT_DELAY 0 -to mem_dq set_instance_assignment -name D5_OCT_DELAY 0 -to mem_dm</pre> <p>Modify the names to match the DQS, DQSn, DQ, and DM pin names in your design.</p>
<p>The Quartus II software version 7.2 does not support automatic placement of the write data clock output pins when you use the ALTMEMPHY megafunction.</p> <p>For Stratix III DDR/DDR2/DDR3 SDRAM High Performance Controllers, the Quartus II software automatically places the write data clock output pins correctly, but not for the QDRII+/QDRII SRAM ALTMEMPHY interface.</p>	<p>Place the <code>mem_clk</code> pin for clocking write data on a DQS pin for QDRII+/QDRII SRAM memory interfaces.</p>

Issue	Workaround
<p>The Quartus II software version 7.2 does not support automatic placement of the clock output pins when you use the ALTMEMPHY megafunction.</p> <p>For Cyclone III devices, the Quartus II software does not correctly place the clock output pins for any memory interface type.</p>	<p>Place the mem_clk and mem_clk_n memory clock pins on DIFFOUT p- and n-pins.</p>
<p>Designs with the ALTMEMPHY megafunction that target Stratix II devices for 333MHz DDR2 SDRAM interfaces may not meet timing on the postamble paths in a default compilation.</p>	<p>Place the registers manually on the resynchronization and postamble paths close to the I/O pins. Some designs may require additional modification. Contact Altera Technical Support at www.altera.com/mysupport and click Create New Service Request.</p>
<p>Version 7.1</p>	
<p>When using the Quartus II software version 7.1 to edit an ALTMEMPHY variation generated with the Quartus II software version 6.1 or 7.0, you will see errors reported by the Quartus II synthesis reporting that modules cannot be declared more than once if you had previously added all the ALTMEMPHY source files to your project. This occurs because the generated source files have changed in 7.1, and you now have a mix of source files from 7.1 and 6.1/7.0 in your project.</p>	<p>Delete the .v/.vhd source files that match the pattern "*alt_mem_phy*" and remove them from your project file list before editing the ALTMEMPHY variation.</p>
<p>Version 6.1</p>	
<p>The assignments generated for the ALTMEMPHY megafunction, in the <code><variation_name>_pin_assignments.tcl</code> file, assume that the top-level pin names match the pins on the ALTMEMPHY variation. Using different names for your top level pins, including using single bit signals instead of one-bit busses, will result in incorrect behavior.</p>	<p>Use the Assignment Editor or Pin Planner to change the assignments to match the top-level pin names in your design.</p>

Simulation Model Changes

altera_mf Models

Model	Changes
dcfifo _mixed _widths, dcfifo	<ul style="list-style-type: none"> Added support for new aclr synchronization logic, which is used when parameter WRITE_ACLR_SYNC is set to ON Changed model to output 'X' when the fifo underflows or overflows until next reset occurs
altlvds _rx	<ul style="list-style-type: none"> Added support for new parameters, which are available for Soft Cdr mode only: SIM_DPA_NET_PPM_VARIATION SIM_DPA_IS_NEGATIVE_PPM_DRIFT ENABLE_DPA_INITIAL_PHASE_SELECTION DPA_INITIAL_PHASE_VALUE Changed flexible LVDS to do a complete reset when PLL is reset
altlvds _tx	<ul style="list-style-type: none"> Changed flexible LVDS to do a complete reset when PLL is reset Updated tx_outclock generation for flexible LVDS so that it will align with the new tx_out data Added support for the new parameter PLL_SELF_RESET_ON_LOSS_LOCK for Stratix III and Cyclone III flexible LVDS
altsyncram	<ul style="list-style-type: none"> Changed model to output 'X' when write and read operation happen to the same address simultaneously when separate clocks are used for read and write ports Changed Stratix III and Cyclone III RAM model behavior so that when address clear goes high, the output latch is invalidated

Additional Notes:

- The Memory Initialization File (.mif) is now supported for all the RAM models.
- The “Extended linear address record” type of the Intel HEX format is now supported for all the RAM models.

Latest Known Quartus II Software Issues

For more information about known software issues, look for information in the **Quartus II Software Support** page at the following URL:

<http://www.altera.com/support/software/sof-quartus.html>

Software Issues Resolved

This section list the numbers of the Customer Service Requests that were fixed or otherwise resolved in this version of the Quartus II software.

Customer Service Request Numbers Resolved in this Release				
10232755	10276568	10394942	10414612	10441686
10488662	10493090	10498844	10504477	10506171
10506555	10507339	10514936	10515757	10516690
10517919	10519034	10522341	10523270	10523678
10524757	10527351	10528378	10530607	10530730
10531296	10532606	10532628	10533751	10534821
10536369	10536378	10536934	10538637	10540271
10542942	10543641	10548197	10549965	10551743
10551745	10552051	10552547	10553891	10555253
10556455	10558118	10558895	10559004	10561380
10561413	10561414	10561512	10564340	10564864
10565355	10565878	10566737	10566737	10568401
10568556	10568742	10568816	10569497	10569902
10571843	10571942	10572662	10572946	10573144
10573592	10574282	10574567	10575309	10577313
10578840	10578866	10579125	10579955	10580053
10580155	10580294	10580464	10580561	10580661
10580688	10581081	10581085	10581700	10581878
10581890	10581916	10582047	10582095	10582170
10582178	10582239	10582428	10582688	10582821
10582893	10583071	10583232	10583573	10583577
10583726	10584104	10584351	10584417	10585020
10585528	10585943	10585976	10585989	10586111
10586173	10586266	10586272	10586272	10586451
10586534	10586738	10586836	10587234	10587281
10587595	10587670	10587750	10587758	10587799
10587860	10587966	10588104	10588477	10588563

Customer Service Request Numbers Resolved in this Release				
10588672	10588840	10588974	10589306	10589433
10589478	10589515	10589653	10589780	10590015
10590080	10590270	10590345	10590487	10590636
10590773	10591018	10591177	10591343	10591357
10591370	10591556	10591749	10591763	10591883
10591996	10592011	10592367	10592519	10592660
10592678	10592829	10592847	10592930	10593052
10593097	10593171	10593297	10593350	10593370
10593449	10593478	10593488	10593505	10593742
10593817	10593855	10593927	10593979	10594026
10594041	10594074	10594225	10594246	10594341
10594409	10594439	10594647	10594755	10594972
10594980	10594988	10595050	10595086	10595119
10595263	10595271	10595342	10595362	10595506
10595623	10595646	10595684	10595763	10595784
10595814	10595826	10595964	10596167	10596219
10596315	10596335	10596341	10596350	10596428
10596561	10596590	10596629	10596679	10596732
10596976	10596977	10597043	10597108	10597152
10597157	10597202	10597225	10597255	10597276
10597325	10597465	10597728	10597744	10597781
10597828	10598179	10598216	10598256	10598257
10598338	10598429	10598451	10598459	10598510
10598524	10598701	10598746	10598752	10598768
10598786	10599107	10599277	10599333	10599346
10599834	10599855	10599898	10599902	10599911
10600028	10600151	10600197	10600251	10600312
10600345	10600362	10600367	10600380	10600392
10600438	10600532	10600555	10600621	10600640
10600973	10601013	10601078	10601117	10601142
10601204	10601292	10601392	10601436	10601520
10601600	10601612	10601621	10601729	10601742
10601817	10601830	10601839	10601852	10601902
10601990	10602030	10602054	10602065	10602074
10602112	10602113	10602199	10602209	10602236
10602374	10602434	10602491	10602509	10602572
10602650	10602804	10602892	10602897	10603020
10603045	10603066	10603086	10603105	10603112
10603147	10603216	10603245	10603533	10603646
10603706	10603844	10604080	10604136	10604152

Customer Service Request Numbers Resolved in this Release				
10604223	10604273	10604613	10604756	10604859
10604870	10605028	10605267	10605296	10605532
10605543	10605664	10605801	10605928	10605959
10606034	10606071	10606098	10606100	10606112
10606132	10606408	10606698	10606827	10606864
10606950	10606972	10607021	10607059	10607129
10607377	10607492	10607563	10607638	10608049
10608089	10608098	10608275	10608439	10608517
10608611	10608715	10608800	10609087	10609151
10609328	10609858	10610181	10610534	10612039

Revision History

Revision	Description
1.0	Initial Release

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