

This document provides late-breaking information about device support in this version of the Altera® Quartus® II software. For information about disk space and system requirements, refer to the **readme.txt** file in your **altera/<version number>/quartus** directory. For information about New Features, EDA Tool version support, and existing and resolved software issues, refer to the *Quartus II Software Release Notes*.

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## Device Support & Pin-Out Status

This section contains information about the status of support in the Quartus II software for the devices listed.

### Full Device Support

Full compilation, simulation, timing analysis, and programming support is now available for the following new devices and device packages:

#### Devices with Full Support

Device Family	Devices	
Arria® II GX	EP2AGX45DF25	EP2AGX45DF29
	EP2AGX45CU17	EP2AGX65DF25
	EP2AGX65DF29	EP2AGX65CU17
	EP2AGX125ESDF25	EP2AGX125ESDF29
	EP2AGX125ESEF35	
Cyclone® III LS	EP3CLS150F780	EP3CLS150F484
	EP3CLS200F780	EP3CLS200F484

### Devices with Full Support

Stratix® IV	EP4SE530ESH35	EP4SE530ESH40
	EP4SE530ESF43	EP4SGX180KF40
	EP4SGX180HF35	EP4SGX180DF29
	EP4SGX180FF35	EP4SGX230KF40
	EP4SGX230HF35	EP4SGX230DF29
	EP4SGX230FF35	EP4SGX530ESHH35
	EP4SGX530ESKH40	EP4SGX530ESNF45
	EP4S40G2F40	EP4S100G2F40

### Advance Device Support

Compilation, simulation, and timing analysis support is provided for the following devices that will be released in the near future. Although the Compiler generates pin-out information for these devices, it does not generate programming files for them in this release.

### Devices with Advance Support

Device Family	Devices	
Cyclone III LS	EP3CLS70F484	EP3CLS70U484
	EP3CLS70F780	EP3CLS100F484
	EP3CLS100U484	EP3CLS100F780
Stratix IV	EP4SE360H29	EP4SE360F35
	EP4SE820H35	EP4SE820H40
	EP4SE820F43	EP4SGX70HF35
	EP4SGX110HF35	EP4SGX290KF43
	EP4SGX290NF45	EP4SGX360KF43
	EP4SGX360NF45	EP4SGX530KF43
	EP4S100G3F45	EP4S100G4F45
	EP4S40G5H40	EP4S100G5F45
	EP4S100G5H40	

### Initial Information Device Support

Compilation, simulation, and timing analysis support is provided for the following devices that will be released in the near future. Programming files and pin-out information, however, are not generated for these devices in this release.

### Devices with Initial Information Support

Device Family	Devices	
Cyclone IV GX	EP4CGX15BF14	EP4CGX15BN11
	EP4CGX22BF14	EP4CGX22CF19
	EP4CGX30BF14	EP4CGX30CF19

## Compilation Support

Compilation support with preliminary timing and power analysis support is provided for the following HardCopy<sup>®</sup> III, HardCopy IV E, and HardCopy IV GX devices.

### Devices with Compilation Support

Device Family	Devices	
HardCopy III	HC325FF484	HC325FF780
	HC325WF484	HC325WF780
	HC335LF1152	HC335FF1152
	HC335LF1517	HC335FF1517
HardCopy IV E	HC4E25WF484	HC4E25FF484
	HC4E25WF780	HC4E25FF780
	HC4E35LF1152	HC4E35FF1152
	HC4E35LF1517	HC4E35FF1517
HardCopy IV GX	HC4GX15LF780	HC4GX15LAF780
	HC4GX25FF1152	HC4GX25LF780
	HC4GX25LF1152	HC4GX35FF1152
	HC4GX35FF1517	

## Memory Requirements/Recommendations

A full installation of the Altera Complete Design Suite version 9.1 requires approximately 8.2 GB of available disk space on the drive or partition where you are installing the Altera Complete Design Suite and approximately 30 MB of available space on the drive that contains your TEMP directory (Windows only).

The Quartus II Stand-Alone Programmer requires a minimum of 1 GB of RAM plus additional memory, based on the size and number of SOF files and the size and number of devices being configured.

Altera recommends that your system be configured to provide swap space (virtual memory) equal to the recommended physical RAM that is required to process your design.

The following table shows the memory required to process designs targeted for Altera devices.

**Memory Requirements/Recommendations (Part 1 of 2)**

<b>Device</b>	<b>Recommended Physical RAM</b>	
	<b>32-bit</b>	<b>64-bit</b>
Arria GX (EP1AGX20C) Cyclone (EP1C3, EP1C4, EP1C6, EP1C12, EP1C20) Cyclone II (EP2C5, EP2C8, EP2C20) Cyclone III (EP3C5, EP3C10, EP3C16, EP3C25, EP3C40) Cyclone IV GX (EP4CGX15B, EP4CGX22B, EP4CGX30B) All MAX <sup>®</sup> 3000A All MAX 7000 All MAX 7000AE All MAX 7000B All MAX 7000S All MAX series and MAX II device families Stratix (EP1S10, EP1S20) Stratix GX (EP1SGX10) Stratix II (EP2S15)	512 MB	512 MB
Cyclone III (EP3C55, EP3C80)	768 MB	1.0 GB
Arria II GX (EP2AGX45) Cyclone II (EP2C35, EP2C50) Stratix (EP1S25, EP1S30, EP1S40, EP1S60) Stratix GX (EP1SGX25, EP1SGX40) Stratix II (EP2S30) Stratix II GX (EP2SGX30, EP2SGX60) Stratix III (EP3SL50, EP3SE50, EP3SL70) Arria GX (EP1AGX35C, EP1AGX35D, EP1AGX50D, EP1AGX60C, EP1AGX60D, EP1AGX60E)	1.0 GB	1.5 GB
Arria II GX (EP2AGX65) Cyclone II (EP2C70) Cyclone III (EP3C120) Cyclone III LS (EP3CLS70, EP3CLS100) HardCopy II (HC210) Stratix (EP1S80) Stratix II (EP2S60, EP2S90) Stratix II GX (EP2SGX90) Stratix III (EP3SE80) Arria GX (EP1AGX90E) Stratix IV (EP4SGX70)	1.5 GB	2.0 GB

**Memory Requirements/Recommendations (Part 2 of 2)**

Device	Recommended Physical RAM	
	32-bit	64-bit
Arria II GX (EP2AGX95, EP2AGX125, EP2AGX190) Cyclone III LS (EP3CLS150, EP3CLS200) Stratix II (EP2S130, EP2S180) Stratix II GX (EP2SGX130) HardCopy II (HC220, HC230, HC240) Stratix III (EP3SL110, EP3SE110, EP3SE150, EP3SL200) Stratix IV (EP4SGX110, EP4SGX230) Stratix IV GT (EP4S40G2 and EP4S100G2)	3.0 GB	4.0 GB
Arria II GX (EP2AGX260) Stratix III (EP3SE260, EP3SL340) Stratix IV (EP4GS290)	4.0 GB	6.0 GB
Stratix IV (EP4SGX360, EP4SGX530, EP4SE530) Stratix IV GT (EP4S40G5, EP4S100G3, EP4S100G4, and EP4S100G5) HardCopy III HardCopy IV (HC4E25)	N/A	8.0 GB
Stratix IV (EP4SE820)	N/A	12.0 GB
HardCopy IV (HC4E35)	N/A	16.0 GB

**Timing and Power Models**

This section contains a summary of timing and power model status in the current version of the Quartus II software.

**Devices with Timing and Power Models (Part 1 of 3)**

Device Family	Device	Timing Model Status	Power Model Status
Arria GX	EP1AGX20	Final – 7.2	Final – 7.2
	EP1AGX35	Final – 7.2	
	EP1AGX50	Final – 7.2	
	EP1AGX60	Final – 7.2	
	EP1AGX90	Final – 7.2	
Arria II GX	EP2AGX45	Preliminary	Preliminary
	EP2AGX65		
	EP2AGX95		
	EP2AGX125		
	EP2AGX190		
	EP2AGX260		

**Devices with Timing and Power Models (Part 2 of 3)**

Device Family	Device	Timing Model Status	Power Model Status
Cyclone III	EP3C5	Final – 8.0 SP1	Final – 8.1
	EP3C10	Final – 8.0 SP1	
	EP3C16	Final – 8.0 SP1	
	EP3C25	Final – 7.2 SP1	
	EP3C40	Final – 8.0	
	EP3C55	Final – 8.0	
	EP3C80	Final – 8.0	
	EP3C120	Final – 7.2 SP1	
Cyclone III LS	EPC3LS70	Preliminary	Preliminary
	EPC3LS100		
	EPC3LS150		
	EPC3LS200		
Cyclone IV GX	EP4CGX15	Preliminary	Preliminary
	EP4CGX22		
	EP4CGX30		
HardCopy II	HC210	Correlated – 8.0	Correlated – 7.2
	HC210W		
	HC220		
	HC230		
	HC240		
HardCopy III	(All)	Preliminary	Preliminary
HardCopy IV-E	(All)	Preliminary	Preliminary
HardCopy IV GX		Preliminary	Preliminary
MAX IIZ	EPM240Z	Final – 9.0 SP1	Final – 9.0 SP1
	EPM570Z		
Stratix II GX	EP2SGX30	Final – 7.0	Final – 7.1
	EP2SGX60	Final – 7.0	
	EP2SGX90	Final – 6.1	
	EP2SGX130	Final – 6.1	
Stratix III <i>(1)</i>	EP3SE50	Final – 9.0	Final – 9.0
	EP3SE80	Final – 8.1	
	EP3SE110	Final – 8.1	
	EP3SE260	Final – 9.0	
	EP3SL50	Final – 9.0	
	EP3SL70	Final – 9.0	
	EP3SL110	Final – 8.1	
	EP3SL150	Final – 8.1	
	EP3SL200	Final – 9.0	
	EP3SL340	Final – 8.1	

**Devices with Timing and Power Models (Part 3 of 3)**

Device Family	Device	Timing Model Status	Power Model Status
Stratix IV	EP4SE230	Preliminary	Preliminary
	EP4SE530		
	EP4SGX70		
	EP4SGX110		
	EP4SGX180		
	EP4SGX230		
	EP4SGX290		
	EP4SGX360		
	EP4SGX530		

**Notes:**

(1) See “Stratix III Timing Model Changes”

The current version of the Quartus II software also includes final timing models for the Cyclone, Cyclone II, MAX, MAX II, Stratix, Stratix II, and Stratix GX device families. Timing models for these device families became final in the Quartus II software versions 6.0 and earlier.

The current version of the Quartus II software also includes final power models for the Cyclone, Cyclone II, MAX, MAX II, Stratix, Stratix II, and Stratix GX device families. Power models for these device families became final in the Quartus II software versions 6.0 and earlier.

The Quartus II software version 8.1 delivers final timing models for automotive grade devices in the MAX, MAX II, and Cyclone device families.

## Cyclone III Timing Analysis Updates

This section details all Cyclone III timing analysis updates in the Quartus II software.

### Changes in the Quartus II software versions 9.0 SP1, 9.0 SP2, and 9.1

The Cyclone III timing analysis has been updated in the Quartus II software version 9.0 SP1. The clock enable path to the M9K was not analyzed in the Quartus II software version 9.0 and earlier for certain M9K configurations. This issue has been fixed in the Quartus II software version 9.0 SP1. The performance of most designs is not significantly affected by this change.

For details, search the Altera Knowledge Database with Solution ID [rd04302009\\_15](#).

**Applies to:** Cyclone III devices

## Stratix III Timing Model Changes

This section details all Stratix III timing model updates in the Quartus II software.

### Changes in the Quartus II software version 9.1

Stratix III I4 timing models have been updated in the Quartus II software versions 9.0 SP2 and 9.1. Only timing delays in Low Power mode LABs and Low Power mode MLABs in I4 industrial speed grade devices are affected. This change in the timing models may affect your static timing analysis and fitting result. Existing designs that target Stratix III I4 devices might exhibit some degradation in performance after timing analysis with the TimeQuest Timing Analyzer in the Quartus II software version 9.1. Other speed grade devices (I3, I4L, and all commercial speed grades) are not affected.

The Stratix III timing models have been updated in the Quartus II software version 9.0 SP2 for the following reasons:

- There is a larger than expected delay variation value for the DQS clock and resynchronization clock paths in the DDIO input block. This update increases the on-die variation and clock uncertainty associated with some DQS clock paths (when used to drive a local interconnect in the core fabric) and the resynchronization clock path (when used to drive the half rate block or local interconnect in the core fabric.)
- External memory interface designs built using stock ALTMEMPHY cores are not affected. The update potentially affects designs that use the customized versions of external memory interfaces in DDR, DDR2, RLDRAM, or QDR.

For details, search the Altera Knowledge Database with Solution ID [rd06172009\\_489](#).

The Stratix III timing models have been updated in the Quartus II software version 9.0 SP1 for the following reasons:

- Added a clock enable path to the M9K and M144K timing models that was missing in the Quartus II software version 9.0 and earlier.
- Corrected the T4 (DDIO\_MUX) timing models to accurately analyze timing on DDIO output paths.
- Corrected the write leveling delay chain timing models to eliminate the possibility of hardware functional failures in designs implementing DDR3 interfaces with leveling.

For details, search the Altera Knowledge Database with Solution ID [rd04292009\\_804](#).

**Applies to:** Stratix III devices

## Changes in Device Support

### Design Software Support for Mature Device Families

Design software support for FLEX, APEX, ACEX, and HardCopy Stratix device families is not provided in versions of the Quartus II software beginning with version 9.1. Use the Quartus II software version 9.0 or earlier to support those devices. The Quartus II software version 9.0 and the associated service packs will remain available on the Altera website (<http://www.altera.com>).

**Applies to:** ACEX, APEX, FLEX and HardCopy Stratix device families

### Higher global clock $f_{MAX}$ supported by Cyclone III and Stratix III devices

Higher global clock  $f_{MAX}$  is now supported by Stratix III devices:

Speed grade	$f_{MAX}$	Previous $f_{MAX}$
C2	730 MHz	600 MHz
C3/13	700 MHz	500 MHz
C4	No change	450 MHz
C4L/14L	No change	375 MHz

**Applies to:** Stratix III devices

Higher global clock  $f_{MAX}$  is now supported by Cyclone III devices:

Speed grade	$f_{MAX}$	Previous $f_{MAX}$
C6	No change	500 MHz
C7/17	437.5 MHz	400 MHz
A7/C8	402 MHz	350 MHz

**Applies to:** Cyclone III devices

### x8 and xN Clock Line Timing Issue for Stratix IV GX and GT devices

The Quartus II software version 9.1 does not implement the correct xN line transceiver data rate restrictions for Stratix IV GX or Stratix IV GT production devices. Refer to the *Stratix IV GX and Stratix IV GT Device Errata Sheet* section "x8 and xN Clock Line Timing Issue for Transceivers" for the actual xN line data rate restrictions in Stratix IV GX and Stratix IV GT production devices, respectively, and how to achieve successful Quartus II compilation at these data rates.

**Applies to:** Stratix IV GX and Stratix IV GT devices

## x8 and xN Clock Line Timing Issue for HardCopy IV GX devices

The Quartus II software version 9.1 does not implement any xN line transceiver data rate restrictions for HardCopy IV GX devices. HardCopy IV GX devices have the same xN line data rate restrictions as Stratix IV GX devices. Refer to the *Stratix IV GX Device Errata Sheet* section “x8 and xN Clock Line Timing Issue for Transceivers” for the xN line data rate restrictions in HardCopy IV GX devices.

**Applies to:** HardCopy IV GX devices

## Higher input clock rate using LVDS for Arria GX devices

The specification for maximum input clock rate using LVDS increased from 598 MHz to 640 MHz.

**Applies to:** Arria GX devices

## Default low temperature for Cyclone IV GX I7 devices

The default low temperature for Cyclone IV I7 devices is set to 0° C in the Quartus II software version 9.1 rather than the default of -40° C.

**Applies to:** Cyclone IV GX devices

## Incorrect Pin-out for HardCopy IV GX devices

When compiling for a HardCopy IV GX device with a Stratix IV GX FPGA device as a companion device, some pins that are supposed to be shown as VREF and GND are shown as NC. To get the correct pin-out for PCB layout, compile for the Stratix IV GX FPGA device with the HardCopy IV GX device as a companion device.

**Applies to:** HardCopy IV GX devices

## Migration combinations of devices show fewer VCCIO pins

In certain migration combinations of Arria II GX and Stratix IV GX and E devices, fewer VCCIO pins may be seen as available, when vertical migration in the following paths is enabled:

### Arria II GX devices

EP2AGX95EF35 with EP2AGX190FF35 or EP2AGX260FF35

EP2AGX125EF35 with EP2AGX190FF35 or EP2AGX260FF35

Pins AJ8 and G8 from VCCIO4B (bank 4B) turn to NC when migration is on in these combinations.

### Stratix IV E devices

EP4SE530F43 with EP4SE820F43

Multiple VCCIO pins from banks 1B, 1C, 2B, 2C, 3C, 4C, 5B, 5C, 6B, 6C, 7C, 8C turn to NC, when migration is on.

**Stratix IV GX devices**

EP4SGX110FF35 with EP4SGX180FF35, EP4SGX230FF35, EP4SGX290FF35, EP4SGX360FF35, or HC4GX25LF1152 (HardCopy IV)

Multiple VCCIO pins from banks 1A, 1C, 3C, 4C, 6A, 6C, 7C, 8C turn to NC, when migration is on.

**Applies to:** Arria II GX and Stratix IV GX and E devices

**No vertical migration for Engineering Sample Stratix IV 230 GX and E and 530 GX and E**

Stratix IV 230 GX and E and 530 GX and E devices in Engineering Sample version are not allowed for vertical migration with the production devices due to the voltage changes. (Core voltage for ES devices is 0.95V, while core voltage for production devices is 0.9V.). To access vertical migration, use the corresponding production device in the design.

**Applies to:** Stratix IV devices

**Incorrect programming for EPCS devices in Quartus II 9.0 and 9.0 SP1 fixed in 9.0 SP2**

When a JAM File (.jam) for Serial Flash Loader is created with an unused address range, the Serial Flash Loader may incorrectly program the EPCS configuration device. This issue affects the Quartus II software versions 9.0 and 9.0 SP1, and is fixed in the Quartus II software versions 9.0 SP2 and 9.1.

**Applies to:** EPCS devices

**Cyclone III Maximum Clock Rate updated**

The maximum clock rate for DDR2 memory interfaces with Wraparound mode for the -6 speed grade has been updated from 150 to 167 MHz.

**Applies to:** Cyclone III devices

**Stratix IV timing model updated**

The Stratix IV EP4SE530 and EP4SGX530 device timing models for the C2 speed grade are updated in the Quartus II software versions 9.0 SP2 and 9.1. The timing reported by the Quartus II software version 9.0 SP1 was 5% faster than the correct timing specification.

**Applies to:** Stratix IV devices

**Power down settings ignored**

The **VCCHIP\_R power** and **VCCHIP\_L power** options are not supported in the Quartus II software versions 9.0 SP1, 9.0 SP2, and 9.1. The **Opportunistically power off** setting is not available; the **Power on** setting will be used instead.

**Applies to:** Stratix IV GX and Stratix IV GT devices