



DSP Builder

Release Notes and Errata



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This chapter describes new features, revision history, known errata and documentation changes for the DSP Builder standard blockset.

Revision History

Table 1–1 lists the revision history for the DSP Builder standard blockset v9.1, v9.0, and v8.1.

Table 1–1. DSP Builder Standard Blockset Revision History

Version	Date	Revision
9.1	November 2009	<ul style="list-style-type: none"> ■ Maintenance release.
9.0 SP1	May 2009	<ul style="list-style-type: none"> ■ Maintenance release.
9.0	March 2009	<ul style="list-style-type: none"> ■ Support for Linux operating systems. ■ Support for Arria® II GX.
8.1	November 2008	<ul style="list-style-type: none"> ■ Removed obsolete <i>Simulation Accelerator</i> block and deprecated support for the Video and Image Processing Suite. ■ Updated Hardware in the loop (HIL) block user interface.

Errata

Errata are functional defects or errors which may cause DSP Builder to deviate from published specifications. Table 1–2 shows the errata that affect the DSP Builder standard blockset v9.1, v9.0, and v8.1.



For the latest errata information, refer to the *DSP Builder Release Notes and Errata* on the Altera literature website.

Table 1–2. DSP Builder Standard Blockset Errata (Part 1 of 2)

Added or Updated	Issue	Affected Version			
		9.1	9.0 SP1	9.0	8.1
15 Nov 09	Reset Signal Inverted if <i>_n</i> Appended to Signal Name	Fixed	✓	✓	✓
15 Jun 09	DSP Block Naming Issue in Software Version 8.1	—	—	Fixed	✓
15 May 09	Incorrect Pin Assignments <i>Test2S60Board.mdl</i> Design Example	—	Fixed	✓	—
01 Apr 09	MATLAB Runs Out of Java Virtual Machine Heap Memory	✓	✓	✓	✓
15 Mar 09	VCD Sink Block Does Not Generate HDL Files on Linux	✓	✓	✓	—
	Errors Issued With Imported Quartus II Project	—	—	Fixed	✓
	Cannot Compare Simulink Against ModelSim When Using VIP Suite IP	—	—	—	✓
01 Nov 08	MATLAB Hangs If You Press Enter in Signal Compiler Device Box	✓	✓	✓	✓

Table 1-2. DSP Builder Standard Blockset Errata (Part 2 of 2)

Added or Updated	Issue	Affected Version			
		9.1	9.0 SP1	9.0	8.1
15 May 08	Additional Project Assignments Required for User Libraries	✓	✓	✓	✓
01 May 07	Dual-Clock FIFO Simulation Does Not Match ModelSim	✓	✓	✓	✓

Reset Signal Inverted if `_n` Appended to Signal Name

The reset signal is inverted if `_n` is appended to the signal name specified in the `Clock` or `Clock_Derived` block.

Affected Configurations

Designs which include a `Clock` or `Clock_Derived` block.

Design Impact

The inverted reset signal is propagated through the design.

Workaround

Do not append `_n` to the reset signal specified in a `Clock` or `Clock_Derived` block unless you explicitly want the signal to be inverted. Note that you can append `_N` (uppercase) without inverting the reset signal.

Solution Status

This issue is fixed in DSP Builder v9.1.

DSP Block Naming Issue in Software Version 8.1

The `Stratix III DSP` block was renamed to `DSP` block in the v8.0 software because it also supports Stratix IV devices. A forwarding table in the library model ensured that any blocks named `Stratix III DSP` block upgraded from the previous release was recognized as a `DSP` block in the v8.0 software.

The name of the block incorrectly reverted to `Stratix III DSP` in the v8.1 software.

Affected Configurations

Designs upgraded from v8.0 that use the `DSP` block.

Design Impact

A `DSP` block in a design upgraded from v8.0 is not recognized in the v8.1 software.

Workaround

If you upgrade to v9.0, any blocks named `DSP` or `Stratix III DSP` are recognized as `DSP` blocks.

Alternatively, you can edit the `<install directory>\quartus\dsp_builder\bin\mdllibrary\allblocks_alteradspbuilder2.mdl` file in the v8.1 software and add the following reverse forwarding table string:

```
ForwardingTableString "|__slOldName__|allblocks_alteradspbuilder2/DSP  
Block|__slNewName__|allblocks_alteradspbuilder2/Stratix III DSP Block"
```

Solution Status

This issue is fixed in DSP Builder v9.0.

Incorrect Pin Assignments Test2S60Board.mdl Design Example

The pin assignments for the PLL output clock resets are incorrect in the design example Test2S60Board.mdl.

Affected Configurations

Design example Test2S60Board.mdl.

Design Impact

Errors are issued reporting invalid pin assignments when you run the Quartus II Fitter from the Signal Compiler block.

Workaround

Perform the following steps to correct the pin assignments.

1. In MATLAB, navigate to the directory *<install directory>\quartus\dsp_builder\DesignExamples\Demos\Board\StratixII_DSPBoard_2S60* and open the model Test2S60Board.mdl.
2. Double-click on the Quartus II assignments block to open the subsystem window.
3. Double-click on the Quartus II Pinout Assignments1 block to open the **Block Parameters** dialog box for PLL clock reset out. Change the pin location assignments to Pin_AD32, Pin_AB30, Pin_M30, Pin_N29. Click **OK** to apply and save the changes.
4. Save the model.
5. Use the normal procedures to compile and download the design to the board, and run SignalTap II Analysis on the design.

Solution Status

This issue is fixed in v9.0 SP1 of DSP Builder.

MATLAB Runs Out of Java Virtual Machine Heap Memory

For a very large design, MATLAB may have insufficient heap memory available for the Java virtual machine.

Affected Configurations

Very large designs containing many thousand blocks.

Design Impact

Compilation fails and MATLAB issues an error message of the form:

```
"OutOfMemoryError: Java heap space"
```

Workaround

Increase the heap space available to the Java virtual machine. For more information, refer to:

<http://www.mathworks.com/support/solutions/data/1-18I2C.html>

Solution Status

This issue will be documented in a future release of DSP Builder.

VCD Sink Block Does Not Generate HDL Files on Linux

The VCD Sink block does not generate HDL files on Linux systems.

Affected Configurations

Linux configurations.

Design Impact

No HDL is generated for the VCD Sink block.

Workaround

None.

Solution Status

This issue will be fixed in a future release of DSP Builder.

Errors Issued With Imported Quartus II Project

HDL Import blocks that import Quartus II projects may cause errors while executing the Signal Compiler or TestBench flows.

Affected Configurations

Models with HDL Import blocks that reference Quartus II projects with SEARCH_PATH assignments, rather than USER_LIBRARIES assignments.

Design Impact

Models containing HDL Import blocks that import Quartus II projects generated using Quartus II v8.0 may fail to generate hardware because the library settings are not recognized.

Workaround

Add a USER_LIBRARIES setting to the .qsf file for the Quartus II project to be imported. The assignment value should be the concatenation of all the project's SEARCH_PATH assignment values, separated by semi-colons and enclosed within quotes. These required search path values may be in the top-level .qsf file, or in .qip files included in the project. Then recompile the HDL Import block.

Solution Status

This issue is fixed in v9.0 of DSP Builder.

Cannot Compare Simulink Against ModelSim When Using VIP Suite IP

Execution of the **Compare against HDL** or **Generate HDL** steps in the **Testbench Generator** dialog box issues an error for Video and Image Processing Suite MegaCore functions.

Affected Configurations

Designs using Video and Image Processing Suite MegaCore function blocks.

Design Impact

Testbench generation does not complete successfully, and automatic comparison of the Simulink simulation results against the results from ModelSim® is not possible.

Workaround

A MATLAB m-script is provided that give access to the testbench flow, with the flow output being sent to the MATLAB command window. The command required to use this script is:

```
alt_dspbuilder_compare_VIP_design_against_HDL(<model>, <performcompare>)
```

where:

- *<model>* is the name of the .mdl file for which the flow is to be run.
- *<performcompare>* is optional, setting it to 0 causes the final Compare Results step to be skipped. The default value of 1 causes the Compare Results step to be run.

After the script is run, you can use the features available in the **Advanced** tab of the **Testbench Generator** dialog box (excluding the **Generate HDL** step).

Solution Status

The Video and Image Processing Suite MegaCore functions are not supported in DSP Builder v9.0 or later.

MATLAB Hangs If You Press Enter in Signal Compiler Device Box

MATLAB hangs if you press the Enter or Return key in the **Device** box on the **Signal Compiler** dialog box.

Affected Configurations

All configurations.

Design Impact

None.

Workaround

Take care to avoid pressing the Enter or Return key after typing the device name.

Solution Status

This issue will be fixed in a future release of DSP Builder.

Additional Project Assignments Required for User Libraries

Additional project assignments may be required when using the Export HDL flow with user libraries.

Affected Configurations

Configurations that include MegaCore function, HDL Import, or State Machine Editor blocks.

Design Impact

Compilation fails in the Quartus II software with an error of the form:

```
Error: Node instance <block_name> instantiates undefined entity
<entity_name>
```

Workaround

Add the following to the Quartus II project:

- The `.qip` file corresponding to the entity named in the error message. (This file is located in the `import` subdirectory corresponding to the library model.)
- In some cases you may also need to add any libraries which are referenced by HDL `Import` block(s) in the library model.

Solution Status

This issue will be fixed in a future release of DSP Builder.

Dual-Clock FIFO Simulation Does Not Match ModelSim

The `Dual-Clock FIFO` simulation in Simulink is functionally equivalent to hardware, but not cycle-accurate.

Affected Configurations

Most configurations are affected.

Design Impact

The delay between the write-side adding data and the read-side seeing it, and between the read-side clearing space in the FIFO and the write-side seeing it, does not match hardware.

Workaround

Do not rely on these timing characteristics for correctness of a design.

Solution Status

This issue will be fixed in a future release of DSP Builder.

This chapter describes new features, revision history, known errata and documentation changes for the DSP Builder advanced blockset.

Revision History

Table 2–1 lists the revision history for the DSP Builder advanced blockset v9.1, v9.0, and v8.1.

Table 2–1. DSP Builder Advanced Blockset Revision History

Version	Date	Revision
9.1	November 2009	<ul style="list-style-type: none"> ■ Primitive block support for: <ul style="list-style-type: none"> ▪ Folding (time-division multiplexing) ▪ Simulink Complex type support in arithmetic and memory primitive blocks ■ Simulink 1-D vector (array) support in arithmetic and memory primitive blocks ■ Improved resource utilization ■ Run ModelSim system-level testbench now verifies ModelSim simulation against Simulink, and there are no longer restrictions on the stimulus blocks supported ■ Primitive block changes: <ul style="list-style-type: none"> ▪ Convert block now has a saturation option ▪ Mux2 is now generalized to an arbitrary number of inputs (and renamed Mux)
9.0 SP1	May 2009	Maintenance release.
9.0	March 2009	<p>Support for Linux operating systems.</p> <p>Support for Arria® II GX.</p> <p>Updated SOPC Builder support and procedures for instantiating a design.</p> <p>Support for running all the automatic testbenches in a design.</p> <p>Improved documentation for the NCO block including multichannel design examples with support for multiple banks.</p>
8.1	November 2008	<p>New W-CDMA example designs.</p> <p>Latency display option on ModelIP blocks.</p> <p>DONT_CARE option on Dual Memory block.</p> <p>Diagrammatic channelization format display for ModelIP blocks.</p> <p>Quartus II IP (.qip) file support.</p> <p>Latency constraints can be applied using the SynthesisInfo block.</p>

Errata

Errata are functional defects or errors which may cause DSP Builder to deviate from published specifications. Table 2–2 shows the errata that affect the DSP Builder advanced blockset v9.1, v9.0, and v8.1.


 For the latest errata information, refer to the *DSP Builder Release Notes and Errata* on the Altera literature website.

Table 2-2. DSP Builder Advanced Blockset Errata

Added or Updated	Issue	Affected Version			
		9.1	9.0 SP1	9.0	8.1
15 Nov 09	Simulation Error With Cyclone Series Devices	✓	—	—	—
	DSP Builder Advanced Blockset Reports an Incorrect Version Number	✓	—	—	—
	Primitive Latency Constraints Do Not Work	✓	—	—	—
	ATB Generation Does Not Follow Links out of Subsystems	✓	—	—	—
	Incorrect VHDL if Single Simulink Inport Block is Connected to Multiple ChannelIn Ports	✓	—	—	—
	Bad Port Indexing for Complex Data on ChannelOut and ChannelIn	✓	—	—	—
	Driving Simulink Scopes With Complex Signals Gives Errors	✓	—	—	—
	No Support for 1-Input Mode	✓	—	—	—
	DSP Builder Advanced User Guide has No Revision History for v9.1	✓	—	—	—
	Imaginary Output from Complex to Real Imaginary Gives Internal Errors	✓	—	—	—
	Hardware Tcl Files Do Not Have Correct Port Names for Vector Ports	Fixed	✓	✓	—
15 May 09	Multiplier Optimizations Can Cause Signal Width Mismatch in Synthesis	✓	✓	—	—
	HIL Simulation of Combined Blockset Design Outputs All Zeros	—	Fixed	✓	—
01 Apr 09	Latency Not Balanced for ModelBus blocks Outside Primitive Subsystem	✓	✓	✓	—
15 Mar 09	Bus and System Clocks Must Match When Using Bus Stimulus Block	✓	✓	✓	✓
	Primitive Automatic Testbench Flow Incorrect with Many Integer Bits	—	—	Fixed	✓
	Limit of 50 Subsystem Ports Anywhere in a Design	—	—	Fixed	✓
01 Nov 08	Saturation Limitation When using the Scale Block	✓	✓	✓	✓
	Very High Hard Multiplier Threshold Does Not Force the Use of Logic	✓	✓	✓	✓
	No Forward Flow Control in Primitive Subsystems	✓	✓	✓	✓
	Limitations of the ModelSim Testbench Flow	✓	✓	✓	✓
15 May 08	Cannot Import a Combined Blockset Design into SOPC Builder	✓	✓	✓	✓
	Incorrect Simulation Results if Word Length Greater Than 64 bits	✓	✓	✓	✓
	Compilation Error if Unused Channel Out Port is Terminated	✓	✓	✓	✓

Simulation Error With Cyclone Series Devices

Primitive Const blocks that generate a signal driving a Mult-Add block sequence may cause a simulation error when targetting Cyclone series devices.

When you target any of the Cyclone devices, simulation may fail in designs that contain a signal from a primitive Const block that drives a Mult block that drives an Add block.

Affected Configurations

This issue affects configurations that target any Cyclone series devices and contain a primitive Const driving a Mult-Add block sequence.

Design Impact

The following assertion failure occurs, which crashes MATLAB.

```
outputClock != m_model->m_infiniteClock.
```

Workaround

Connect the constant signal to the `Mult` block using a `Convert` block.

Solution Status

This issue will be fixed in a future release of the DSP Builder advanced blockset.

DSP Builder Advanced Blockset Reports an Incorrect Version Number

DSP Builder Advanced Blockset reports an incorrect version number.

Affected Configurations

This issue affects all configurations.

Design Impact

The version number reported by DSP Builder Advanced Blockset within MATLAB (for example, through the `ver` MATLAB command) is 0.0.0. This incorrect version number also appears in the header comment of generated HDL files.

Workaround

Ignore the incorrect version numbers.

Solution Status

This issue will be fixed in a future release of the DSP Builder advanced blockset.

Primitive Latency Constraints Do Not Work

In primitive subsystems an option on the `SynthesisInfo` block should allow you to set a latency constraint for the subsystem. However this feature does not work.

Affected Configurations

This issue affects all configurations.

Design Impact

There is no design impact.

Workaround

This issue has no workaround.

Solution Status

This issue will be fixed in a future release of the DSP Builder advanced blockset.

ATB Generation Does Not Follow Links out of Subsystems

Synthesizable subsystems where Simulink Inports are directly connected to Simulink Outports may lead to ATB VHDL errors.

Affected Configurations

Synthesizable subsystems where a Simulink Inport block feeds directly into a Simulink Outport block.

Design Impact

When you use the generated ATB (for example by double-clicking **Run ModelSim**), you receive the following error, because the ATB is trying to read simulation data from a file that does not exist:

```
# ** Error: (vsim-7) Failed to open VHDL file
"../MATLAB/./rtl/device_atb_problem/DUT/Wire/Out1_auto.stm" in rb
mode.
```

Workaround

To workaroud the issue, replace direct connections from a Simulink Inport block to a Simulink Outport block with direct connections outside the corresponding subsystem.

Solution Status

This issue will be fixed in a future release of the DSP Builder advanced blockset.

Incorrect VHDL if Single Simulink Inport Block is Connected to Multiple ChannelIn Ports

Connecting single Simulink Inport block to multiple ChannelIn ports may lead to VHDL error in synthesis.

Affected Configurations

This issue affects primitive subsystems where a Simulink Inport block feeds into multiple ChannelIn ports

Design Impact

When you compile for synthesis in the Quartus II software, you receive the following error, because the same port name appears multiple times in the port list:

```
Error (10465): VHDL error at
one_inport_to_many_channelin_ports_Chip.vhd(40): name "d0" cannot be
used because it is already used for a previously declared item
```

Workaround

Add a Simulink Inport block for each ChannelIn input in your subsystem, and feed the desired signals to those ports outside the subsystem.

Solution Status

This issue will be fixed in a future release of the DSP Builder advanced blockset.

Bad Port Indexing for Complex Data on ChannelOut and ChannelIn

You should always connect the channel (DC) input port of the ChannelOut ModelPrim block, if your design uses complex data types. If your design does not have the DC input port connected, as it is not required, you should drive it with a constant zero `uint(8)`.

Similarly, you should always connect the channel (DC) input port of the ChannelIn ModelPrim block, if your design uses complex data types. If your design does not have the DC input port connected, as it is not required, you should connect it up through the subsystem levels and drive it with a constant zero `uint(8)` in the testbench.

Affected Configurations

This issue affects all configurations.

Design Impact

Without these imaginary components any complex data signals through the channel out may not be correctly connected, and the imaginary component are lost. In addition for the ChannelIn ModelPrim block, if completely unconnected a port ChannelIn_2 is created on the entity, but not on the components.

Workaround

This issue has no workaround.

Solution Status

This issue will be fixed in a future release of the DSP Builder advanced blockset.

Driving Simulink Scopes With Complex Signals Gives Errors

You cannot drive Simulink scopes with complex signals. They only accept real signals (including real vectors). If you attempt to drive a scope with a complex signal in your design, Simulink assume this signal should be real and back-propagates the real type through the design, until such time as there is a clash, where a block is explicitly driven by a complex type.

Affected Configurations

This issue affects all configurations.

Design Impact


This clash results in the following error message:

```
"Attempted to set output port (n) complexity after it was already set to opposite sense."
```

If you see this error for a complex port, check that the signal downstream is not driving a scope directly.

Workaround

Add a Simulink Complex to Real-Imag block (Simulink > Math Operations library) and connect the real and imaginary components to the scope individually.

 Blocks other than Simulink scopes may also cause similar errors, if they only accept real data types. The same workaround applies.

Solution Status

This issue will be fixed in a future release of the DSP Builder advanced blockset.

No Support for 1-Input Mode

There is no support for 1-input mode on AND, OR, or other logical ModelPrim blocks.

Affected Configurations

This issue affects all configurations.

Design Impact

You see the following error:

```
Altera DSP Builder Advanced Internal Restriction: 'in[i].m_inWidth
<= WIDE_MAX_DATAWIDTH'. Error in block
'rrh_duc/device/DUC/carrier_duc/CarrierEnableGainSum/Or_rsrvd_fix'
in .\hw_fu.cpp:1221. .
```

Workaround

This issue has no workaround.

Solution Status

This issue will be fixed in a future release of the DSP Builder advanced blockset.

DSP Builder Advanced User Guide has No Revision History for v9.1

The DSP Builder Advanced User Guide has no revision history for v9.1. The following revision history is correct:

- Added appendix on folding
- Added descriptions on complex datatype and vectorization

Solution Status

This issue will be fixed in a future release of the DSP Builder advanced blockset.

Imaginary Output from Complex to Real Imaginary Gives Internal Errors

You cannot use the imaginary output from `Complex to Real-Imag` block, if the input signal is real, (despite this imaginary output signal appearing in Simulink). Attempts to use the imaginary output leads to internal errors. In synthesizable subsystems, you receive an error message; in subsystems not for synthesis, you receive a warning message.

Affected Configurations

This issue affects all configurations.

Design Impact

If you use the imaginary output, DSP Builder issues internal errors.

Workaround

Ensure the source signal is complex or remove the `Complex to Real-Imag` block and generate a constant zero to drive the elements connected to the imaginary signal.

Solution Status

This issue will be fixed in a future release of the DSP Builder advanced blockset.

Hardware Tcl Files Do Not Have Correct Port Names for Vector Ports

If any input ports to the synthesizable system have vector inputs (for example if they feed into a FIR filter with more than one channel and a sample rate matching the clock rate), the `<hardware>_hw.tcl` file generated for SOPC Builder has misnamed ports.

Affected Configurations

Any synthesizable system that has vector input ports.

Design Impact

The port names in the `<hardware>_hw.tcl` file are not vectorized. For example, it might only list an input `a` and an output `q`, although the VHDL actually contains input port names `a0, a1,...` and output port names `q0, q1,...`

Workaround

Manually correct the Tcl file using the generated VHDL as a reference. For example:

```
add_interface_port exp a export Input 17
```

becomes:

```
add_interface_port exp a0 export Input 17
add_interface_port exp a1 export Input 17
add_interface_port exp a2 export Input 17
...
...
```

Solution Status

This issue is fixed in the DSP Builder advanced blockset v9.1.

Multiplier Optimizations Can Cause Signal Width Mismatch in Synthesis

Multiplier optimizations can lead to signal bit width mismatches and VHDL errors in synthesis.

Affected Configurations

Primitive subsystems where a multiplier feeds directly into an output port.

Design Impact

When you compile for synthesis in the Quartus II software, an error is issued of the form:

```
Error: Actual width (34) of port "q1" on instance "<model>:<submod>"
is not compatible with the formal port width (30) declared by the
instantiated entity
```

This is because the output signal is smaller than expected because of a multiplier optimization not being propagated on to a fixed width entity (usually an subsystem boundary or other fixed-width block).

Workaround

Use a `Convert` block from the `ModelPrim` library to explicitly set the required signal format on the output of the multiplier.

Solution Status

This issue will be fixed in a future release of the DSP Builder advanced blockset.

HIL Simulation of Combined Blockset Design Outputs All Zeros

A Hardware in the loop (HIL) design containing blocks from both the standard and advanced blocksets sometimes outputs all zeros when simulated. This problem occurs when the reset type is set to **Low** in the `Signals` block.

The *DSP Design Flow Guide* currently states that an embedded advanced blockset design should have the same reset type as the standard blockset design in which it is embedded. This is incorrect; the advanced blockset design must always have an active high reset.

Affected Configurations

HIL designs derived from a model created using the advanced blockset.

Design Impact


The HIL simulation output remains zero.

Workaround

Change the reset type specified in the `Signals` block to **High** by performing the following steps:

1. In the original combined blockset design, set the **Reset** name to `aclr` and **Reset active** to **High** in the `Signals` block.
2. Delete all the generated files from the `rtl` directory specified as the **Hardware destination directory** in the `Control` block.
3. Delete all the files from the `DSPBuilder_<top level>_import` directory.
4. Delete all the files from `<top level>_dspbuilder` directory.
5. Run Simulink simulation (to generate HDL for the advanced blockset).
6. Compile the design in the `Signal Compiler` block (generate HDL and create a Quartus II project for the whole design).

7. Open the HIL model and run the normal HIL flow.

 The reset level specified in the Clock block is not relevant.

Solution Status

This issue is fixed in the latest version of the *DSP Design Flow Guide*.

Latency Not Balanced for ModelBus blocks Outside Primitive Subsystem

If you are using ModelBus blocks outside of a primitive subsystem with **Scheduled** synthesis style, it is likely that the latencies on the address, write enable and data paths created for these blocks may not be balanced in v9.0.

Affected Configurations

Configurations using ModelBus blocks outside of a primitive subsystem with **Scheduled** synthesis style. ModelBus blocks inside a scheduled subsystem are not affected.

Design Impact

The latencies on the address, write enable and data paths created for ModelBus blocks outside of a primitive subsystem may not be balanced.

Workaround

To ensure the data path is registered in line with the address and write enable for such unscheduled blocks, define the following workspace variable before performing simulation and HDL generation (for example in the model **InitFnc** callbacks):

```
DSPBA_Features.useScheduledDataBus = false;
```

The default v9.0 behavior can be restored by setting this variable to `true`.

Solution Status

This issue will be fixed in a future release of the DSP Builder advanced blockset.

Bus and System Clocks Must Match When Using Bus Stimulus Block

Testbench simulation results are incorrect when using the `Bus Stimulus` block if the bus clock frequency is different from the frequency of the system clock.

Affected Configurations

Any design that uses the `Bus Stimulus` block.

Design Impact

The testbench simulation results are incorrect.

Workaround

The bus clock frequency must be the same as the frequency of the system clock. Turn on **Separate Bus Clock** and **Bus Clock Synchronous with System Clock** in the Signal block for your model.

Solution Status

This issue will be fixed in a future release of the DSP Builder advanced blockset.

Primitive Automatic Testbench Flow Incorrect with Many Integer Bits

The primitive automatic testbench flow may be incorrect when using fractional representations with many integer bits.

Affected Configurations

Designs that require a large number of integer bits.

Design Impact

Unexpected simulation mismatches are reported.

Workaround

Reduce the number of integer bits required by your model.

Solution Status

This issue is fixed in v9.0 of the DSP Builder advanced blockset.

Limit of 50 Subsystem Ports Anywhere in a Design

All blocks that become functional units are restricted to a maximum of 50 ports.

Affected Configurations

Any block or subsystem that has more than 50 ports.

Design Impact

An assert `m_inCount <= m_maxInCount` which crashes MATLAB.

Workaround

Avoid creating a subsystem or block with more than 50 ports.

Solution Status

This issue is fixed in v9.0 of the DSP Builder advanced blockset.

Saturation Limitation When using the Scale Block

When you increase the number of fractional bits used for a signal, the MSB may be truncated.

Affected Configurations

Configurations using the `Scale` block.

Design Impact

The MSB may be truncated.

Workaround

Use a `Convert` block inside the primitive subsystem.

Solution Status

This issue will be fixed in a future release of the DSP Builder advanced blockset.

Very High Hard Multiplier Threshold Does Not Force the Use of Logic

Setting a very high Hard Multiplier Threshold should avoid using any DSP blocks.

Affected Configurations

All configurations.

Design Impact

Unwanted use of DSP blocks.

Workaround

None.

Solution Status

This issue will be fixed in a future release of the DSP Builder advanced blockset.

No Forward Flow Control in Primitive Subsystems

'Bursty' input data is not supported for primitive subsystems, that is designs where the `valid` signal toggles high and low repeatedly.

Affected Configurations

Any primitive subsystem.

Design Impact

The simulation results are incorrect.

Workaround

Avoid using bursts of data.

Solution Status

This issue will be fixed in a future release of the DSP Builder advanced blockset.

Limitations of the ModelSim Testbench Flow

The `Run ModelSim` block can be used to simulate a model in ModelSim. This flow attempts to make a ModelSim testbench by synthesizing all the block (including any Simulink blocks in the top-level). However only a limited number of Simulink blocks are synthesizable and an empty subsystem is created for the unsupported blocks.

Affected Configurations

Any model with unsynthesizable Simulink blocks in the top-level.

Design Impact

The testbench cannot be simulated.

Workaround

Use only the supported blocks in the testbench for your design or write your own HDL for the empty subsystems. (A full list of synthesizable blocks is given in the description of the Run ModelSim block.) Alternatively, you can use the automatic testbench flow to simulate each subsystem in your design separately.

Solution Status

This issue will be fixed in a future release of the DSP Builder advanced blockset.

Cannot Import a Combined Blockset Design into SOPC Builder

You cannot import a design that combines blocks from the standard and advanced blocksets into SOPC Builder.

Affected Configurations

Configurations which combine blocks from the standard and advanced blocksets.

Design Impact

If you attempt to import a combined blockset design into SOPC Builder, warning are issued stating that there are multiple clocks with the same name and the component is not added to the system.

Workaround

There is no workaround.

Solution Status

This issue will be fixed in a future release of the DSP Builder advanced blockset.

Incorrect Simulation Results if Word Length Greater Than 64 bits

The simulation results are incorrect for ModelIP blocks if the word length is greater than 64 bits.

Affected Configurations

Configurations which include ModelIP blocks are affected. However, ModelPrim blocks do support word lengths greater than 64 bits.

Design Impact

The simulation results are incorrect.

Workaround

Restrict the word length used by ModelIP blocks to 64 bits.

Solution Status

This issue will be fixed in a future release of the DSP Builder advanced blockset.

Compilation Error if Unused Channel Out Port is Terminated

Quartus II compilation fails if an unused channel or valid signal from a Channel Out block is connected to a Simulink Terminator block inside a primitive subsystem.

Affected Configurations

Primitive subsystems with unused channel or valid output signals.

Design Impact

Incorrect HDL is generated and errors are issued when you attempt to compile the design in the Quartus II software.

Workaround

Leave the unused signals unconnected or terminate them outside the subsystem.

Solution Status

This issue will be fixed in a future release of the DSP Builder advanced blockset.

Update Status

The following table displays the update status for these release notes.

Date	Version	Changes Made
15 November 2009	9.1	Updated for software version 9.1.
15 June 2009	4.3	Added an errata in the standard blockset chapter.
May 2009	4.2	Updated for software version 9.0 SP1.
April 2009	4.1	Added and updated errata in the advanced blockset chapter.
March 2009	4.0	Updated for software version 9.0.

How to Contact Altera

For the most up-to-date information about Altera® products, refer to the following table.

Contact 1	Contact Method	Address
Technical support	Website	www.altera.com/support
Technical training	Website	www.altera.com/training
	Email	custrain@altera.com
Product literature	Website	www.altera.com/literature
Non-technical support (General) (Software Licensing)	Email	nacomp@altera.com
	Email	authorization@altera.com






Note to table:

(1) You can also contact your local Altera sales office or sales representative.

Typographic Conventions

This document uses the typographic conventions shown in the following table.

Visual Cue	Meaning
Bold Type with Initial Capital Letters	Indicates command names, dialog box titles, dialog box options, and other GUI labels. For example, Save As dialog box.
bold type	Indicates directory names, project names, disk drive names, file names, file name extensions, and software utility names. For example, \qdesigns directory, d: drive, and chiptrip.gdf file.
<i>Italic Type with Initial Capital Letters</i>	Indicates document titles. For example: <i>AN 519: Stratix IV Design Guidelines.</i>
<i>Italic type</i>	Indicates variables. For example, $n + 1$. Variable names are enclosed in angle brackets (<>). For example, <file name> and <project name>.pof file.

Visual Cue	Meaning
Initial Capital Letters	Indicates keyboard keys and menu names. For example, Delete key and the Options menu.
"Subheading Title"	Quotation marks indicate references to sections within a document and titles of Quartus II Help topics. For example, "Typographic Conventions."
Courier type	Indicates signal, port, register, bit, block, and primitive names. For example, <code>data1</code> , <code>t_{di}</code> , and <code>input_n</code> . Active-low signals are denoted by suffix <code>n</code> . Example: <code>reset_n</code> . Indicates command line commands and anything that must be typed exactly as it appears. For example, <code>c:\qdesigns\tutorial\chiptrip.gdf</code> . Also indicates sections of an actual file, such as a Report File, references to parts of files (for example, the AHDL keyword <code>SUBDESIGN</code>), and logic function names (for example, <code>TRI</code>).
1., 2., 3., and a., b., c., and so on.	Numbered steps indicate a list of items when the sequence of the items is important, such as the steps listed in a procedure.
■ ■	Bullets indicate a list of items when the sequence of the items is not important.
	The hand points to information that requires special attention.
	A caution calls attention to a condition or possible situation that can damage or destroy the product or your work.
	A warning calls attention to a condition or possible situation that can cause you injury.
	The angled arrow instructs you to press the enter key.
	The feet direct you to more information about a particular topic.