

These release notes for the POS-PHY Level 4 MegaCore® function v7.1 SP1 contain the following information:

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System Requirements

The POS-PHY Level 4 MegaCore function has the same system requirements as the Quartus® II software.

When migrating from the Quartus II software v7.1 to v7.1 SP1, Altera recommends that you regenerate any existing MegaCore function variations and SOPC Builder systems in development to ensure that they use the latest version of each core. Quartus II recompilation of the existing project is not sufficient to update the core version.



For system requirements and installation instructions, refer to *Quartus II Installation & Licensing for Windows* or *Quartus II Installation & Licensing for UNIX & Linux Workstations*.

New Features & Enhancements

The following list outlines new features and enhancements in this release:

- Maintenance release

Errata Fixed in This Release



The “Recovery Violation in ALTLVDS_RX Megafunction” errata was fixed in this release.

For existing up-to-date errata, refer to the *POS-PHY Level 4 MegaCore Function v7.1 SP1 Errata Sheet* on the errata page on the Altera website at www.altera.com/literature/es/es_posphy4_71.pdf

Contact Altera

For the most up-to-date information about Altera products, see [Table 1](#).

Table 1. Contact Information	
Information Type	Contact <i>Note (1)</i>
Technical support	www.altera.com/mysupport/
Technical training	www.altera.com/training/
Technical training services	custrain@altera.com
Product literature	www.altera.com/literature
Product literature services	literature@altera.com
FTP site	ftp.altera.com

Note to Table 1:

(1) You can also contact your local Altera sales office or sales representative.

Revision History

[Table 2](#) shows the revision history for the POS-PHY Level 4 MegaCore function.

Table 2. POS-PHY Level 4 MegaCore Function Revision History (Part 1 of 2)		
Version	Date	Revision
7.1 SP1	June 2007	See “New Features & Enhancements” on page 1
7.1	May 2007	<ul style="list-style-type: none"> ● Full support for HardCopy® II devices ● Preliminary support for Arria™ GX devices ● Low speed LVDS I/O support ● Maximum burst size support in transmitter ● Removed unused almost empty and almost full ports ● Update to receiver external status override ● Improvements for Cyclone®, Cyclone II, and Cyclone III devices: wider internal bus and LVDS support up to 622 Mbps
7.0	December 2006	Preliminary support for Cyclone III devices.
6.1	December 2006	<ul style="list-style-type: none"> ● Preliminary support for Stratix® III devices ● Added new status bypass port information ● Added FIFO RAM blocks option
2.4.1	April 2006	Maintenance release.
2.4.0	October 2005	<ul style="list-style-type: none"> ● Preliminary support for Stratix II GX devices ● Preliminary support for HardCopy® II devices ● Updated the reset structure ● Added the <code>stat_rx_pll_locked</code> or <code>stat_tx_pll_locked</code> signals ● Added the <code>ctl_rx_pll_areset</code> or <code>ctl_tx_pll_areset</code> signals ● Instantiates an ALTDDIO megafunction on all status interfaces to reduce on-chip skew

Table 2. POS-PHY Level 4 MegaCore Function Revision History (Part 2 of 2)

Version	Date	Revision
2.3.1	April 2005	<ul style="list-style-type: none"> ● ALTLVDS instances can be edited with the ALTLVDS megafunction wizard ● Relaxed restrictions on calendar length and calendar multiplier
2.3.0	February 2005	<ul style="list-style-type: none"> ● Cyclone II device family support at up to 250 Mbps ● Asymmetric ports and hitless bandwidth reprovisioning ● Re-architected clock-domain crossing and Atlantic™ alignment blocks, significantly reducing the logic consumption for 64- and 128-bit receiver variations ● Option to select single or multiple clock domain Atlantic buffering ● Optional Atlantic interface width ● Optional parity protection across Atlantic first-in first-out (FIFO) buffer memories



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