



# Quartus II Software Release Notes

December 2006

Quartus II software version 6.1

This document provides late-breaking information about the following areas of this version of the Altera® Quartus® II software. For information about memory, disk space, and system requirements, refer to the **readme.txt** file in your `\altera\<version number> \quartus` directory. For information about device support in this version of the Quartus II software, along with the latest information about timing and power models, refer to the *Quartus II Device Support Release Notes* on the Altera website at <http://www.altera.com/literature/lit-qts.jsp>.

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# New Features & Enhancements

The Quartus II software version 6.1 includes the following new features and enhancements:

- Advanced support for the Stratix III device family.
- The Chip Planner, an integrated floorplan editor and Chip Editor that provides a visual display of chip resources.
- The Tutorial, a new Flash-based Quartus II interactive tutorial that you can access from the Help menu.
- Advanced I/O Timing, which allows you to specify the board trace and any resistive or capacitive termination connected to each of the FPGA outputs.
- Multiprocessor support, which allows parallel processing during compilation for computers with multiple processors and results in a reduction in compilation times.
- Programmable Power Technology for Stratix III devices.
- Pin Planner enhancements to allow you to specify board trace model assignments.
- Detachable windows support.
- Windows 64-bit version.
- SUSE Linux Enterprise Server 9 in addition to Red Hat Enterprise Linux 3.0 and 4.0.
- Full device support for Cyclone II devices: EP2C8AF256, EP2C15AF256, EP2C15AF484, EP2C20AF256, and EP2C20AF484.
- Full device support for HardCopy II devices: HC210F484, HC240F1020, and HC240F1508.
- Full device support for MAX II devices: EPM240GF100, EPM240GM100, EPM570GF100, EPM570GM100, EPM570GM256, and EPM1270GM256.
- Full device support for Stratix II GX devices: EP2SGX30CF780, EP2SGX30DF780, EP2SGX60CF780, EP2SGX60DF780, EP2SGX60EF1152, and EP2SGX130GF1508.

## EDA Interface Information

The current version of the Quartus II software supports the following EDA tools.

### Supported EDA Tools

Synthesis Tools	Version	NativeLink Support
Synplicity Synplify & Synplify Pro	8.8	✓
Mentor Graphics Precision RTL Synthesis	2006a	✓
Mentor Graphics LeonardoSpectrum	2006a	✓
Synopsys Design Compiler FPGA	2005.09	
Synopsys FPGA Compiler II	3.8	✓
Synopsys Design Compiler	2004.12-SP4	
Magma Design Automation PALACE	2.4	✓
Simulation Tools	Version	NativeLink Support
Mentor Graphics ModelSim	6.1g	✓
Mentor Graphics ModelSim-Altera	6.1g	✓
Cadence NC-Sim (Windows)	5.4 s011	✓
Cadence NC-Sim (UNIX)	5.82 p001	
Synopsys VCS / VCS MX	2005.06-SP2	✓
Aldec Active-HDL	7.1 SP1	✓
Formal Verification Tools (Equivalence Checking)	Version	NativeLink Support
Cadence Encounter Conformal	6.1 USR1	
Synopsys Formality	2005.09	
Chip Level Static Timing Analysis	Version	NativeLink Support
Synopsys PrimeTime	2006.06	✓
Board Level Static Timing Analysis	Version	NativeLink Support
Mentor Graphics TAU	3.6	
Board Level Symbol/Pin-out Management	Version	NativeLink Support
Mentor Graphics I/O Designer	2005.1	

## Changes to Software Behavior

This section documents instances in which the behavior and default settings of this release of the Quartus II software have been changed from earlier releases of the software.

Items listed in the following table represent cases in which the behavior of the current release of the Quartus II software is different from a previous version.

Description	Workaround
<b>Version 6.1</b>	
<p>A minor change has been made to the power breakdown between I/O power and Core power in the PowerPlay Power Analyzer report. The total power dissipated on the device and the total current drawn from each voltage supply are unaffected. I/O routing power refers to the power dissipated by device core routing resources that are driven by input I/O cells. In Quartus II software versions 6.0 and 6.0 SP1, I/O routing power was reported on the PowerPlay Power Analyzer Summary report section as I/O power rather than core dynamic power.</p> <p>For a typical design, the net change is a change of less than 2% of power from I/O Power to Core Dynamic Thermal Power Dissipation in the Summary report section of the PowerPlay Power Analyzer. Also, the Core Dynamic Thermal Power Dissipation by Clock Domain report section did not enumerate the I/O routing power.</p>	
<p>The current version now supports the following Stratix II GX industrial ordering codes:</p> <ul style="list-style-type: none"> <li>EP2SGX90EF1152I4</li> <li>EP2SGX90FF1508I4</li> <li>EP2SGX130GF1508I4</li> <li>EP2SGX60DF780I4</li> <li>EP2SGX60EF1152I4</li> <li>EP2SGX30DF780I4</li> </ul>	

Description	Workaround
<p>Designs that contain a user-edited Memory Initialization File (.mif) that compile successfully earlier versions of the Quartus II software may fail with the error "File &lt;filename&gt;.mif contains illegal syntax at line &lt;num&gt;" in the Quartus II 6.1 software. These Memory Initialization Files contain illegal syntax. Illegal Memory Initialization Files were ignored by previous releases of the software.</p>	<p>Correct the syntax of the Memory Initialization File by referring to the Memory Initialization File syntax description in the Quartus II Help, or create a new Memory Initialization File with the Quartus II software.</p>
<p>In the Quartus II software version 6.1, the tcllib library is updated from 1.7 to 1.8. If you are using advanced Tcl scripting, this change may cause your script to produce unexpected results.</p>	
<p>You may receive the following warnings when you use the write_sdc command in the TimeQuest Timing Analyzer:</p> <p>Warning: Ignored assignment create_generated_clock</p> <p>Warning: Collection filter Positional argument &lt;source_objects&gt; with value [get_nodes Pll_Inst\ altpll_component\ pll \ clk\[0\]] requires type (port pin reg kpr net ), but found type node.</p> <p>You receive these warnings because the create_clock or create_generated_clock assignments are ignored by the TimeQuest Timing Analyzer when using get_nodes collections. This issue is most likely to occur when using a Synopsys Design Constraints File (.sdc) generated from the Quartus II software version 6.0 or 6.0sp1 using the write_sdc command.</p>	<p>Change get_nodes to use one of get_ports, get_pins, get_nets, get_registers, or get_keepers.</p>

Description	Workaround
<p>In the Quartus II software version 6.1, when you simulate designs that use MAX II UFM or any PLL, you might see X's in the initial part of the simulation time instead of 0's. The behavior after the X's are correct.</p> <p>This behavior is the same as in any third party simulators, but different from Quartus II Simulator in versions earlier than Quartus II software version 6.1.</p>	
<p><b>Version 6.0 SP1</b></p>	
<p>In the Quartus II software version 6.0 and earlier, when you created a receiver-only instance of the alt2gxb megafunction, a CMU PLL was created that has pll_inclk and pll_locked ports. These ports prevented the combination of two receiver-only implementations at different data rates in the same quad.</p>	<p>In the Quartus II software version 6.0 SP1, a CMU PLL is no longer created when you create a receiver-only instance. You must recreate the megafunction instance with the <b>MegaWizard Plug-In Manager</b> or manually remove the pll_inclk and pll_locked ports from the wrapper file.</p>
<p>In the Quartus II software version 6.0 SP1 and later, the TimeQuest Timing Analyzer no longer recognizes uppercase pin suffix names in an SDC constraints file.</p>	<p>You must manually change the pin name suffixes to lowercase in your SDC file. For example [get_pins myreg CLK] should be changed to [get_pins myreg clk].</p>
<p><b>Version 6.0</b></p>	
<p>The TimeQuest Timing Analyzer's QSF2SDC conversion utility cannot properly convert all Classic Timing Analyzer timing assignments. The results from the TimeQuest Timing Analyzer may also be different from the Classic Timing Analyzer due to other default behavior differences.</p>	<p>The QSF2SDC conversion utility is considered a guide to help reduce the time to switch to the TimeQuest analyzer, and it is not intended to make the TimeQuest analyzer a plug-in replacement for the Quartus II Classic Timing Analyzer. You should review all converted SDC constraints for correctness and completeness. Refer to the <i>Switching To the TimeQuest Timing Analyzer</i> chapter in the Quartus II Software Handbook for more information.</p>
<p>The Quartus II software version 6.0 does not create a Verilog Quartus Mapping File (.vqm) for any Stratix II GX design that contains any GXB-related blocks.</p>	<p>If a VQM is necessary, partition your design so the GXB-related block is in one partition, then create VQMs for the other portions of the design.</p>

Description	Workaround
The maximum frequency of the GXB – core clock signal for the -5 speed grade of Stratix II GX devices has been lowered from 250 MHz to 200 MHz in this release of the Quartus II software.	If your design requires a GXB – core clock frequency higher than 200 MHz, use a -4 or -3 speed grade device.
For designs that target Stratix II GX devices, that use the alt2gxb megafunction in a transmitter-only configuration, the loop_filter_resistor_control value was not correctly written to the megafunction instance.	Use the MegaWizard Plug-In Manager in the Quartus II software version 6.0 to generate a new instance of the alt2gxb megafunction.
If you created a Verilog Quartus Mapping File (.vqm) for a design containing the alt2gxb megafunction in its XAUI configuration with the Quartus II software version 5.1 SP2 or earlier, the setting for <b>Force Signal Detect</b> was incorrectly set to false.	You should regenerate the alt2gxb instantiation in a XAUI configuration using the Quartus II software version 6.0.
Beginning in the 6.0 release, the Quartus II Parallel Flash Loader megafunction (altparallel_flash_loader) erases flash memory blocks before programming them.	No action is required.
The column names “from” and “to” in the Source Assignments panel of the Analysis & Synthesis section of the Compilation Report have changed to “From” and “To” in this release.	If you are accessing the contents of these columns using a script, you must update your script to reflect the change in capitalization, or use a case-insensitive search.
Beginning in the 6.0 release, Quartus II integrated synthesis handles bidirectional pins differently. For example if bidir1 and bidir2 are declared as inout, the assignment bidir1 <= bidir2 creates a directional connection in which data flows from bidir2 to bidir1. In the Quartus II software version 5.1 and earlier, a bidirectional connection was created.	If your design requires that data flow in both directions, you must directly connect the bidirectional pins together without using an assignment statement. Assignment statements always produce a unidirectional data flow.
In versions of the Quartus II software prior to 6.0, the software incorrectly merged PLLs when they were set to different operating modes.	Beginning in version 6.0, you cannot merge PLLs that are in different operating modes unless you use the <b>Ignore PLL mode when merging PLLs</b> assignment.

Description	Workaround
<p>In versions of the Quartus II software prior to version 6.0, the output clock division factors (<b>outclock_divide_by</b>) were incorrectly reported by a factor of 2, when the altlvds megafunction was implemented in LEs (such as in Cyclone and Cyclone II families).</p>	
<p>The method the Quartus II NativeLink interface uses to locate other EDA tools changed in this release. You might receive a message indicating that the tool cannot be found when you launch it through the NativeLink interface.</p>	<p>You must specify the path to the EDA tool program file on the <b>EDA Tool Options</b> page of the <b>Options</b> dialog box, or with the <code>set_user_command</code> Tcl command.</p>
<p><b>Version 5.1 SP2 and earlier</b></p>	
<p>Beginning with version 5.1, implicit or explicit declarations inside unnamed <code>generate</code> blocks are no longer visible outside the <code>generate</code> block.</p>	<p>Declare the object outside the generate block. You can also add a name to the generate block and refer to the object with a hierarchical name.</p>
<p>The following primitives now use a new library instead of the <b>altera_mf</b> library:</p> <p>CARRY            CARRY_SUM            CASCADE            CLKLOCK            EXP            GLOBAL            LUT_INPUT            LUT_OUTPUT            ROW_GLOBAL            TRI            SOFT            OPNDRN            DFF            DFFE            DFFEAS            JKFF            JKFFE            DFFEAS            LATCH            SRFF            SRFFE            TFF            TFFE            ALT_INBUF            ALT_IOBUF            ALT_OUTBUF            ALT_OUTBUF_TRI</p>	<p>To perform functional simulations in Verilog HDL, you must use the <b>altera_primitives.v</b> library located in the <i>&lt;Quartus II installation directory&gt;\eda\sim_lib</i> directory. For VHDL, you must use the <b>altera_primitives.vhd</b> library located in the <i>&lt;Quartus II installation directory&gt;\eda\sim_lib</i> directory. The VHDL component declaration file is located in the <b>altera_primitives_components.vhd</b> library in the <i>&lt;Quartus II installation directory&gt;\eda\sim_lib</i> directory.</p>

Description	Workaround
The frequency limit on the PLL reference clock on Stratix GX devices changed to 640 MHz.	To take advantage of the new setting, change your design and recompile after installing the Service Pack.
Designs compiled with the Quartus II software version 5.0 and earlier could fail their boundary-scan test (BST) if the test expected all input buffers to be active after device configuration. Under some circumstances, unused input buffers are disabled by the Quartus II software to minimize power usage in Stratix II, Cyclone II, and MAX II device families.	Beginning in version 5.0 Service Pack 1, the Quartus II software supports the <b>always_enable_input_buffers</b> option to prevent unused input buffers from being disabled during configuration.
The Quartus II software version 5.0 and earlier did not correctly enforce the Fitter rule that there must be one row of separation between dynamic phase alignment (DPA) channels to prevent interference.	Beginning in version 5.0 Service Pack 1, the Quartus II software gives a critical warning of this condition if the maximum data rate is between 701 MHz and 1 GHz and an error if the data rate is 1GHz and above. If you receive such warning, reassign your DPA channels to have one row of separation between them.
The <b>data_out[]</b> bus signals from the <code>altremote_update</code> megafunction are incorrectly inverted in the Quartus II software version 5.0. This condition is corrected in version 5.0 SP1.	Recompile your design after installing the Quartus II software version 5.0 Service Pack 1.
The Quartus II software version 5.0 corrects a previous problem in which the Cyclone and Cyclone II CRC configuration oscillator was shown to run at 100 MHz rather than the 80 MHz rate correctly shown in the device family handbooks.	
In the Quartus II software version 5.0 and later, you can assign the <b>Allow XOR Gate Usage</b> logic option to individual nodes and entities. In previous versions, you could apply this logic option only to the entire design (that is, it was a global logic option).	

Description	Workaround
<p>In the Quartus II software versions 5.0, 5.1, 6.0, and 6.1, if your Quartus II Settings File (.qsf) contains an error, you cannot compile the project until the error has been corrected. In previous versions, a warning message was displayed and compilation continued. In the Quartus II software version 6.1, a different error message from previous versions is generated.</p>	
<p>In the Quartus II software version 5.0 and later, the <code>\altera\qdesigns&lt;version number&gt;\ll_makefile</code> directory has been replaced by the <code>\altera\qdesigns&lt;version number&gt;\logiclock_makefile</code> directory.</p>	
<p>The <code>altgxb</code> megafunction has been updated in the Quartus II software version 5.0. Any Stratix GX project that used the <code>altgxb</code> megafunction and was archived with the <b>Include functions from system libraries</b> option turned on will not compile correctly.</p>	<p>You must delete the <b>altgxb.tdf</b> file that is included in the project archive, and recompile your design.</p>
<p>The Quartus II software version 5.0 and later does not support Advanced NativeLink integration with the Synopsys VCS MX software.</p>	
<p>The following megafunctions have clear box models that contain assignments that are not stored in the Quartus Settings File (.qsf) and are not written out to a Verilog Quartus Mapping File (.vqm):</p> <ul style="list-style-type: none"> <li>altdqs</li> <li>altdq</li> <li>altddio_bidir</li> <li>altddio_out</li> <li>altddio_input</li> <li>altlvds_rx</li> <li>altlvds_tx</li> <li>altufm_i2c</li> <li>dcfifo</li> <li>alt2gxb_reconfig</li> </ul>	<p>Do not save your atom netlist file as a Verilog Quartus Mapping file if you are using these megafunctions.</p>

<b>Description</b>	<b>Workaround</b>
When you are using formal verification tools with a design that contains LogicLock regions that was compiled with the Quartus II software version 3.0 or earlier, under certain circumstances when you open the design in the Quartus II software version 4.0 and later, the LogicLock regions will not be handled properly.	Redefine the LogicLock regions in the Quartus II software version 4.0 or later to eliminate the errors.

# Known Issues & Workarounds

## General Quartus II Software Issues

Issue	Workaround
<b>Version 6.1</b>	
When you use the <code>altparallel_flash_loader</code> megafunction in Quartus II software version 6.0 and earlier, the design may not compile successfully.	Regenerate the <code>altparallel_flash_loader</code> megafunction with the current version of the Quartus II software.
In timing simulations of designs that use the QDR II core generated by the Quartus II software versions earlier than 6.1 in Stratix II and Stratix II GX devices, the DQ data can be captured at an incorrect time in comparison to silicon when CQ and CQ# pins toggle under a certain configuration.	The QDR II IP core has added data recapture for the Quartus II software version 6.1, so that designs generated by the Quartus II software versions earlier than 6.1 should not have the issue. For designs generated by Quartus II software versions earlier than 6.1, update the design with the Quartus II software version 6.1 or later and re-compile and simulate the designs.
When adding <code>SDC_FILE</code> to the Quartus II Settings File ( <code>.qsf</code> ), the newly added <code>SDC_FILE</code> is processed last regardless of its placement within the Quartus II Settings File.	Back up the Quartus II Settings File, remove all <code>SDC_FILE</code> assignments from the Quartus II Settings File, and run <b>quartus_sta.exe</b> . Then restore the Quartus II Settings File and rerun <b>quartus_sta.exe</b> .
In Quartus II software version 6.1, designs that have double width deserializer datapath configurations that use the rate matcher and that were created in the Quartus II software versions 6.0 or 6.0 SP1 receive the errors "Error: WYSIWYG primitive "channel_rec[0].receive" has illegal value..."	If you receive these errors, regenerate the <code>alt2gxb</code> megafunction with the MegaWizard Plug-In Manager.
When using <b>Input Maximum Delay</b> ( <code>INPUT_MAX_DELAY</code> ) or <b>Input Minimum Delay</b> ( <code>INPUT_MIN_DELAY</code> ) assignments to constrain I/O pins in the classic timing analyzer, the Fitter will not optimize hold timing for those pins when the <b>Optimize hold timing</b> option in the <b>Fitter Settings</b> page is set to <b>I/O Paths and Minimum TPD Paths</b> .	Change the value of the <b>Optimize hold timing</b> option in the <b>Fitter Settings</b> page to <b>All Paths</b> to optimize hold timing for these pins. This option will also optimize hold timing for core logic.

Issue	Workaround
<p>In the TimeQuest Timing Analyzer, if you have <code>set_max_delay</code> or <code>set_min_delay</code> exceptions for I/O paths as a translation of Classic Timing Analyzer <math>t_{SU}</math> or <math>t_{CO}</math> constraints, then you may encounter poor quality of results from the Fitter, especially if the constraints have negative values.</p>	<p>Instead, use <code>set_input_delay</code> or <code>set_output_delay</code>, even if you are analyzing for <math>t_{SU}</math> or <math>t_{CO}</math>. See the “Switching to the TimeQuest Timing Analyzer” handbook chapter for <math>t_{SU}/t_{CO}</math> conversion details.</p>
<p>You may receive an error if all three of the following conditions are true:</p> <ul style="list-style-type: none"> <li>• You have compiled a Stratix II GX design in a Quartus II software version earlier than 6.1.</li> <li>• The design uses the alt2dprio megafunction.</li> <li>• At least one of the alt2gxb megafunctions fed by the alt2prio megafunction has a logical channel address greater than 31.</li> </ul>	<p>Either recompile the design in the Quartus II software version 6.1 or change the logical channel address of all alt2gxb megafunctions to 31 or less and recompile the design in Quartus II software versions earlier than 6.1.</p>
<p>The Quartus II software version 6.1 can't compile a design from the HardCopy Advisor once the TimeQuest Timing Analyzer returns an error because the design has not been compiled.</p>	<p>Restart the Quartus II software.</p>
<p>The <b>Examine</b> option is unavailable for CFI devices when there is a file attached to the parent MAX II device.</p>	<p>Using the <b>Examine</b> option for CFI devices with a Programmer Object File (<b>.pof</b>) attached to the parent device is not supported. Remove the file associated with the MAX II device, and the <b>Examine</b> option is available. Use the <b>Examine</b> option on the CFI device as you normally would.</p>
<p>If <b>Export version-compatible database</b> in the <b>Compilation Process Settings</b> page is turned on, using the <b>Check &amp; Save All Netlist Changes</b> command causes an Internal Error during the database export phase of the fit.</p>	<p>Turn off <b>Export version-compatible database</b> in the <b>Compilation Process Settings</b> page before using the <b>Check &amp; Save All Netlist Changes</b> command.</p>

Issue	Workaround
<p>In projects that use VHDL files with Generate constructs, the TimeQuest Timing Analyzer GUI may fail to properly generate Shortcut menu commands on report panels that show a name from the Generate statement. These names have a "\" escape character that the Shortcut menu command removes.</p>	<p>There is no workaround to fix the TimeQuest Timing Analyzer GUI, but you can use the Tcl console to type the required command manually. For the Tcl console, place the name within "{}" to ensure that the Tcl interpreter does not remove the "\" character. For example:</p> <pre>report_timing -to {abc il:\inst}</pre>
<p>You may get one or more messages "Error: Can't generate programming files for project because design file "&lt;name&gt;" is encrypted. It does not have license file support that allows generation of programming files" from the Assembler when compiling a design that is using Altera IP with the OpenCore Plus evaluation feature when your design has VHDL source files that have the construct "use work.all;".</p>	<p>The errors are reported for IP source files that were added to your project by IP Toolbench, but which are not actually used during compilation. Remove the files listed in the error messages from your project file list and recompile the design.</p>
<p>For the HardCopy II device family, the default tasks have the <b>Routing congestion</b> layer turned on. This layer causes the view to show the routing congestion instead of the device resources.</p>	<p>To see the chip resources, open the <b>Layers Settings</b> dialog box and turn off <b>Routing congestion</b> layer for both the main view and the Bird's Eye View.</p>
<p>Running the PowerPlay Power Analyzer directly following an ECO fit results in an Internal Error.</p>	<p>Run the Classic Timing Analyzer (quartus_tan) or the TimeQuest Timing Analyzer (quartus_sta) before you run the PowerPlay Power Analyzer (quartus_pow).</p>

Issue	Workaround
<p>The Quartus II software version 6.1 may run out of memory when Formal Verification is turned on and you are using the Quartus II Integrated Synthesis flow. This happens only when Quartus II Integrated Synthesis extracts finite state machines from the design.</p>	<p>To avoid the out of memory issue in the Quartus II software version 6.1, turn off state machine extraction and rerun synthesis. To turn off state machine extraction, use the following settings in the Quartus II project:</p> <pre>set_global_assignment -name EXTRACT_VERILOG_STATE_MACHINES OFF set_global_assignment -name EXTRACT_VHDL_STATE_MACHINES OFF</pre> <p>You can also use the Quartus II GUI:</p> <ol style="list-style-type: none"> <li>1. On the Assignments menu, click <b>Settings</b>.</li> <li>2. Select <b>Analysis &amp; Synthesis Settings</b>, and click <b>More Settings</b>.</li> <li>3. Turn off <b>Extract Verilog State Machines</b> and <b>Extract VHDL State Machines</b>.</li> </ol>
<p>If you have created a new node using an ECO command or SignalProbe command and have not yet performed a netlist check, clicking <b>Create Timing Netlist</b> in the TimeQuest Timing Analyzer causes the Quartus II software to crash.</p>	<p>Ensure there are no uncommitted ECO changes before clicking <b>Create Timing Netlist</b>.</p>
<p>Simulation models generated by the Megawizard Plug-In Manager for alt2gxb wrappers don't support parameterization of starting_channel_number parameter.</p>	<p>To simulate alt2gxb wrappers with starting_channel_number parameterized (that is, multiple calls to the same wrapper with different parameter settings for starting_channel_number), users need to generate separate wrappers and simulation models for the different parameterized instances</p>
<p>When a design contains IP that is evaluated using the OpenCore Plus hardware evaluation feature, the Quartus II software produces a sequence of Info messages beginning with Info: Elaborated megafunction instantiation "pzdyqx:nabboc".</p>	<p>These messages can be safely ignored.</p>

Issue	Workaround
If a MegaCore is created in the Block Editor and you do not generate a Block Symbol File (.bsf) on the summary page of the MegaWizard Plug-In Manager, you get an error "Found unknown error in Block Symbol File <name>".	Generate the Block Symbol File from the MegaWizard Plug-In Manager summary page.
When viewing a web page or PDF from a MegaWizard, the MegaWizard may try to launch a web browser other than that which is specified on the <b>Internet Connectivity</b> page in the <b>Options</b> dialog box. Instead of using the currently defined web browser, the MegaWizard is using a web browser defined by a previous version of the Quartus II software. If the browser does not exist, you may receive the following error:  Problem opening web browser for <path>/<user_guide_name>	Manually edit the <b>quartus2.ini</b> file and ensure that all instances of the <b>WEB_BROWSER</b> variable point to a valid web browser installation.
In Quartus II and EDA tool simulations of the Stratix III MLAB block, the data output from the MLAB block is incorrect if you de-assert the clock enable between the rising and falling edge of the clock. The simulation models do not show the write, but the write actually happens in the hardware. The same holds true if you assert the clock enable between the rising and falling edge of the clock. The simulation models show the write, but the write does not happen in the hardware.	Keep the clock enable high for more than half the clock cycle beyond the falling edge of the clock for the write to happen. Conversely, if no write is desired, you should keep the clock enable low for more than half the clock cycle beyond the falling edge of the clock.
<b>Version 6.0 SP1</b>	
When evaluating a Tcl script in the TimeQuest Timing Analyzer, calling <code>exit</code> before deleting the timing netlist may result in an Internal Error.	Delete the timing netlist and close the project before exiting TimeQuest using the commands <code>delete_timing_netlist</code> and <code>project_close</code> .
Running multiple instances of the Quartus II software using the same Quartus Project File (.qpf) may cause unpredictable results or may cause the Quartus II software to crash.	Altera recommends that you not open multiple instances of the Quartus II software using the same project.

Issue	Workaround
<b>Version 6.0</b>	
<p>In the classic Timing Analyzer, when a clock (base or derived) is assigned to an internal register, then data paths to and from the register are not analyzed for clock setup and clock hold analysis.</p>	<p>First, analyze the design with the clock settings assigned to the internal registers. Then remove the clock settings from the internal registers and perform a second analysis, checking only paths to and from those registers. The other resolution is to use the TimeQuest Timing Analyzer instead of the classic Timing Analyzer.</p>
<p>If you change an I/O primitive assignment or an <code>altera_attribute</code> assignment, or any assignment made in a Verilog HDL or VHDL design file, the assignment may not be applied to the design database correctly in the next compilation.</p>	<p>Delete the <code>&lt;project&gt;\db</code> directory and recompile the design.</p>
<p>The <b>SignalProbe</b> dialog box may take a long time to open, so it appears that the Quartus II software is “hanging.” The delay is dependent upon the size of the netlist and the number of device pins.</p>	<p>Do not open the <b>SignalProbe</b> dialog box while a compilation is in progress.</p>
<p>The TimeQuest Timing Analyzer erroneously analyzes paths to the asynchronous data pins of registers (that is, the <code>adata</code> pin) during a recovery/removal analysis.</p>	<p>Apply the <code>set_false_path</code> command from the asynchronous data signal’s source port or register to declare these paths as false paths.</p>
<p>If you change the type of a parameter setting in the Quartus II Settings File (<code>.qsf</code>) or a Block Design File (<code>.bdf</code>) and recompile your design, your change appears to have no effect. The type of a parameter is denoted by appending a prefix such as “B” (binary), “D” (decimal). For example, B“10101” represents the binary string “10101”, but D“10101” represents the decimal number 10101.</p>	<p>Delete the <code>&lt;project&gt;\db</code> directory and recompile the design.</p>
<b>Version 5.1 SP2 and earlier</b>	
<p>Due to a limit of the Windows operating system, path names longer than 229 characters can cause an internal error in the Quartus II software.</p>	<p>Make sure that all path names do not exceed 229 characters. This limitation applies to UNIX and Linux installations also.</p>

Issue	Workaround
When you are using the Chip Editor to delete the connections in carry chains, the destination node must be in a legal location for the carry chain. If this is not the case, you will not be able to undo the operation or any prior operations.	Perform the following steps: 1. Delete the <b>Remove-Chain</b> command in the Change Manager. 2. Move the node back to its legal position. 3. Recreate the chain in the Resource Property editor. 4. Move the node to the desired position.
The Quartus II archive feature does not correctly archive files that have duplicate file names, even when they are in different directories. This failure can cause compilation failures when you are using the distributed processing feature of Design Space Explorer (DSE).	Make all design file names unique.
If your design contains illegal pin assignments, and you open the Resources window in the Pin Planner, the Quartus II software may crash.	Remove any illegal pin location assignments before opening the Resources window.
If you make a single-point CUT=ON assignment to a node, and then override it with a point-to-point CUT=OFF assignment on a specific path, the OFF assignment will not be honored.	
Under certain circumstances the Design Assistant reports Critical Warnings (that locate to the altvds_rx or dcfifo megafunction) for your project, which uses the altvds_rx or dcfifo megafunction or an IP core that uses the altvds_rx or dcfifo megafunction.	These warnings can be safely ignored; no action is necessary.
You may receive a “License not found...” error if the path to the license file contains non-ASCII characters.	Change or remove any non-ASCII characters from the license file path.
During a SignalProbe™ compilation, you might receive warning message(s) similar to the following example: “Routing constraints for signal <signal_name> seem to be causing unresolvable routing congestion. The constraints for the signal were removed.”	The Compiler issues these warnings when it is unable to retain the routing constraints from a previous compilation because those routing resources were needed by the SignalProbe signal routing.

Issue	Workaround
There is no distinction between output ports and bidirectional ports in AHDL Function Prototypes; instead, all ports listed after the RETURNS keyword are treated as output ports. As a result, if you specify a bidirectional port in a logic function's Function Prototype Statement and do not connect the port to a top-level bidirectional pin or to other logic in the design where you instantiate the logic function, an error can occur.	Connect the port to a top-level bidirectional pin or to other logic in the design.
Context-sensitive Help is not available for some items in the Quartus II software.	To locate Help on those items, click <b>Search</b> on the Help menu, and type the name of the item.
The Classic Timing Analyzer does not recognize non-PLL clock signals when using any PLL megafunction.	Make clock settings assignments to all non-PLL clocks.
The Waveform Editor does not allow you to create a bus with nodes that are nonconsecutive members of a bus.	Create buses only with nodes that are consecutive members of a bus. Or, use the <b>Group</b> command on the Edit menu to create groups of arbitrary nodes.
If you are using the altcam, altclklock, altlvds_rx, or altlvds_tx megafunctions, the equations shown in the Equations Section of the Compilation Report are not complete.	To view the complete equations for any of these megafunctions, use the Equations window of the Timing Closure Floorplan.
The Quartus II software does not support design file names with more than one extension. For example, you cannot use the file name <b>file.eda.edif</b> .	Use design file names with only one extension.
If you install the Quartus II software for PCs on a UNIX server that exports shares with the Samba software version 1.9.18p10, you may experience problems accessing project files that are also on the network.	Altera recommends using version 1.9.16p11 or 2.0 of the Samba software.
If you make assignments to reserve pins as a group or with group notation (debug [7..0] ), the Quartus II software does not correctly generate simulation output files, and you receive a warning message saying "Unsupported data type in the top-level module."	Reserve the pins using single-name notation (for example, debug [7] , debug [6] , and so on).

Issue	Workaround
Do not change the file permissions (such as changing “read-only” to “read and write”) of Quartus II Settings File (.qsf) and Quartus II Project File (.qpf) while a Quartus II project is open.	Close the Quartus II project before making changes to the file permissions.
Node names containing numbers greater than $2^{31}-1$ (2147483647) will cause an Internal Error in the Quartus II software.	Do not use node names containing large numbers.
Occasionally the Programmer does not allow you to use a MAX 7000AE Programmer Object File (.pof) with a MAX 7000AE device. This error sometimes occurs after a compatible MAX 7000B device is used with the MAX 7000AE POF.	Do not switch between compatible MAX 7000B and MAX 7000AE devices when a MAX 7000AE POF is loaded, or reload the MAX 7000AE POF.
Routing back-annotation may fail if the back-annotated locations do not match the location assignments in the Quartus II Settings File (.qsf) or if the location assignments are missing. This problem can occur if you change devices, or if you remove some location assignments by using the <b>Assignment Editor</b> on the Assignments menu or by manually editing the Quartus II Settings File.	If you experience a “no fit” or an Internal Error while using routing back-annotation, delete the Routing Constraints File (.rcf) and back-annotate the design again after a successful compilation.
Occasionally, the Quartus II software may crash or hang with no error message immediately upon opening a project.	Delete the Quartus II Workspace File (.qws) <i>&lt;project name&gt;.qws</i> from the project directory. If the problem persists, delete the <i>\&lt;project directory&gt;\db</i> directory and recompile the design.
When you are setting phase shift and duty cycle values for clock signals using the altpll megafunction, some combinations of settings may result in values that cannot be synthesized exactly. Under certain circumstances, the Quartus II software attempts to synthesize the phase shift parameter before the duty cycle parameter.	You should first select values for the parameter (phase shift or duty cycle) that is most important for your design.
During compilation or simulation, the Quartus II software may “hang” and not proceed to the next module if a menu or modal dialog box is open at the time the current module finishes running.	Close any open menus or modal dialog boxes before the compilation or simulation reaches the next stage.

Issue	Workaround
Running individual Quartus II software executables ( <b>quartus_map</b> , <b>quartus_fit</b> , and so on) from within the Quartus II Tcl Console may cause the Quartus II software to crash.	Run individual executables either from within the Quartus II scripting shell ( <b>quartus_sh</b> ) or directly at a command prompt.
The time shown in the Status window may not agree with the processing times reported in the Compilation Report. This difference is due to differences in how the times are calculated during processing.	
If you type a name in the entity column of the Assignment Editor that differs from an existing name only by case, the Assignment Editor's "auto-completion" feature always uses the existing name.	Type the new entity name in another application, such as a text editor, copy it to the clipboard, and paste the name from the clipboard into the Assignment Editor.
Altera recommends that you do not use node or entity names that differ only by case if you are using the Quartus II Simulator or Waveform Editor.	
Under certain circumstances, a design that uses <b>Virtual Pin</b> assignments may fail to fit after back-annotation. This situation occurs because the clock signals chosen automatically for the first compilation do not match those chosen for the second compilation.	Manually assign your clock signals, using <b>Virtual Pin Clock</b> assignments before the first compilation, or use Advanced Back-Annotation to explicitly write out the virtual clock assignments before the second compilation.
If you use the <code>dcfifo</code> or <code>scfifo</code> megafunctions in an AHDL design, you may receive an error message similar to "The parameter <code>LPM_WIDTHU</code> has been set to an invalid value..."	Either remove the <code>LPM_WIDTHU</code> parameter arguments from your AHDL <code>dcfifo</code> or <code>scfifo</code> megafunction instantiation, or explicitly set the <code>LPM_WIDTHU</code> parameter to <code>ceil(log2(LPM_NUMWORDS))</code> .
Do not open, change permissions, or delete the <code>/&lt;project directory&gt;/db</code> directory or any file therein while any Quartus II executable is running.	
If you are using the IP Toolbench and add a user library, the Quartus II software may add a backslash (\) to the end of the library file name. The Quartus II user interface ignores this trailing backslash.	

Issue	Workaround
<p>Support for non-decimal radix numbers (such as hexadecimal) used as constants in the <code>lpm_constant</code>, <code>lpm_compare</code>, and <code>lpm_add_sub</code> megafunctions is limited to values that can be represented by 31 bits or fewer.</p>	<p>For values that require more than 31 bits, use decimal radix only.</p>
<p>Under certain circumstances, back-annotation of routing in unreserved LogicLock regions can cause unsatisfiable routing constraints for signals going to clock and clock-enable ports of LABs. This can occur when other portions of the design are not back-annotated, and the Fitter populates empty LCELLs in the back-annotated LogicLock region during subsequent compilations.</p> <p>For example, assume that on the initial compilation, LogicLock region L contains register A, which uses the CLK1 and ENA1 ports of a LAB. When the design is recompiled, the Fitter may place register B, which is not part of region L, and uses the SLOAD input, in the same LAB as register A (assuming that the LAB has sufficient empty space to accommodate it).</p> <p>The LAB control signal generation block does not allow use of both ENA1 and SLOAD in the same LAB; therefore, register A must use the CLK0 and ENA0 ports, rather than CLK1 and ENA1. To avoid a no-route situation, the Fitter will ignore the routing constraints for the clock and enable signals, and re-route the signals using the appropriate control signal multiplexing for the CLK0 and ENA0 ports of the LAB. The Fitter picks the most appropriate routing and, in the majority of cases, the circuit's timing is not adversely affected. When the Fitter is forced to ignore routing constraints, info messages of the form "Info: Can't route signal &lt;name&gt; to atom &lt;name&gt;" are displayed to inform the user; the appearance of such messages is not a cause for alarm.</p>	<p>This situation can be avoided entirely by marking all LogicLock regions as Reserved, thereby preventing the Fitter from placing new items in a region. The tradeoff, of course, is that should a Reserved LogicLock region be under-utilized, the Fitter will be unable to place other logic items in the unused portion of the region.</p>

## Platform-Specific Issues

### Windows Platforms Only

Issue	Workaround
<b>Version 6.1</b>	
<p>The VHO (VHDL Output) generated by the EDA Netlist Writer on Window XP 64-bit might be erroneous when the design contains WYSIWYG atom which has ports with huge port sizes (e.g. rxdprio in of the stratixiigx_hssi_central_management_unit atom). The error will produce functionally incorrect simulation results on the XP-64bit platform when used in third party VHDL simulators such as Modelsim, VCS, and NCSIM.</p>	<p>Use other 32-bit platforms to generate the VHO or using the VO (Verilog Output) for simulation, or contact Altera for a patch. Contact the Regional Service Center for a patch for the Windows 64-bit platform only when using 64-bit Quartus II for Windows XP64. This issue does not affect 32-bit Quartus II behavior for the WinXP32 or WinXP64.</p>
<p>When using 64-bit operation for 64-bit Windows, and when the Use TimeQuest Timing Analyzer during compilation option is turned on, the compilation time is up to twice as long as expected.</p>	<p>Faster compilation time can be restored by using 32-bit operation if the design can be processed in that mode. If 32-bit operation is not an option, you can contact Altera for a software patch that resolves this issue.</p>
<p>After you commit any ECO changes, the detached Resource Property Editor displays old property values. This problem only happens on the currently displayed node.</p>	<p>Relocate the node into Resource Property Editor after you detach the Resource Property Editor.</p>
<p>If the Quartus II software is installed on a network drive, Windows is unable to start the JTAG server service because it does not have rights to read from the network drive (services run before users are logged in). If this service is not running, it is not possible for other computers to use JTAG cables on this machine. Occasionally it is not possible for the Quartus II software to use JTAG cables attached to the same machine.</p>	<p>You can either install the Quartus II software locally or run <code>&lt;full-path-to&gt;/jtagserver --install &lt;username&gt; &lt;password&gt;</code> to specify the username and password that Windows should use when running the JTAG server service.</p>

Issue	Workaround
<p>The installation of the USB Blaster is not successful for Quartus II software version 6.1 because a file is missing.</p>	<p>To update the driver:</p> <ol style="list-style-type: none"> <li>1. Attach the USB Blaster to the USB port.</li> <li>2. In the Control Panel, double-click <b>System</b>, and then click the <b>Hardware</b> tab. Click <b>Device Manager</b>.</li> <li>3. Open the Universal Serial Bus controllers and right-click Altera USB-Blaster 32, and click <b>Update Driver</b>.</li> <li>4. In the Hardware Update wizard, select <b>Install from a list or specific location (Advanced)</b> and click <b>Next</b>. (For Windows 2000, you must select <b>Search for a suitable driver for my device</b> and then select <b>Specify a location</b> and click <b>Next</b>.)</li> <li>5. Browse for the new driver location and click <b>Next</b> (or <b>OK</b> for Windows 2000).</li> <li>6. You may be asked to reselect the location of the driver again if there is a previous driver existing in the system. If you are using Windows 2000, you must select <b>Install one of the other drivers</b>, and then select the path to the new driver again. If you are using Windows XP, you can directly select from the list of drivers and select the new driver path.</li> <li>7. Install the driver. If the system still asks for <b>FTD2XX.sys</b>, your selection was incorrect. You should be asked for <b>FTDIBUS.sys</b>.</li> </ol>
<p>After installing the Quartus II software version 6.1, if you plug in an Altera USB dongle into an XP-64 system, you may be prompted about searching for the driver.</p>	<p>Navigate to <b>c:\Program Files\Common Files\Safenet Sentinel\Sentinel System Driver</b>.</p>
<p><b>Version 6.0</b></p>	
<p>If you are running the Quartus II software on the Windows XP64 operating system, the software may “hang” when the Text Editor is opened.</p>	<p>You must end the <b>quartus.exe</b> process in the Process tab of the Windows Task Manager, delete all the files in your <b>%TEMP%</b> directory, and restart the Quartus II software.</p>
<p>If you are running the Quartus II software on the Windows XP64 operating system with a USB Software Guard, you may receive a message that there is no license found.</p>	<p>You must install the Sentinel driver for the Software Guard by browsing to the <b>quartus/drivers/sentinel/win_xp64</b> directory when asked for the location of the driver.</p>

Issue	Workaround
<b>Version 5.1 SP2 and earlier</b>	
The introduction of Microsoft Security Update MS05-026 prevents the proper display of Quartus II Help across a network.	To properly display HTML Help files, you must access them from a local PC. If you are unable to access Help files locally, go to Microsoft Knowledge Base Article 896054 ( <a href="http://support.microsoft.com/?kbid=896054">support.microsoft.com/?kbid=896054</a> ) for more information about possible workarounds.
The keyboard accelerators (underlines) for Alt+ key combinations do not appear in the Quartus II user interface until the Alt key is pressed the first time.	This behavior is a Windows 2000 user-specified preference. To change to the previous behavior, follow these steps: <ol style="list-style-type: none"> <li>1. On the Start menu, click <b>Control Panel</b>.</li> <li>2. Click <b>Display properties</b>.</li> <li>3. Click the <b>Appearance</b> tab.</li> <li>4. Click <b>Effects</b>.</li> <li>5. Turn off <b>Hide underlined letters for keyboard navigation until I press the Alt key</b>.</li> </ol>
If you use Windows 2000 as a software server to serve the Quartus II software to a client computer running Windows XP, running the Quartus II software on the Windows 2000 server at the same time clients are running the Quartus II software, will cause the Quartus II software on the server to crash.	Do not run the Quartus II software on the Windows 2000 server.
You cannot access the web-based PowerPlay Early Power Estimator on the Altera web site if you have installed Windows XP SP2 because the service pack blocks the active content.	Refer to the Altera Knowledge Database on the Altera web site for more information on enabling your browser to access the PowerPlay Early Power Estimator spreadsheets.
Some dialog box title bar text is not displayed correctly when the Quartus II software is installed on a computer running the Chinese version of Windows XP.	Change the font in the <b>Active Title Bar</b> section of the <b>Windows Appearance</b> Control Panel.
If you do not have Administrator privileges when you install the Quartus II software, certain features of the software, particularly the online Help, will not work properly, for example: <ul style="list-style-type: none"> <li>• Software guards (parallel and USB)</li> <li>• Programming with JTAG server</li> </ul>	Altera recommends that you have Administrator privileges when installing the Quartus II software.

Issue	Workaround
<p>Under certain circumstances, the Quartus II installation program may crash or you may receive an error message immediately upon launching the installation program.</p>	<p>Reinstall the <b>stdole32.tlb</b> file from the original Windows distribution disks. To reinstall the file, type the appropriate command at a command prompt. (Note: the command must be typed on one line.)</p> <p><b>Windows 2000:</b> &lt;CD-ROM drive letter&gt;:\i386\expand.exe stdole32.tl_ %SystemRoot%\System32\stdole32.tlb &lt;Enter&gt;</p> <p><b>Windows XP:</b> &lt;CD-ROM drive letter&gt;:\i386\expand.exe stdole32.tl_ %SystemRoot%\System32\stdole32.tlb &lt;Enter&gt;</p>
<p>If the full, hierarchical name of an instance exceeds 247 characters, it may not be displayed properly in the Quartus II user interface. This problem occurs most often with EDIF netlist files generated by other EDA synthesis tools.</p>	<p>Limit the full, hierarchical instance name to fewer than 247 characters if possible.</p>
<p>If you are running the Quartus II software from a network server, the Quartus II software will not run properly on the client computer if you share the <b>\quartus\bin</b> directory.</p>	<p>You must share the <b>\quartus</b> directory, not the <b>\quartus\bin</b> directory.</p>
<p>The Quartus II software is not compatible with the MATLAB web server.</p>	<p>Turn off the MATLAB web server in the <b>Services Control Panel</b> on the Start menu before running the Quartus II software.</p>
<p>Under some circumstances, the Quartus II splash screen appears and the Quartus II icon appears in the Taskbar, but the graphical user interface does not appear. Under other circumstances, the user interface appears but windows and/or toolbars do not appear correctly.</p>	<p>The registry settings controlling the position of the Quartus II windows may have become corrupted. If the user interface appears, click the <b>Reset All</b> button on the <b>Toolbars</b> page of the <b>Customize</b> dialog box, or, if the user interface does not appear, type the following command at a command prompt: quartus -reset_desktop &lt;Enter&gt;</p>

Issue	Workaround
<p>If you install the stand-alone Quartus II Programmer and the Quartus II software, and then uninstall either one, the Programmer may report “JTAG Server -- internal error code 82 occurred” when you click the <b>Add Hardware</b> button in the <b>Hardware Setup</b> dialog box on the Edit menu. This error occurs because uninstalling the software has disabled the JTAG Server service.</p>	<p>Manually restart the JTAG Server service by locating the <b>jtagserver.exe</b> program and at a command prompt for that directory, type <code>jtagserver --install</code> &lt;Enter&gt;</p>
<p>If you choose to uninstall a previous version of the Quartus II software during installation, and there is a “locked” file or directory, the installation program will not reboot the computer as is necessary to successfully complete the installation.</p>	<p>Exit from the installer and reboot the computer manually after the removal of the previous version is complete, before completing the installation of the new version.</p>
<p>The Quartus II software version 4.2 and later does not allow a Parallel Port Software Guard (T-guard or dongle) to be used on the same parallel port as a ByteBlaster™ II download cable.</p>	<p>Use another download cable, such as a USB-Blaster™ or MasterBlaster™ to configure your device, or use separate parallel ports for the Software Guard and the download cable. The Quartus II Programmer is not a licensed feature, so you can remove the Software Guard to program your device, but you must replace it to use any other Quartus II software features. You can also use the USB Software Guard.</p>
<p>During installation of the Quartus II software, when you insert the ModelSim-Altera CD-ROM, a Windows Explorer window may appear.</p>	<p>Close the Windows Explorer window before proceeding with the installation.</p>

**Solaris & Linux**

Issue	Workaround
<p><b>Version 6.1</b></p>	
<p>Using the Cut, Copy, and Paste features in the TimeQuest SDC File Editor may cause the software to hang, close unexpectedly, or both.</p>	<p>Instead of using these features in the TimeQuest SDC File Editor, use an external text editor if these features are necessary.</p>

Issue	Workaround
<p>Under some circumstances, your web browser software may fail to launch correctly from the IP MegaStore MegaWizard Plug-In Manager. The web browser defined in the MegaWizard Plug-In Manager for the IP MegaStore inherits the environment settings from the Quartus II software. Specifically, the LD_LIBRARY_PATH environment variable may contain entries that conflict with web browsers such as FireFox, preventing them from starting correctly.</p>	<p>Edit the script that launches the web browser to make sure the Quartus II directories are the last entries in the LD_LIBRARY_PATH variable.</p>
<p><b>Version 6.0</b></p>	
<p>When using the TimeQuest Timing Analyzer Graphical User Interface, occasionally when sourcing a script or generating several report panels in rapid succession (for example, the “Macros” in the Task pane), the user interface may not display any report data at all, or the report data may be old or incomplete. On Linux, the GUI may crash completely. This is due to UNIX file systems not synchronizing between when the user interface reads the report file while the report panels are being generated. The problem is worse with large reports and on slow file systems (for example across a slow network).</p>	<p>Generate only one individual report panel at a time manually from the GUI. This gives the TimeQuest analyzer a chance to finish generating the report panel before the GUI reads and displays it.</p>
<p>Performing any operation on a flash memory connected to a MAX II device used in a Parallel Flash Loader configuration scheme may cause the Quartus II software to crash with an internal error.</p>	<p>Use a Windows-based computer to configure devices used in a Parallel Flash Loader configuration scheme.</p>
<p>While any shortcut menu is open from an undocked dockable window, if you right-click in the title bar, then all activity in the title bar (left-click and drag, right click context menu, 'X' close button) stops working.</p>	<p>Display a shortcut menu again and perform any action except right-clicking in the title bar to restore normal operation.</p>

Issue	Workaround
<b>Version 5.1 SP2 and earlier</b>	
If the operating system crashes, and the file system in \$TMP is rebuilt automatically, the data in the \$TMP/Mw_<user ID> file is corrupted, the Quartus II software may fail to start correctly.	Delete the \$TMP/Mw_<user ID> file and restart the Quartus II software.
If you are using the Exceed X server software for Windows while running the Quartus II software, the font size may be larger than the line height. This problem occurs most often if you installed the Exceed software while running at a screen resolution greater than 1024 × 768.	Reinstall the Exceed software while running at a screen resolution of 1024 × 768. You can then switch back to your normal, higher resolution setting.
Under some circumstances, there may be editor windows listed on the Window menu that you cannot see.	To display the hidden windows, click <b>Cascade</b> on the Window menu.
You cannot launch the AXD Debugger software from within the Quartus II software.	Launch the AXD Debugger software from outside the Quartus II software.
Under some circumstances, the Internet connectivity features of the Quartus II software are not functional.	Specify the full path to your web browser software on the <b>Internet Connectivity</b> page of the <b>Options</b> dialog box. If you access the Internet through a proxy server, you must also specify the address of the proxy server and its port number.
Under some circumstances you cannot access the Quartus II online Help in the user interface.	To access Help, type <code>hh quartus.chm</code> <Return> at a command prompt.
If you are accessing the Quartus II software through one of the following versions of the Hummingbird Exceed software (6.2, 7.0, 7.1, or 8.0) and have any Microsoft Office application or Internet Explorer open, the Quartus II user interface may start very slowly.	Contact Hummingbird Software at <a href="http://www.hummingbird.com">www.hummingbird.com</a> for a patch for the Exceed software.
The stand-alone Quartus II Programmer and SignalTap® II programs are not available on Solaris and Linux workstations.	

**Linux Only**

Issue	Workaround
<b>Version 6.0</b>	
The Quartus II software may crash with a core dump if you close the Quartus II software while a properties dialog box is open from any link in Help.	Do not open the properties dialog box on any link in Help.
When you are running the Quartus II software on Red Hat Enterprise Linux 4.0 and using the KDE 3.3 desktop, the Quartus II software may 'hang' when a graphical tool such as the Chip Editor or Pin Planner displays a tooltip when you select an element to edit.	Set the environment variable <code>cui_disable_tooltips = 1</code> to disable tooltips.
Your programming hardware is not shown in the <b>Add Hardware</b> dialog box when running under Red Hat Enterprise Linux 64.	Only the EthernetBlaster is supported for programming on 64-bit platforms.
<b>Version 5.1 SP2 and earlier</b>	
If you run a remote Linux desktop session in a Windows client such as Exceed, depending on your configuration, the SignalTap II Logic Analyzer may be unstable and could crash with a segmentation fault.	Use an Xterm window to access the Quartus II software instead of a remote desktop session.
Clicking the "X" close button is visible on the Chip Editor loading progress dialog box may cause the Quartus II software to crash.	Do not click the "X" button while the Chip Editor is loading.
If the MasterBlaster download cable is not listed in the <b>Available hardware items</b> list in the <b>Hardware Settings</b> tab of the <b>Hardware Setup</b> dialog box, but it is connected properly, you may not have read/write permission for the serial ( <code>dev/ttySx</code> ) port to which the MasterBlaster cable is connected.	Have a system administrator assign read/write permission for the appropriate port. This change can be accomplished by adding you to the "uucp" group, or by giving read/write permission for the serial port to everyone, using the following command: <code>chmod o+rw /dev/ttySx</code> where <i>x</i> is the serial port affected.
If you are using the ReflectionX X-server software as your display on a Linux workstation, the Quartus II software may hang and a white box may appear.	Set the <code>QUARTUS_MWWM</code> environment variable to <code>allwm</code> and then start the Quartus II software without the splash screen by typing the following commands at a command prompt: <code>setenv QUARTUS_MWWM allwm &lt;Return&gt;</code> <code>quartus -no_splash &lt;Return&gt;</code>

Issue	Workaround
Under certain circumstances, the Quartus II software may not start properly.	On a system with a static IP address, ensure that the <b>/etc/hosts</b> file has an entry for the host name of the machine on which you are running. For example, if the workstation is named “orange,” there should be an entry in <b>/etc/hosts</b> with the IP address of the “orange” workstation as shown below: <pre>&lt;IP address of orange&gt; orange</pre> In addition, the network configuration (hostname, DHCP host name, DNS search path, and domain names) must be correct or the Quartus II software will abort on startup.
If you are running the Quartus II software version 4.0 and later using VNC software, the Quartus II software may terminate unexpectedly whenever you open any file or browse any directory from within the Quartus II software.	Make sure your VNC server software is version 3.3.4 or later.
If you are running the Quartus II software under Red Hat Linux 8.0, you may experience substantial degradation of compilation times if your design files are located on a separate server from the Quartus II software.	Make sure that the operating system kernel is upgraded to the latest available. If you are using a NetApps server, refer to the following document for more information: <a href="http://www.netapp.com/tech_library/ftp/3183.pdf">www.netapp.com/tech_library/ftp/3183.pdf</a>

## Device Family Issues

### Cyclone, Stratix & Stratix GX

Issue	Workaround
<b>Version 6.0</b>	
The Altera PCI core may have timing violations if you have selected <b>Use TimeQuest Timing Analyzer during compilation</b> and you are targeting a Stratix, Stratix GX, or Cyclone II device.	To improve the optimization of the PCI core in this case, which will likely resolve the timing violations, add the following line to your <b>&lt;revision_name&gt;.qsf</b> file: <pre>set_global_assignment -name INI_VARS "FITTER OPTIMIZE BIAS FOR PCI=ON"</pre>

Issue	Workaround
Editing the global level of an input port in Resource Property Editor for Stratix, Stratix GX, Cyclone or MAX II devices may cause an Internal Error when you click <b>Check and Save All Netlist Changes</b> .	In order to prevent this error, either 1) modify the global levels of <i>all</i> input ports fed by the driving output port of the input port; or 2) remove the connections associated with the other fan-outs of the driving output port using the Resource Property Editor and restore the logical connection using the Change Manager.
The method used to report power for clock networks is different between the Quartus II PowerPlay Power Analyzer and the PowerPlay Early Power Estimator (EPE). The Quartus II PowerPlay analyzer reports the power for the resource (pin or PLL) that drives the network, while the EPE reports the power in the Clock Network section of the spreadsheet.	No action is necessary.
<b>Version 5.1 SP2 and earlier</b>	
When you use a Routing Constraints File (.rcf) to control fitting after performing Routing Back-Annotation, your timing analysis results may change slightly due to parasitic and other effects. Any change will be very small.	
If you use the SignalProbe feature to observe the signals at an output pin, by routing them to another output pin, the SignalProbe output pin signal will be shown as Unknown (X) in the Quartus II Simulator.	The signal will be correct in actual operation, the error appears only in the Quartus II Simulator.
In the <b>SignalProbe Source to Output Delays</b> table of the Timing Analyzer Report, the following shortcut menu commands are not available although they are available in other similar Timing Analyzer Report tables: <ul style="list-style-type: none"> <li>• List Paths</li> <li>• Locate in Chip Editor</li> <li>• Locate in Timing Closure Floorplan</li> </ul>	You can use other Timing Analyzer Report tables to list and locate the affected paths.

**Stratix and Stratix GX**

Issue	Workaround
<b>Version 6.0</b>	
<p>The Quartus II PowerPlay Power Analyzer reports PLL, XGMII state machine, GXB transceiver, and I/O pin power as contributors to the power reported for High Speed Transceiver blocks. However, the PowerPlay Early Power Estimator (EPE) spreadsheet reports this power in a “High Speed Transceiver Blocks” section as well as an entry in the “Clock Networks” section. Similarly, the PLL, SERDES blocks, and I/O pins of an LVDS block are reported in the PowerPlay Power Analyzer, and as entries in the Clock Networks and HSDI sections of the EPE spreadsheet.</p>	
<b>Version 5.1 SP2 and earlier</b>	
<p>If you use the altddio_bidir or alt_dqs megafunction and connect any data port directly to VCC or GND, the Quartus II software version 3.0 SP1 and later will insert an additional logic element in the circuit path.</p>	
<p>The behavior of the 0-degree phase shift setting of the DLL_PHASE_SHIFT parameter of the alt_dqs megafunction or the <b>DQS Phase Shift</b> logic option with the altddio_bidir megafunction has changed in the Quartus II software version 3.0 SP2. The previous behavior produced an uncharacterized delay that cannot be specified to fall within the specified 500 ps delay difference.</p>	<p>If your design uses this setting and does not work correctly after installing the Quartus II software version 3.0 SP2 or later, you should contact the Altera Applications department for further information.</p>

**Stratix**

Issue	Workaround
<p>Designs compiled for Stratix EP1S40ES devices must be recompiled for the EP1S40 device before programming.</p>	

Issue	Workaround
Stratix PLL simulation models have been enhanced to handle jitter on the input clock. This enhancement has the unintended side effect that functional simulations for LVDS designs using cascaded PLLs may be incorrect by one clock cycle.	Altera recommends that you perform Timing Simulation to display the correct behavior in the Quartus II Simulator or in other EDA Simulators.

**Stratix II**

Issue	Workaround
<b>Version 6.1</b>	
The PLL automatically generated for use with the ALTMEMPHY megafunction for designs that target Stratix II devices does not have its locked output held low after the PLL initializes. This may result in incorrect hardware behavior.	Use the PLL MegaWizard Plug-in to turn on the locked output signal after the PLL initializes.
<b>Version 6.0 and earlier</b>	
An intermittent read failure has been detected on Stratix II M4K RAMs due to a software configuration error for designs compiled with Quartus II software version 5.0 SP1 and earlier.	This issue has been resolved in the Quartus II software 5.0 Service Pack 2 and Quartus II software version 5.1. To learn more about this issue, please refer to the Stratix II Errata on the Altera website.
Due to changes in the altlvds_tx and altlvds_rx megafunctions in the Quartus II software version 5.0, user-created timing assignments to the megafunctions are changed. The megafunctions now make most timing assignments automatically.	Check your assignments to make sure that the Quartus II software implemented them correctly.
The Quartus II software version 5.0 does not support programming file generation for some Stratix II devices when M-RAM blocks are used in some memory modes, and if the STRATIXII_MRAM_COMPATIBILITY option is turned off.	For more information about programming file support for Stratix II devices, please refer to the <i>Stratix II FPGA Family Errata Sheet</i> , which is available on the Altera website.
The Quartus II software version 4.2 and later supports programming file generation for EP2S60 ES devices, but only for designs where the M-RAM memory is not used.	For more information about programming file support for Stratix II devices, please refer to the <i>Stratix II FPGA Family Errata Sheet</i> , which is available on the Altera website.

Issue	Workaround
Back-annotating some designs targeted to a Stratix II device with the <b>Demote cell assignments to</b> option set to <b>LABs</b> may prevent the design from fitting.	Back-annotate the design with <b>Demote cell assignments to</b> turned off.

**Stratix GX**

Issue	Workaround
<b>Version 6.0</b>	
Timing simulation performed in the Quartus II software on designs that use the altgxb megafunction in Stratix GX devices is not accurate on the rx_clkout and rx_out outputs. The simulation is functionally correct, but the relative timing delays between the signals are not accurate.	Perform your timing simulation in another tool such as ModelSim.
<b>Version 5.1 SP2 and earlier</b>	
The RREFB pin names for EP1SGX10C, EP1SGX25C, EP1SGX25D, and the EP1SGX40F devices changed in the Quartus II software version 5.0. This may affect your PCB layout.	Each RREFB pin must be tied to ground through a resistor. Altera recommends that you not connect multiple RREFB pins through a single resistor to ground.

**Stratix II GX**

Issue	Workaround
<b>Version 6.0 SP1</b>	
When you select SONET OC-48 configurations in the alt2gxb megafunction and the “ <b>Flip word alignment pattern bits</b> ” option is turned off, it is possible that the byte ordering block may lock to a data pattern that is not optimal.	Do not turn off the “ <b>Flip word alignment pattern bits</b> ” option (it is on by default).

Issue	Workaround
<b>Version 6.0</b>	
<p>The latency of alt2gxb megafunction simulations on Stratix II GX is not accurate in comparison to the device. This is due to approximation used in the Quartus II simulation in modeling the analog portion of the hardware. The latency on the digital portion is within the range of a few clock cycles of the device. The latency is an exact match with the hardware when input vectors are carefully made and do not contain any race conditions.</p>	<p>The Stratix II GX handbook has specified latency range information. The latency information from Quartus II simulations is a good approximation.</p>
<p>You may receive an error message saying “The Quartus II software could not combine the following GXB REFCLK divider(s)...” when performing incremental compilation on a Stratix II GX design. These error messages result from two causes:</p> <ol style="list-style-type: none"> <li>1. You are trying to combine multiple alt2gxb megafunctions and they are not in the same partition.</li> <li>2. You are using multiple alt2gxb megafunctions that use a calibration block, and are not in the same partition.</li> </ol>	<ol style="list-style-type: none"> <li>1. Place all alt2gxb megafunctions in the same partition.</li> <li>2. There is only one calibration block in the device. You should enable the calibration block for one instance of the alt2gxb megafunction only, and disable the calibration block for the other instances.</li> </ol>
<b>Version 5.1 SP2 and earlier</b>	
<p>In Basic protocol, when the 8B10B encoder is used, the alt2gxb MegaWizard provides the tx_forcedisp and tx_dispval ports. These ports do not have any effect on the transmitted serial data when used in the Quartus II software version 5.1. This behavior is reflected in simulation.</p>	<p>None necessary.</p>

**Stratix III**

Issue	Workaround
<b>Version 6.1</b>	
<p>Compiling a Stratix III design with a multiplier in Two-Level-Adder Chainout Mode or Multiply-Accumulator Chainout Mode may result in an internal error in some specific clocking schemes. Specifically, the error occurs when the roundchainout or saturatechainout signal is registered at the second-adder with a clock that is different from the output clock.</p>	<p>Use the same clock for both signals.</p>
<p>The Quartus II software version 6.1 does not perform placement and I/O standard legality checks for input termination on a bidirectional pin when this bidirectional pin is using both input (parallel) and output (series) termination at the same time.</p>	<p>Follow the I/O standard and location guidelines for dynamic Parallel OCT as described in the Stratix III device handbook.</p>
<p>Stratix III designs with PLLs originally generated for Stratix II give errors during the Quartus II functional simulation netlist generation step.</p>	<p>Regenerate the PLL for the Stratix III design.</p>
<p>The assignments generated for the ALTMEMPHY megafunction assume that the top level pin names match the pins on the ALTMEMPHY variation. Using different names for your top level pins, including using single bit signals instead of one-bit busses, will result in incorrect behavior.</p>	<p>Use the Assignment Editor to change the assignments to match the top-level pin names in your design.</p>
<p>Timing requirements for the ALTMEMPHY megafunction in designs that target Stratix III devices may not be met on the address and command timing paths.</p>	<p>Use the MegaWizard Plug-In Manager to adjust the phase of the dedicated address and command clock (C6) from 315 degrees to a value that causes your design to achieve timing closure.</p>
<p>Placement of the ALTMEMPHY megafunction on the side I/Os of a Stratix III device results in a no fit because an incorrect dqs_input_frequency parameter is applied to the dqs_delay_chain WYSIWYG.</p>	<p>In the HDL file <code>&lt;instance&gt;_alt_mem_phy_dqs_ip_siii.v</code> (or <code>.vhd</code>), search for "dqs_input_frequency". This parameter has the picosecond setting <b>2500 ps</b>. Change the number setting to the period of the memory clock.</p>

**Cyclone**

Issue	Workaround
Altera recommends that the frequency of the external clock output of the PLLs be limited to 312 MHz.	
The operating frequency range of the Cyclone PLL has been changed. In the Quartus II software version 3.0 and earlier, the range was 300 MHz to 800 MHz. In version 3.0 Service Pack 1 and later, that range changed to 500 MHz to 1000 MHz because of concerns about jitter at frequencies below 500 MHz. Because of this change, the minimum input frequency is now 15.625 MHz (previously 15 MHz) and the minimum output frequency is also 15.625 MHz (previously 9.38 MHz).	Recompile your design after installing the current version of the Quartus II software.
The PLL lock circuit does not function correctly for PFD (Phase Frequency Detector) frequencies below 200 MHz when the temperature is below -20°C.	If operation at temperatures below -20°C is required, choose a higher input frequency and clock division (N) factor such that the PFD input frequency is higher than 200 MHz.

**Cyclone II**

Issue	Workaround
<b>Version 6.0</b>	
If your design uses a Cyclone or Cyclone II device and you add the VREF Pad column to the Pin Planner UI, the Quartus II software may crash with an internal error.	Do not use the VREF Pad column in the Pin Planner if your design is for a Cyclone or Cyclone II device. If you have already added the column, open a project that uses a device family other than Cyclone or Cyclone II, open the Pin Planner, and turn off the VREF Pad column.
<b>Version 5.1 SP2 and earlier</b>	
A write error has been detected on Cyclone II M4K RAMs when using dual ports and dual clocks for designs compiled with Quartus II software version 5.0 SP1 and earlier.	A software workaround is available to address this issue in the Quartus II software version 5.0 SP2 and Quartus II software version 5.1. To learn more, please refer to the Cyclone II Errata on the Altera website

Issue	Workaround
<p>If your design uses dual-port, dual-clock memory with a Memory Initialization File (.mif) and you have set the CYCLONE_SAFE_WRITE parameter in the altsyncram megafunction to RESTRUCTURE, any changes to the MIF file contents will be ignored if you have Smart Compilation turned on.</p>	
<p>Back-annotating some designs targeted to a Cyclone II device with the <b>Demote cell assignments to</b> option set to <b>LABs</b> may prevent the design from fitting.</p>	<p>Back-annotate the design with <b>Demote cell assignments to</b> turned off.</p>

**MAX II**

Issue	Workaround
<p>If your design uses an <code>altparallel_flash_loader</code> instantiation created in the Quartus II software version 5.0 SP1 or earlier, you may receive errors during compilation because the port names have changed in the <code>altparallel_flash_loader</code> megafunction included in the Quartus II software version 5.1.</p>	<p>Use the Megawizard Plug-in Manager to regenerate your <code>altparallel_flash_loader</code> instantiation. Modify your design files to connect to the new <code>altparallel_flash_loader</code> port names.</p>

**HardCopy II**

Issue	Workaround
<p><b>Version 6.0</b></p>	
<p>The Quartus II software may crash with an internal error when you perform an incremental compilation on a HardCopy II design.</p>	<p>Turn off the Incremental Compilation option and remove your design partitions before compiling.</p>
<p>A HardCopy II design that contains latches with preset or clear signals and a constant (VCC or GND) data, may cause the HardCopy II Revision Compare tool to report a difference in the timing constraints because of a difference in which signal is considered the enable for the latch.</p>	<p>No workaround is necessary, and you can safely ignore the warning.</p>

Issue	Workaround
Formal verification is not supported during development of designs for migration to HardCopy II devices.	If you must use formal verification during development of your HardCopy II design, you must turn off formal verification options, perform full compilations on both (Stratix II and HardCopy II) revisions, and perform the migration again before generating the handoff files.
When migrating a design from Stratix II to HardCopy II, the Revision Compare tool can report differences between the two revisions because of different packing of fast I/O registers because additional packing can be performed on HardCopy II devices that cannot be performed on Stratix II devices.	Either accept the additional packing, and ignore the reported differences or disable Fast I/O assignments on the nodes reported by the Revision Compare tool.
The Design Space Explorer's Search for Lowest Power functionality is not available for HardCopy II devices.	To optimize the device power in a design that targets a HardCopy II device, follow the recommendations in the Power Optimization Advisor, and manually run the Power Analyzer in the Quartus II software to determine the results.
Under certain circumstances, the HardCopy II Companion Revision Comparison tool may report a mismatch in Memory Initialization Files (.mif) between the Stratix II and HardCopy II revisions.	Manually compare the Memory Initialization Files to determine if they are functionally equivalent.
Under certain circumstances, you may receive the following error message when migrating your Stratix II design that contains RAM blocks to HardCopy II: Error: Source file <file> in directory <dir> was compiled at <time> and saved at <time>. The problem reported for the file is: Only in HardCopy II (<design>).	Turn off the <b>Auto RAM Block Balancing</b> option for your Stratix II design and recompile the design. Then proceed with the migration process.

Issue	Workaround
<b>Version 5.1 SP2 and earlier</b>	
<p>The HardCopy II Companion Revision Comparison tool can be too strict and produce false positives. That is, it flags certain netlist block differences as functionality differences when they do not actually produce different behavior in silicon. The following example illustrates this behavior:</p> <ul style="list-style-type: none"> <li>• The Companion Revision Comparison tool considers a global assignment of &lt;NONE&gt; to be different from "" (null), and reports a difference.</li> </ul>	<p>In each of these cases, the functionality of the two revisions is the same in silicon, but you must manually verify that the functionality is the same. You can use the block names listed in the Companion Revision Report to locate to the Resource Property Editor to verify the functionality</p>
<p>PCI core designs compiled with versions of the PCI Compiler earlier than 4.0.0 will cause numerous spurious differences to be reported in the Companion Revision Compare section of the Compilation Report, even though the source files are correct.</p>	<p>Recompile the PCI core with the PCI Compiler version 4.0.0 or later.</p>
<p>You may receive Revision Comparison warnings about differing EDA tool settings if your project directory contains a Quartus II Defaults File (.qdf).</p>	<p>Delete the Quartus II Defaults File from your project directory.</p>

**EPC2 Configuration Devices**

Issue	Workaround
<b>Version 6.0</b>	
<p>When using the EPC2 configuration device to configure an Altera FPGA using a compressed configuration bit stream, you may encounter a configuration failure due to the CONF_DONE error checking feature. The failure mode occurs when the FPGA releases the CONF_DONE signal outside the acceptable time window. The reason this may occur is because the compression ratio varies depending on the design file. Since the configuration file size varies due to compression there may be insufficient padding at the end of the configuration file. This issue can result in a configuration failure, as indicated by the nSTATUS pin transitioning low near the end of configuration. The error occurs because the CONF_DONE signal is released by the FPGA before the EPC2 device expects it to be released</p>	<p>For assistance implementing the work around, please contact Altera Technical Support at <a href="http://www.altera.com/mysupport">www.altera.com/mysupport</a>, and click “Create New Service Request”.</p>

## Design Flow Issues

### Verification

Issue	Workaround
<b>Version 6.1</b>	
<p>The ALTMEMPHY VHDL code may fail to compile in simulators other than Modelsim because of a missing library clause.</p>	<p>Generate your ALTMEMPHY variation in Verilog HDL or edit the following files, which were generated in the project directory. Insert the necessary "LIBRARY STRATIXII;" or "LIBRARY STRATIXIII;" clause as appropriate. Note: The file names are prefixed by the variation name.</p> <p>STRATIX III Files</p> <p><b>alt_mem_phy_ac_siii.vhd</b>  <b>alt_mem_phy_clk_reset_siii.vhd</b>  <b>alt_mem_phy_dm_siii.vhd</b>  <b>alt_mem_phy_dp_io_siii.vhd</b>  <b>alt_mem_phy_dq_io_siii.vhd</b>  <b>alt_mem_phy_dqs_ip_siii.vhd</b>  <b>alt_mem_phy_dqs_op_siii.vhd</b></p> <p>STRATIX II Files</p> <p><b>alt_mem_phy_dp_io_sii.vhd</b>  <b>alt_mem_phy_clk_reset_sii.vhd</b></p>
<p>The ALTMEMPHY Verilog code may fail to compile in simulators other than Modelsim because some regs are declared within a generate block but referenced outside the block.</p>	<p>Edit the <i>&lt;variation name&gt;</i>_alt_mem_phy_read_dp_sii_ciii.v file that was generated in the project directory, and move the declaration for the following regs from the generate block to the declaration section at the top of the file.</p> <pre>inc_read_lat_ams inc_read_lat_sync dec_read_lat_ams dec_read_lat_sync</pre>
<b>Version 6.0 and earlier</b>	
<p>If you are using IP Toolbench to generate simulation models for Altera IP Megacore® functions, you will get an error if support for the Stratix device family is not installed.</p>	<p>Install support for the Stratix device family.</p>

Issue	Workaround
<p>If you are using IP Toolbench to generate simulation models for Altera IP Megacore<sup>®</sup> functions, and you do not turn on <b>Generate Simulation Model</b> in the <b>Set Up Simulation Model</b> dialog box during setup, you will get an error when you launch the simulation using Modelsim.</p>	<p>Turn on <b>Generate Simulation Model</b> in the <b>Set Up Simulation Model</b> dialog box and regenerate the Megacore<sup>®</sup> .</p>

**Megafunction**

Issue	Workaround
<p><b>Version 6.1</b></p>	
<p>If you generate the floating-point divider megafunction in the MegaWizard Plug-In Manager in the AHDL format, there is a compilation error for two modes, the reduced_functionality = “NO” and “denormal_support = “NO” mode, and the reduced_functionality = “YES” mode.</p> <p>The compilation process is stopped before compilation is complete with the error “Warning: underflow is missing source”.</p>	<p>Manually remove the underflow output port and wires connecting to the underflow output port from the wizard-generated AHDL design.</p>

**Integrated Synthesis (VHDL and Verilog HDL)**

Issue	Workaround
<p><b>Version 6.0 SP1</b></p>	
<p>In the Quartus II software version 6.0 and earlier, when an inverted cone of logic drove a bidir pin, the inversion was incorrectly removed.</p>	<p>Recompile your design with the Quartus II software version 6.0 SP1 or later.</p>
<p>In the Quartus II software version 6.0 and earlier, the Quartus II Integrated Synthesis ignored the default value for an incomplete CASE statement if the CASE statement has overlapping conditions in the same CASE item.</p>	<p>Recompile your design with the Quartus II software version 6.0 SP1 or later.</p>

Issue	Workaround
<p>Quartus II Integrated Synthesis does not correctly synthesize two or more configured instances of the same entity in the same VHDL hierarchy if they have different generic settings.</p>	<p>Recompile the design with the Quartus II software version 6.1.</p>
<p><b>Version 6.0 and earlier</b></p>	
<p>When a VHDL or Verilog design specifies a RAM, there are a few cases in which the read-during-write behavior of the RAM will differ between the original design and the hardware implementation and no warning will be given. The following examples illustrate this behavior:</p> <p>The first case occurs when a RAM in a lower-level module directly drives a set of registers in an upper-level module. To work around this problem, move the registers to the lower-level module.</p> <p>The second case occurs when there is combinational logic between a RAM and a set of registers, and the design specifies the write operation of the RAM will occur before the read operation. To work around this problem, remove the logic between the RAM and the registers.</p> <p>The third case is the same as the second case, with the exception that the design specifies the read operation of the RAM will occur before the write operation, and the read address of the RAM is registered. To get around this problem, either remove the logic between the RAM and the registers, or set the <b>Automatic RAM Replacement</b> option to <b>Off</b>.</p>	<p>The workaround for each case is shown immediately following the example.</p>

**Verilog HDL Integrated Synthesis**

Issue	Workaround
A Verilog HDL design that compiles successfully in earlier versions fails in the Quartus II software version 5.1 with the message "Formal port <port_name> must be connected to a structural net expression."	The Verilog language requires that a module instance output port be connected to a net, and not to a reg variable or to a constant. Previous versions of the Quartus II software did not enforce this restriction. Change the variable connected to the module instance output port to a wire datatype.
A Verilog design that compiles successfully in earlier versions fails in the Quartus II software version 5.0 with the message "Error: Verilog HDL or VHDL error at <filename(line)>: object "<pin_name>" declared in a List of Port Declarations cannot be redeclared within the Module Body"	Remove the declaration in the module body. Ports must be completely specified in the Verilog 2001 list of ports declaration, including where necessary the direction, width, net or variable type, and whether the port is signed or unsigned.

**SOPC Builder Issues**

Issue	Workaround
<b>Version 6.1</b>	
Port names might change on an SOPC Builder system module that includes a tristate bridge. SOPC Builder v6.1 uses different rules to name shared ports associated with a tristate bridge, which might cause a port name mismatch in HDL design files that instantiate the system module.	Update your HDL design file to use the new port names.
<p>Compiling an SOPC Builder design generates "Warning: Found invalid timing assignments -- see Ignored Timing Assignments report for details".</p> <p>SOPC Builder erroneously applies an invalid timing assignment as an embedded attribute in the HDL code it generates.</p>	You can ignore these warnings for the SOPC Builder system.
The <b>Browse Project Directory</b> command on the File menu in SOPC Builder fails when the project directory has a space in it.	Browse the directory using an external tool.

<b>Issue</b>	<b>Workaround</b>
SOPC Builder does not find Nios II components on Linux.	Run the <code>sdk_shell</code> script located in the top level of the Nios II EDS directory to allow SOPC Builder to find the Nios II components.
SOPC Builder doesn't launch when you double-click an SOPC Builder-created Block Design File (.bdf) when the Quartus II software is installed in a path with spaces in it.	Either launch SOPC Builder through the Quartus II icon or menu or don't install the Quartus II software in a path with spaces.
SOPC Builder can't launch ModelSim when the path to ModelSim contains spaces.	Use Windows renaming, for example, instead of <b>c:/program files/altera/61/modelsim_ae/win32aloem</b> use <b>c:/progra~1/altera/61/modelsim_ae/win32aloem</b>
<b>Version 6.0</b>	
The Avalon Interface Specification incorrectly describes the behavior for <code>address</code> and <code>burstcount</code> during burst transfers. The Avalon Interface Specification states: "The start of a write burst is similar to the start of a fundamental master write transfer. The master port asserts <code>address</code> , <code>writedata</code> , <code>write</code> , and <code>byteenable</code> (if present) in addition to <code>burstcount</code> . ... This is the only time that the Avalon switch fabric captures <code>burstcount</code> and <code>address</code> ; the master port can deassert them through the remainder of the burst."	During Avalon master transfers, assert constant values on <code>address</code> and <code>burstcount</code> for the duration of the burst.
If multiple masters control a slave that asserts <code>endofpacket</code> , both masters will see the asserted <code>endofpacket</code> . This may cause problems in systems where masters take action upon <code>endofpacket</code> .	Use <code>endofpacket</code> only in the case that a single master of the asserting slave will take action on the <code>endofpacket</code> .
<b>Version 5.1 SP2 and earlier</b>	
Back-to-back burst transfers from a master to a slave that has a different burst count or bandwidth may fail.	Wait until the slave has finished the read burst before starting a write burst.
Under some circumstances, the automatic addressing feature does not function correctly.	Assign the base address for the component manually.

<b>Issue</b>	<b>Workaround</b>
The setting of the <b>Dual-Port Access</b> option, in the Legacy On-Chip Memory wizard is always shown as “Off” regardless of setting.	Always set the <b>Dual-Port Access</b> option to your desired setting before clicking <b>Finish</b> in the wizard.
Under some circumstances, the SOPC Builder does not display correctly on systems in which the graphics card uses hardware acceleration.	Turn off, or reduce the level of hardware acceleration.
In SOPC Builder, Avalon Masters that address more than 32 bits of slave address space do not issue warning.	Redesign your system to avoid giving masters greater than 32 bits of address space.
SOPC Builder fails to open on UNIX when invoked from the <b>MegaWizard Plug-In Manager</b> .	Open SOPC Builder by clicking <b>SOPC Builder</b> on the Quartus II Tools menu.
You may see random display errors, such as streaks and blotches, in the SOPC Builder GUI.	Lower the <b>Hardware Acceleration</b> setting on the <b>Troubleshooting</b> tab of the <b>Advanced Display Settings</b> dialog box in your <b>Display Settings</b> control panel. There is a known incompatibility between the current Java Runtime Environment (JRE) and certain laptop graphics drivers.
When creating a component with the SOPC Builder Component Editor, you must not choose a component name that exactly matches the HDL file name or the top-level module name. If the names are the same, SOPC Builder will generate an error during system generation. This problem will be fixed in a future version of SOPC Builder.	Using the SOPC Builder Component Editor, rename the component to a different name. In the SOPC Builder table of active components, add the newly-named component to your system, and delete the old component.
If the Quartus II software is installed in a directory that has space characters in its name, the SOPC Builder software will not run.	Install the Quartus II software in a directory that does not have space characters in the path.
The SOPC Builder and Nios II Software Development Kit shell may “hang” and become unresponsive if you run either program while the Frisk antivirus software is running.	Turn off the Dynamic Virus Checking feature of the Frisk software before running SOPC Builder or the Nios II SDK shell.

## EDA Integration Issues

Issue	Workaround
<b>Version 6.1</b>	
<p>If there are virtual I/O pin assignments at the time of generating board-level timing files in the STAMP format, and if there is any other tool or format selected in any EDA tool category on the <b>EDA Tool Settings</b> page, you may receive an error when you run the EDA Netlist Writer.</p>	<p>If the design has virtual I/O pin assignments, and you want to generate board-level timing files in the STAMP format, then either remove the virtual I/O pin assignments from the Quartus II Settings File (.qsf) and recompile the design, or make sure the following is true before running quartus_eda: All tool and format settings in all categories are set to None with the exception of Board-Level timing analysis tool category. STAMP is selected as the EDA format in the Board-Level Timing Analysis tool category in the Board-Level page under EDA Tool Settings.</p> <p>Or, you can run</p> <pre>quartus_eda --format=stamp --board_timing &lt;project&gt; -c &lt;revision&gt;</pre>
<p>Active-HDL 7.1SP2 is unable to compile VHDL simulation model file <b>altera_mf.vhd</b>.</p>	<p>Contact Aldec and request the patch with the fix to this issue.</p>
<p>Conformal reports register mismatches when Formal Verification is run on HardCopy II designs. During design compilation, buffers inserted close to the black box boundary can create two or more logically equivalent output ports on the Revised side black box. This results in mismatches between the Golden and Revised black boxes (BBOXs) and non-equivalence of registers (DFFs) that are downstream from the black boxes.</p>	<p>The extra equivalent output ports in the netlist, created by buffer insertion, are named <code>unassoc_output []</code>, while the original port retains its name. Manually check that the mismatched points in the logic cone of the DFF on the Golden and Revised sides (that is, the non-corresponding support) are in fact equivalent, by comparing the name of the wire connected to the <code>unassoc_output</code> of the black box on the Revised side with the port on the Golden side.</p>
<b>Version 6.0</b>	
<p>When using Formal Verification, if you recompile the design without changing the source files, the Formal Verification database generated by the Quartus II software will not contain information about Quartus II synthesis optimizations. This can lead to mismatches and/or other issues in the Formal Verification tool.</p>	<p>Delete the <code>&lt;project&gt;\db</code> directory and recompile the design.</p>

Issue	Workaround
The ModelSim software may fail to simulate a design if <b>Glitch Filtering</b> is turned on in the EDA Simulation Settings page and the <code>+nospecify</code> option is passed to the ModelSim <code>vsim</code> command.	Remove the <code>+nospecify</code> option from the ModelSim <code>vsim</code> command.
If you add or change a component in a Library Mapping File ( <b>.lmf</b> ), the Quartus II software does not recognize the changes upon the next compilation.	Delete the project database ( <b>db</b> ) directory and recompile.
Running a simulation using NC-Sim version 5.5 or later with files generated with the Quartus II software version earlier than 6.0 causes you to receive the following warning message from ncelaboration: “ncelab: *W,CUNOTB: component instance is not fully bound”	Add the <code>-relax</code> or <code>-lib_binding</code> option to your elaboration command.
<b>Version 5.1 SP2 and earlier</b>	
Timing simulation with the Synopsys VCS MX software is not supported in the Quartus II software versions 5.1 and later.	
You cannot perform RTL simulation of the SerialLite and RLDRAM IP MegaCores in 3 <sup>rd</sup> party simulators using the NativeLink integration feature.	Perform simulation manually as described in the User Guide for the MegaCore you are using.
FIFO Partitioner instances can only be simulated in 3 <sup>rd</sup> party simulators using the original VHDL source files from the <b>quartus/libraries/megafunctions/</b> directory, and NativeLink integration is not supported.	Perform simulation manually as described in the FIFO Partitioner User Guide available from the Literature page of the Altera web site.
The current version of the Quartus II software allows you to select the Synplicity Amplify software as a physical optimization tool. However, this setting is for an automated mode called ATOPS, which is currently not supported by the Amplify software.	Contact Synplicity for the support schedule for the Amplify software ATOPS mode.
NativeLink support does not work with versions of Mentor Graphics Precision RTL Synthesis Software earlier than version 2003b due to a change in the Precision project interface.	

## Simulation Model Changes

### altera\_mf Models

Model	Changes
<b>altsyncram</b>	Read during write mode on the same address by different ports: the CE signal on the write port will be checked to determine whether it is a valid write cycle, and the read port will read according to the setting of <code>read_during_write_mode_mixed_ports</code> , or else it will read out the memory content at the read address.
<b>altsyncram,</b> <b>altdpram</b>	Added support for Stratix III devices.
<b>scfifo,</b> <b>dcfifo</b>	Added support for Stratix III devices.
<b>altmult_add,</b> <b>altmult_accum</b>	Added support for Stratix III devices.
<b>dcfifo</b>	The reduced latency version on <code>wrempty</code> and <code>rdfull</code> flag is now available for <code>sync_delaypipe &gt;= 2</code> . Only available for Stratix II, Cyclone II, Hardcopy II, Stratix II GX, and Stratix III devices.
<b>dcfifo_mixed_widths</b>	New model in Quartus II 6.1 to support different read and write widths. Supported Stratix II, Stratix III, Cyclone II, Hardcopy II, and Stratix II GX devices.
<b>altlvds_rx,</b> <b>altlvds_tx</b>	Added support for Stratix III LVDS receiver and transmitter.
<b>altlvds_rx</b>	Added simulation only parameter “ <code>x_on_bitslip</code> ” to control whether the corrupted bits should be displayed as ‘X’ in the output.
<b>altlvds_tx</b>	Added new parameter “ <code>outclock_duty_cycle</code> ” to specify the duty cycle for output clock of flexible LVDS. Added new output clock divide factor for x6 and x10 mode of flexible LVDS.
<b>altpll</b>	Added support for Stratix III devices.
<b>altddio_in,</b> <b>altddio_out,</b> <b>altddio_bidir</b>	Added new input ports “ <code>sclr</code> ” and “ <code>sset</code> ”. Added new output ports “ <code>oe_out</code> ” for <code>altddio_out</code> and <code>altddio_bidir</code> , which shows the oe input (or registered oe input) that feeds the tri-state used in the megafunction.
<b>altfp_mult</b>	Added new parameter “ <code>denormal_support</code> ” to specify whether to take in denormal input as zero input and output denormal results as zero result.

## Altera\_primitives

<i>Model</i>	<i>Changes</i>
alt_inbuf_diff alt_outbuf_diff alt_outbuf_tri_diff alt_iobuf_diff alt_bidir_diff	New primitives in Quartus II 6.1 Available for Stratix III devices only.
dffeas	Added timing path to support timing simulation with delays. Added new parameter “power_up” to specify the power up value of the register.

## Notes

- Simulation PLI function `convert_hex2ver.dll` has been replaced by Verilog task `convert_hex2ver`, located under `ALTERA_MF.V` library.
- Additional Note : `convert_hex2ver.dll` and its sources files are no longer available in the `quartus/eda/<cadence/mentor/synopsys>` directory.
- RAM megafunction models support only HEX format for all other EDA simulators. Manually convert MIF format to HEX first in the Quartus II software.
- Major changes on Altera primitives simulation models since Quartus II 5.1:
  - Added new primitives `clklock`, `TRI`, `lut_input`, `lut_output`, `dff`, `dffe`, `srff`, `srffe`, `jkff`, `jkffe`, `tff`, `tffe`, `latch`, `alt_inbuf`, `alt_iobuf`, `alt_outbuf` & `alt_out_buf_tri`.
  - All new and existing primitives have been reallocated to new `altera_primitives` library.
  - `Altera_primitives.v(hd)` & `altera_primitives_components.vhd` are located under `quartus\eda\sim_lib\`.
  - Only `LCELL` primitive still remain in `altera_mf` library.

## Latest Known Quartus II Software Issues

For more information about known software issues please look for information in the **Quartus II Software Support** page at the following URL:

<http://www.altera.com/support/software/sof-quartus.html>

## Software Issues Resolved

This section list the numbers of the Customer Service Requests that were fixed or otherwise resolved in this version of the Quartus II software.

Customer Service Request Numbers Resolved in this Release				
10003223	10217451	10221881	10263477	10308899
10367572	10400600	10411310	10413158	10419904
10422568	10437750	10450380	10461020	10463248
10472000	10478862	10483864	10484555	10485851
10486196	10487820	10489187	10491332	10492795
10492851	10493763	10495118	10498026	10498791
10499761	10502476	10502521	10502731	10505103
10505497	10505743	10509950	10510062	10510280
10510645	10510919	10511222	10512034	10512274
10513103	10514159	10514393	10515630	10515641
10515649	10516059	10516180	10516252	10516720
10517381	10517599	10517722	10518935	10519057
10519242	10519589	10520168	10520608	10521025
10521030	10521215	10521250	10521997	10522520
10523054	10523478	10523858	10523884	10523992
10524276	10524392	10524504	10524757	10524918
10525129	10525348	10525368	10525575	10525610
10525831	10526013	10526159	10526472	10526702
10526746	10526804	10526992	10526996	10527445
10527679	10528268	10528277	10528595	10528921
10529295	10529639	10529852	10529926	10530139
10530180	10530492	10530521	10531097	10531583
10531770	10531828	10532116	10532219	10533252
10533481	10533570	10533826	10533826	10534108
10534332	10534492	10534655	10534668	10534866
10535234	10535354	10535419	10535540	10535549
10535748	10535827	10535904	10536369	10537061
10537163	10537191	10537240	10537326	10537343

<b>Customer Service Request Numbers Resolved in this Release</b>				
10537381	10537455	10537862	10538257	10538270
10538408	10538503	10538710	10538764	10538777
10538991	10539212	10539287	10539287	10539629
10539643	10539752	10539765	10539766	10539870
10539908	10539985	10540031	10540509	10540546
10540549	10540637	10541356	10541471	10541509
10541522	10541803	10542007	10541855	10541670
10542039	10542207	10542241	10545599	10542286
10542516	10542660	10542761	10542870	10543139
10543233	10543304	10543462	10543499	10543526
10543733	10543758	10544087	10544152	10544188
10544485	10544501	10544656	10544873	10544874
10544875	10544887	10544900	10544908	10544925
10545041	10545361	10545518	10545687	10545772
10545909	10545949	10545960	10545983	10546174
10546222	10546292	10546325	10546452	10546515
10546565	10546704	10546725	10546877	10546892
10547016	10547023	10547054	10547097	10547322
10547582	10547636	10547642	10547645	10547723
10547860	10547921	10547962	10548133	10548195
10548208	10548209	10548450	10548465	10548579
10548582	10548654	10548724	10548750	10548789
10548795	10548926	10549020	10549071	10549187
10549208	10549209	10549276	10549287	10549306
10549343	10549455	10549463	10549470	10549569
10549640	10549682	10549766	10549866	10549871
10549872	10549908	10549944	10550035	10550095
10550117	10550153	10550287	10550381	10550451
10550455	10550468	10550534	10550633	10550801
10550911	10551244	10551337	10551355	10551362
10551365	10551428	10551482	10551503	10551690
10551813	10551832	10551845	10551874	10551910
10552023	10552055	10552056	10552100	10552146
10552177	10552192	10552244	10552339	10552390
10552449	10552503	10552513	10552517	10552519
10552534	10552547	10552662	10552698	10552726
10552779	10552801	10552826	10552827	10552923
10552926	10553040	10553233	10553267	10553407
10553454	10553567	10553781	10553886	10553938
10553967	10554017	10554084	10554099	10554120
10554153	10554155	10554207	10554231	10554282

<b>Customer Service Request Numbers Resolved in this Release</b>				
10554487	10554574	10554691	10554832	10554888
10554912	10554931	10554984	10555016	10555222
10555268	10555359	10555378	10555383	10555477
10555487	10555497	10555521	10555605	10555673
10555723	10555727	10555792	10555897	10556177
10556206	10556245	10556277	10556282	10556315
10556442	10556576	10556622	10556731	10556784
10556873	10556933	10556946	10556957	10557052
10557071	10557079	10557131	10557159	10557179
10557180	10557201	10557273	10557283	10557292
10557309	10557329	10557434	10557596	10557606
10557848	10557869	10557879	10558131	10558234
10558235	10558294	10558402	10558533	10558539
10558553	10558731	10558888	10558916	10558971
10559004	10559093	10559288	10559352	10559557
10559594	10559647	10559808	10559918	10559921
10559990	10560068	10560076	10560223	10560235
10560310	10560603	10560613	10560843	10560855
10560952	10560983	10561064	10561141	10561203
10561221	10561225	10561280	10561319	10561638
10561726	10561748	10561914	10561962	10562028
10562282	10562321	10562499	10562623	10562901
10562909	10563167	10563215	10563223	10563470
10563479	10563848	10563969	10564055	10564078
10564353	10564681	10564827	10564991	10565074
10565278	10565301	10565465	10565688	10565725
10567672	10567785	10567785	10567934	10569057
10569786				

## Revision History

Revision	Description
1.0	Initial Release

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