



Quartus II Device Support Release Notes

December 2006

Quartus II version 6.1

This document provides late-breaking information about device support in this version of the Altera® Quartus® II software. For information about memory, disk space, and system requirements, refer to the **readme.txt** file in your `\altera\quartus<version number>` directory. For information about New Features, EDA Tool version support, and existing and resolved software issues, refer to the *Quartus II Software Release Notes*.

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Device Support & Pin-Out Status

This section contains information about the status of support in the Quartus II software for the devices listed.

Full Device Support

Full compilation, simulation, timing analysis, and programming support is now available for the following new devices and device packages:

Devices with Full Support

Device Family	Devices	
Stratix® II GX	EP2SGX30CF780	EP2SGX30DF780
	EP2SGX60CF780	EP2SGX60DF780
	EP2SGX60EF1152	EP2SGX130GF1508
HardCopy® II	HC240F1020	HC240F1508

Advance Device Support

Compilation, simulation, and timing analysis support is provided for the following devices that will be released in the near future. Although the Compiler generates pin-out information for these devices, it does not generate programming files for them in this release.

Devices with Advance Support

Device Family	Devices	
Stratix III	EP3SE50	EP3SL70
	EP3SE110	EP3SL150
	EP3SL200	EP3SE260
	EP3SL340	
HardCopy II	HC210WF484	

Timing Models

This section contains a summary of timing model status in the current version of the Quartus II software.

Preliminary Timing Models

The following table shows the devices with preliminary timing models in the current version of the Quartus II software:

Devices with Preliminary Timing Models

Device Family	Device	
HardCopy II	HC210	HC210W
	HC220	HC230
	HC240	
Stratix II GX	EP2SGX30	EP2SGX60
Stratix III	EP3SE50	EP3SL70
	EP3SE110	EP3SL150
	EP3SL200	EP3SE260
	EP3SL340	

Final Timing Models

The following table lists the devices with final timing models that are available in the current version of the Quartus II software:

Devices with Final Timing Models

Device Family	Device	Timing Models Final in Quartus II Version Number
Cyclone® II	EP2C5	6.0
	EP2C8	5.1 SP2
	EP2C20	5.1 SP2
	EP2C35	5.1 SP2
	EP2C50	6.0
	EP2C70	5.1 SP2
MAX® II	EPM240	5.0
	EPM1270	5.0
	EPM570	5.0 SP1
	EPM2210	5.0 SP1
Stratix	EP1S10	4.1
	EP1S20	4.1
	EP1S25	4.1
	EP1S30	4.1
	EP1S40	4.1
	EP1S60	4.1
	EP1S80	4.1
Stratix II	EP2S15	5.0 SP1
	EP2S30	5.0
	EP2S60	5.0
	EP2S90	5.0 SP1
	EP2S130	5.0 SP1
	EP2S180	5.1
Stratix GX	EP1SGX10	4.1
	EP1SGX25	4.1
	EP1SGX40	4.1
Stratix II GX	EP2SGX90	6.1
	EP2SGX130	6.1

The current version of the Quartus II software also includes final timing models for the ACEX® 1K, APEX® 20K, APEX 20KE, APEX 20KC, APEX II, Cyclone, FLEX® 6000, FLEX 10K, FLEX 10KA, FLEX 10KE, and MAX 7000S device families. Timing models for these device families became final in versions earlier than version 4.0.

Power Models

This section contains a summary of power model status for recent devices in the current version of the Quartus II software.

Device Family	Power Model Status
Stratix	Final – 5.1
Stratix GX	Final – 5.1
Stratix II	Final – 6.0
Stratix II GX	Preliminary
Stratix III	Preliminary
Cyclone	Final – 5.1
Cyclone II	Final – 6.0
MAX 3000A	Final – 5.1
MAX 7000AE	Final – 5.1
MAX 7000B	Final – 5.1
MAX II	Final – 5.0 SP1
HardCopy II	Preliminary

Changes in Device Support

All Families

Incorrect Mapping of Output Bits of altlvds_rx Megafunction

The altlvds_rx megafunction produced incorrect mapping of its output bits when the deserialization factor was set to 2. This issue affected all device families that support this megafunction. You must recompile your design with the Quartus II software version 6.1 or later to correct this problem.

Input Delay Chains Not Set Correctly for Input Pins

If you are using the Classic Timing Analyzer and use the INPUT_MIN_DELAY or OUTPUT_MIN_DELAY timing assignments, those assignments won't be used for I/O hold time analysis if the **Optimize hold timing** option is set to "I/O Paths and Minimum TPD Paths". To cause those assignments to be honored for I/O hold time analysis, you must set the **Optimize hold timing** option to "All paths."

MAX II, Stratix II & Cyclone II Device Families

Power Reporting Change for MAX II, Cyclone II, and Stratix II Power Models

A minor change has been made to the power breakdown between **I/O power** and **Core power** in the PowerPlay Power Analyzer report. The total power dissipated on the device and the total current drawn from each voltage supply are unaffected. I/O routing power refers to the power dissipated by device core routing resources that are driven by input I/O cells. In the Quartus II software versions 6.0 and 6.0 SP1, I/O routing power was reported on the PowerPlay[®] Power Analyzer Summary report section as I/O power rather than core dynamic power.

For a typical design, the net change is a change of less than 2% of power from **I/O Power** to **Core Dynamic Thermal Power Dissipation** in the Summary report section of the PowerPlay Power Analyzer. Also, the Core Dynamic Thermal Power Dissipation by Clock Domain report section did not enumerate the I/O routing power.

Inaccuracy in Junction Temperature Used for Power Analysis

Previous versions of the Quartus II software could have a small inaccuracy in the junction temperature used for power analysis when the **Auto-compute junction temperature from cooling solution** option was used. Version 6.1 of the Quartus II software corrects that inaccuracy.

Under the worst possible conditions, the error in the calculated junction temperature was less than 1.5° C, and the typical error was much smaller. There is no change in reported power compared to the results reported by the Quartus II Version 6.0 when a fixed junction temperature is used.

This issue affects the following families with Final power models: Stratix II, Cyclone II, MAX II.

Stratix II, Stratix II GX & HardCopy II Device Families

PLL Lock Circuit Errors Due to High Compensation Variability

The lock circuit in Stratix II, Stratix II GX, and HardCopy II PLLs may fail for PLL settings that use very low M counter values. Specifically, all settings with M=1 or M=2, or settings with M=3, 4, 5 where the charge-pump-current is 12uA or 30uA (see errata for a detailed description). Versions of the Quartus II software prior to 6.1 may have picked such illegal settings, mostly for applications requiring very high PLL input clock frequencies. Starting in version 6.1 of the Quartus II software, the software will no longer pick these illegal settings. If a PLL was generated using the normal `altpll` MegaWizard flow in an older version of the Quartus II software, then when recompiling with the Quartus II software version 6.1, the software will automatically pick a new legal setting. If a PLL was generated using advanced parameters and used one of the illegal settings, then it should be manually updated to use one of the legal settings (e.g., by opening the instantiation in the `altpll` MegaWizard and re-generating the PLL instantiation). If the instantiation is not updated, the Quartus II software will give a critical warning for any illegal settings stating that it “can't achieve optimal bandwidth settings”.

Updated Differential HSTL / SSTL I/O Power Models

This version of the Quartus II software contains updated power models of differential HSTL and SSTL I/O standards when configured as an output or bidir and driven by one of four enhanced PLLs or one of 36 DQS pins. This update

affects power models for the Stratix II, Stratix II GX, and HardCopy II device families.

Stratix II & Stratix II GX Device Families

LVDS Sampling Window FPLL Delay Bits Settings

In the Quartus II software version 5.1, the sampling window for the Stratix II LVDS receiver was optimized based on characterization data. However, there was an issue in which one of the settings was set incorrectly which could result in a reduction of margin where the sampling clock is not in the center of the data window and could be off by approximately 80 ps. This issue was resolved in the Quartus II software version 6.1. Designs created in versions of the Quartus II software earlier than v6.1 will use the new settings automatically when compiled using version 6.1. This issue affects all Stratix II and Stratix II GX designs that use an `altlvds` receiver. However, designs that use Dynamic Phase Alignment (DPA) are not affected because with DPA the LVDS receiver automatically chooses the optimal clock phase.

Enhanced PLL Clock Switchover for Industrial Grade Devices

Versions of the Quartus II software prior to 6.1 gave a warning indicating that the Enhanced PLL's clock switchover feature may not work at Industrial temperatures in Stratix II and Stratix II GX devices. However, after further detailed characterization, these features have been shown to work at industrial temperatures. As a result, the Quartus II software version 6.1 will no longer issue a warning for designs using clock switchover in an Industrial grade device.

Differential I/O and Dynamic Phase Alignment

This issue affects Stratix II GX and Stratix II devices using differential I/O standards with Dynamic Phase Alignment circuitry. Versions of the Quartus II software prior to 6.1 did not allow you to place single-ended output pins inside a bank that also used DPA. Starting with version 6.1 of the Quartus II software, this restriction is relaxed so that single-ended outputs are now allowed inside the DPA bank so long as total drive-strength of these single-ended outputs or bidir pins does not exceed 120 mA.

Stratix II GX Device Family

Stratix II GX Power Pins Identified by Quad

The power supply pins for the Stratix II transceiver PLLs are identified by quad number beginning in version 6.1 of the Quartus II software. The pins are now labeled VCCL_B [17...13] instead of just VCCL.

V_{OD} Setting Too Low When Using alt2gxb MegaWizard

When using the MegaWizard Plug-in Manager to configure the alt2gxb megafunction for PCI Express, the preset value for V_{OD} in the **TX Analog** tab was set too low. In the Quartus II software version 6.1, the value has been increased to 960 mV from the previous setting of 800 mV.

Increase Maximum Data Rate in Stratix II GX Transceivers

The maximum data rate limit for Basic configurations of Stratix II GX Receivers and Transmitters that use the single width deserializer data path, bit slipping circuitry, and the byte deserializer has been raised from 2.5 Gbps to 3.125 Gbps. This change does not affect existing designs.

Add Support for Lower Data Rates

The minimum data rate limit for Basic configurations of Stratix II GX receivers and transmitters that use the double width deserializer data path has been reduced from 3.125 Gbps to 1 Gbps. The absolute minimum data rate limit for any configuration of Stratix II GX receivers and transmitters has been reduced from 622 Mbps to 600 Mbps. This change does not affect existing designs.

Stratix II GX -5 Speed Grade Data Rate Limit Increase

The maximum data rate limit for Stratix II GX receivers and transmitters in -5 speed grades has been raised from 3.125 Gbps to 4.25 Gbps. This change does not affect existing designs.

Incorrect Voltages Shown in Pin-Out File for Stratix II GX I/O Banks

If you turned on Physical Synthesis for a design in a Stratix II GX device, versions of the Quartus II software prior to version 6.1 incorrectly listed the voltage of the GXB I/O Banks as 3.3 V instead of the correct value of 1.2 or 1.5 V in the table at the beginning of the Pin-Out file (.pin). The specific VCC pins for the GXB blocks (VCCA, VCCP, VCCR, VCCT, and VCCH) are reported correctly. The error existed only in the summary table at the beginning of the file.

Incorrect Pin Labeling in Pin-Out File for Stratix II GX GND Pins

In the Quartus II software prior to version 6.1, the HSSL_VSS and VSSGXB pins are labeled in the Pin-out file as GND*, which indicates that they can remain unconnected. The pins should have been labeled GND, which indicates that they must be connected to ground.

Incorrect Configuration of Rate Matching Block

For Stratix II GX Receivers using the double width deserializer data path and the rate matching block, the rate matching blocks rate matching pattern was incorrectly configured. This issue has been solved in the Quartus II software version 6.1. If your design has GXB Receivers using the double width deserializer data path and the rate matching block, you must regenerate your `alt2gxb` megafunction using the `alt2gxb` MegaWizard in the Quartus II software version 6.1.

Minimum Reference Clock Frequency Reduced

The minimum reference clock frequency to Stratix II GX GXB transmitter PLLs (`pll_inclk`) and receivers (`rx_cruclk`) has been lowered from 62.2 MHz to 50 MHz. This change does not affect existing designs.

SONET OC-48 Word Alignment Pattern Change

This issue affects Stratix II GXB configurations using the SONET OC-48 protocol. Versions of the Quartus II software prior to 6.1 incorrectly configured the byte ordering pattern when the **Flip word alignment pattern bits** option in the `alt2gxb` Megafunction was turned off. If your SONET OC-48 configuration has the **Flip word alignment pattern bits** option turned off, you must regenerate your `alt2gxb` Megafunction instance using the `alt2gxb` MegaWizard in the Quartus II software version 6.1.

HSPICE Writer Support Added

This version of the Quartus II software adds HSPICE Writer support for single-ended and differential output buffers in the Stratix II GX device families. Please see the “Signal Integrity Analysis with Third Party Tools” chapter in the *Quartus II Handbook* on the Altera web site.

Stratix II Device Family

IBIS Models Updated for Stratix II Devices

The Stratix II IBIS models have been updated to improve accuracy and to add three new I/O models:

Differential HSTL-15 OCT 50 ohms

Differential HSTL-18 OCT 25 ohms

Differential HSTL-18 OCT 50 ohms

HardCopy II Device Family

LVDS Receiver Sampling Window Updates for HardCopy II Devices

In the Quartus II software version 6.1, the HardCopy II LVDS receiver sampling window was optimized based on characterization data. The result is that the sampling clock will be centered in the data window. In versions of the Quartus II software prior to 6.1, the settings were based on simulation data and as a result may not yield the most optimal sampling window.

MAX II Device Family

IBIS Models Updated for MAX II Devices

The MAX II IBIS models have been updated to improve accuracy and to add support for MAX II G devices

Cyclone II Device Family

Increased Junction Temperature Range for Cyclone II Industrial Grade Devices

In the Quartus II software version 6.1 and later, you can change the **Junction temperature range** setting for Industrial grade Cyclone II devices from the

default range of –40 to 100 degrees Celsius to an extended range of –40 to 125 degrees Celsius. You can then run the PowerPlay Power Analyzer to analyze power within this extended temperature range. The **Junction temperature range** setting is located on the Temperature page of the Settings dialog box.

Revision History

Revision	Description
1.0	Initial Release

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