



Quartus II Device Support Release Notes

March 2007

Quartus II version 7.0

This document provides late-breaking information about device support in this version of the Altera® Quartus® II software. For information about memory, disk space, and system requirements, refer to the **readme.txt** file in your `\altera\quartus<version number>` directory. For information about New Features, EDA Tool version support, and existing and resolved software issues, refer to the *Quartus II Software Release Notes*.

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Device Support & Pin-Out Status

This section contains information about the status of support in the Quartus II software for the devices listed.

Full Device Support

Full compilation, simulation, timing analysis, and programming support is now available for the following new devices and device packages:

Devices with Full Support

Device Family	Devices	
None		

Advance Device Support

Compilation, simulation, and timing analysis support is provided for the following devices that will be released in the near future. Although the Compiler generates pin-out information for these devices, it does not generate programming files for them in this release.

Devices with Advance Support

Device Family	Devices	
Stratix III	EP3SE50	EP3SL70
	EP3SE110	EP3SL150
	EP3SL200	EP3SE260
	EP3SL340	
Cyclone III	EP3C10	EP3C16
	EP3C25	EP3C40
	EP3C55	EP3C80
	EP3C120	
HardCopy II	HC210WF484	

Timing Models

This section contains a summary of timing model status in the current version of the Quartus II software.

Preliminary Timing Models

The following table shows the devices with preliminary timing models in the current version of the Quartus II software:

Devices with Preliminary Timing Models

Device Family	Device	
HardCopy II	HC210	HC210W
	HC220	HC230
	HC240	
Cyclone III	EP3C10	EP3C16
	EP3C25	EP3C40
	EP3C55	EP3C80
	EP3C120	
Stratix III	EP3SE50	EP3SL70
	EP3SE110	EP3SL150
	EP3SL200	EP3SE260
	EP3SL340	

Final Timing Models

The following table lists the devices with final timing models that are available in the current version of the Quartus II software:

Devices with Final Timing Models

Device Family	Device	Timing Models Final in Quartus II Version Number
Cyclone® II	EP2C5	6.0
	EP2C8	5.1 SP2
	EP2C20	5.1 SP2
	EP2C35	5.1 SP2
	EP2C50	6.0
	EP2C70	5.1 SP2
MAX® II	EPM240	5.0
	EPM1270	5.0
	EPM570	5.0 SP1
	EPM2210	5.0 SP1
Stratix	EP1S10	4.1
	EP1S20	4.1
	EP1S25	4.1
	EP1S30	4.1
	EP1S40	4.1
	EP1S60	4.1
	EP1S80	4.1
Stratix II	EP2S15	5.0 SP1
	EP2S30	5.0
	EP2S60	5.0
	EP2S90	5.0 SP1
	EP2S130	5.0 SP1
	EP2S180	5.1
Stratix GX	EP1SGX10	4.1
	EP1SGX25	4.1
	EP1SGX40	4.1
Stratix II GX	EP2SGX30	7.0
	EP2SGX60	7.0
	EP2SGX90	6.1
	EP2SGX130	6.1

The current version of the Quartus II software also includes final timing models for the ACEX® 1K, APEX® 20K, APEX 20KE, APEX 20KC, APEX II, Cyclone, FLEX® 6000, FLEX 10K, FLEX 10KA, FLEX 10KE, and MAX 7000S device

families. Timing models for these device families became final in versions earlier than version 4.0.

Power Models

This section contains a summary of power model status for recent devices in the current version of the Quartus II software.

Device Family	Power Model Status
Stratix	Final – 5.1
Stratix GX	Final – 5.1
Stratix II	Final – 6.0
Stratix II GX	Preliminary
Stratix III	Preliminary
Cyclone	Final – 5.1
Cyclone II	Final – 6.0
Cyclone III	Preliminary
MAX 3000A	Final – 5.1
MAX 7000AE	Final – 5.1
MAX 7000B	Final – 5.1
MAX II	Final – 5.0 SP1
HardCopy II	Preliminary

Changes in Device Support

Stratix II PLL Auto Reset Feature No Longer Supported

The self-reset feature of the Stratix II PLL was found to malfunction in the device. As a result this feature is no longer supported, and will result in a compilation error. Altera recommends asserting the PLL `areset` signal upon loss of lock to reset the PLL and to maintain the phase relationship between the output clocks.

Quartus II Software Incorrectly Reports VCC Voltage in Stratix II GX Designs

In versions of the Quartus II software earlier than 7.0, the Pin-Out file (`.pin`) incorrectly specifies that VCCA pins be connected to 2.5 V when they should be connected to the 3.3-V supply voltage to operate correctly. This issue affects only Stratix II GX devices and is corrected in the Quartus II software version 7.0 and later.

Final Timing Models for Fast PLLs Changed for all Stratix II and Some Stratix II GX Devices

Fast PLL scan chain frequencies slightly below 100 MHz were flagged as timing violations by the Quartus II Timing Analyzer in previous releases. The Fast PLL scan chain can be operated at up to 100 MHz in all Stratix II devices at all speed grades, and this version of Quartus II updates the Timing analyzer to allow operation at this speed. Because this change increases only the maximum operation frequency of the Fast PLL scan chain, there is no need perform timing analysis upon any design which met timing in a previous version of the Quartus II software. Enhanced PLLs are not affected.

Final timing models affected: Stratix II (all devices) and Stratix II GX (all 2SGX90 and 2SGX130 devices).

Quartus II Software Incorrectly Reports Power for PCI I/O Pins

Previous versions of the Quartus II Power Analyzer did not calculate power for PCI I/Os in MAX II devices. This omission is fixed in version 7.0 of the Quartus II software. Only designs targeting MAX II devices and using PCI I/Os are affected; the net effect for these designs is an increase in the power estimate shown in the Power Analyzer.

Memory Simulation Shows Unknown Value Incorrectly

Version 7.0 of the Quartus II software corrects an issue in the behavioral memory simulation model which causes data port values to be shown as unknown when clock enable signal is inactive during the falling edge of the write clock signal.

Revision History

Revision	Description
1.0	Initial Release

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