



Quartus II Device Support Release Notes

May 2007

Quartus II version 7.1

This document provides late-breaking information about device support in this version of the Altera® Quartus® II software. For information about memory, disk space, and system requirements, refer to the **readme.txt** file in your `\altera\quartus<version number>` directory. For information about New Features, EDA Tool version support, and existing and resolved software issues, refer to the *Quartus II Software Release Notes*.

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Device Support & Pin-Out Status

This section contains information about the status of support in the Quartus II software for the devices listed.

Full Device Support

Full compilation, simulation, timing analysis, and programming support is now available for the following new devices and device packages:

Devices with Full Support

Device Family	Devices	
Cyclone® III	EP3C25F324	EP3C25F256
	EP3C25E144	EP3C25Q240
HardCopy® II	HC210WF484	

Advance Device Support

Compilation, simulation, and timing analysis support is provided for the following devices that will be released in the near future. Although the Compiler generates pin-out information for these devices, it does not generate programming files for them in this release.

Devices with Advance Support

Device Family	Devices	
Arria™ GX ⁽¹⁾	EP1AGX20F780	EP1AGX35F780
	EP1AGX50F1152	EP1AGX50F780
	EP1AGX60F1152	EP1AGX60F780
	EP1AGX90F1152	
Stratix® III ⁽¹⁾	EP3SL50F484	EP3SL50F780
	EP3SE80F780	EP3SE80F1152
	EP3SL110F1152	EP3SL110F1152
Cyclone III	EP3C5E144	EP3C5F256

⁽¹⁾ Pin-out support is not available for Arria GX and Stratix III device families in the current version of the Quartus II software.

Timing Models

This section contains a summary of timing model status in the current version of the Quartus II software.

Preliminary Timing Models

The following table shows the devices with preliminary timing models in the current version of the Quartus II software:

Devices with Preliminary Timing Models

Device Family	Device	
Arria GX	EP1AGX20	EP1AGX35
	EP1AGX50	EP1AGX60
	EP1AGX90	
HardCopy II	HC210	HC210W
	HC220	HC230
	HC240	
Cyclone III	EP3C10	EP3C16
	EP3C25	EP3C40
	EP3C55	EP3C80
	EP3C120	
Stratix III	EP3SE50	EP3SL70
	EP3SE110	EP3SL150
	EP3SL200	EP3SE260
	EP3SL340	

Final Timing Models

The following table lists the devices with final timing models that are available in the current version of the Quartus II software:

Devices with Final Timing Models

Device Family	Device	Timing Models Final in Quartus II Version Number
Cyclone II	EP2C5	6.0
	EP2C8	5.1 SP2
	EP2C20	5.1 SP2
	EP2C35	5.1 SP2
	EP2C50	6.0
	EP2C70	5.1 SP2
MAX [®] II	EPM240	5.0
	EPM1270	5.0
	EPM570	5.0 SP1
	EPM2210	5.0 SP1
Stratix II	EP2S15	5.0 SP1
	EP2S30	5.0
	EP2S60	5.0
	EP2S90	5.0 SP1
	EP2S130	5.0 SP1
	EP2S180	5.1
Stratix II GX	EP2SGX30	7.0
	EP2SGX60	7.0
	EP2SGX90	6.1
	EP2SGX130	6.1

The current version of the Quartus II software also includes final timing models for the ACEX[®] 1K, APEX[®] 20K, APEX 20KE, APEX 20KC, APEX II, Cyclone, FLEX[®] 6000, FLEX 10K, FLEX 10KA, FLEX 10KE, and MAX 7000S, Stratix, and Stratix GX device families. Timing models for these device families became final in versions 4.1 and earlier.

Power Models

This section contains a summary of power model status for recent devices in the current version of the Quartus II software.

Device Family	Power Model Status
Stratix	Final – 5.1
Stratix GX	Final – 5.1
Stratix II	Final – 6.0
Stratix II GX	Final – 7.1
Stratix III	Preliminary
Cyclone	Final – 5.1
Cyclone II	Final – 6.0
Cyclone III	Preliminary
MAX 3000A	Final – 5.1
MAX 7000AE	Final – 5.1
MAX 7000B	Final – 5.1
MAX II	Final – 5.0 SP1
HardCopy II	Preliminary
Arria GX	Preliminary

Changes in Device Support

Changes to SONET/SDH Clock Frequencies

The Quartus II software version 7.0 added support for 77.76 MHz and 155.52 MHz reference clock frequencies for the SONET/SDH protocol. This release adds 622.08 MHz clock frequency. Beginning in version 7.1 of the Quartus II software, the SONET/SDH protocol supports the following clock frequencies: 62.2 MHz, 77.76 MHz, 155.52 MHz, 311.04 MHz and 622.08 MHz.

Applies to: Stratix II GX devices

Additions to Transceiver Configurations in 8-bit Deserialization Datapath

The Quartus II software version 7.1 adds the following two new transceiver configurations in the 8-bit deserialization data path:

- 8-bit deserialization, A1A2/A1A1A2A2-style word alignment. The byte deserialization block and the byte ordering block can be turned on or off in the alt2gxb receiver channel.
- 8-bit deserialization, bit-slipping at the word aligner. The byte deserialization block can be turned on or off in the alt2gxb receiver channel.

These two new transceiver configurations can operate over a range of data rates from 600 Mbps to 2500 Mbps.

Applies to: Stratix II GX devices

Additions to Two Transceiver Configurations in Double-Width Deserialization Mode

The byte deserializer can now be disabled in the following two configurations:

- 20-bit deserialization with manual word alignment and the byte ordering block enabled.
- 16-bit deserialization with bit-slipping at the word aligner.

Applies to: Stratix II GX devices

Change to Double-Width Deserializer Block Width Data Rate and Operating Voltage

The Quartus II software versions 7.0 and earlier limited the use of the double-width deserializer block width to data rates above 3.125 Gbps and required that the operating voltage (VCCHTX) be 1.5-V.

The Quartus II software version 7.1 allows you to use double-width deserializer block width at data rates above 1.0 Gbps. You can select VCCHTX of 1.2-V/1.5-V at data rates from 1.0 Gbps to 3.125 Gbps. You can select VCCHTX of 1.5 V only at data rates above 3.125 Gbps.

Applies to: Stratix II GX devices

Change to Pin-File Naming of GND* Pin

The Quartus II software versions 6.1 and earlier incorrectly reported pin Y4 of the EP2SGX30CF780 and EP2SGX60CF780 devices as GXB_GND. The Quartus II software versions 7.0 and later correctly report this pin as GND*

Applies to: Stratix II GX devices

Change to VOD Setting

Beginning in version 7.1 of the Quartus II software, you cannot set the Voltage Output Differential (VOD) to 160 mV on the TX Analog page of the alt2gxb MegaWizard.

Applies to: Stratix II GX devices

Change to XAUI Configuration Mode

In the Quartus II software version 7.0 and earlier, the rate matching block potentially introduces an extra Start of Packet Column when it should insert characters, corrupting the data packet. This issue is corrected in the Quartus II software version 7.1. Existing designs should be recompiled with the current version of the software.

Applies to: Stratix II GX devices

Revision History

Revision	Description
1.0	Initial Release

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