

Device Support & Pin-Out Status

This section contains information about the status of support in the Quartus II software for the devices listed.

Full Device Support

Full compilation, simulation, timing analysis, and programming support is now available for the following new devices and device packages:

Devices with Full Support

Device Family	Devices	
Arria™ GX	EP1AGX20CF780	EP1AGX35DF780
	EP1AGX50DF780	EP1AGX50DF1152
	EP1AGX60DF780	EP1AGX60EF1152
	EP1AGX90EF1152	
Cyclone® III	EP3C25U256	EP3C120F484
	EP3C120F780	

Advance Device Support

Compilation, simulation, and timing analysis support is provided for the following devices that will be released in the near future. Although the Compiler generates pin-out information for these devices, it does not generate programming files for them in this release.

Devices with Advance Support with Pin-out Support

Device Family	Devices	
Arria GX	EP1AGX20CF484	EP1AGX35CF484
	EP1AGX50CF484	EP1AGX60CF484
Stratix® III	EP3SL50F484	EP3SL50F780
	EP3SE50F484	EP3SE50F780
	EP3SL70F484	EP3SL70F780
	EP3SE80F780	EP3SE80F1152
	EP3SL110F780	EP3SL110F1152
	EP3SE110F780	EP3SE110F1152
	EP3SL150F780	EP3SL150F1152
	EP3SL200F1152	EP3SL200F1517
	EP3SE260F1152	EP3SE260F1517
	EP3SL340F1517	EP3SL340F1760

Device Family	Devices	
Cyclone III	EP3C5U256	EP3C10U256
	EP3C16U256	EP3C16U484
	EP3C40U484	EP3C55U484
	EP3C80U484	

Timing Models

This section contains a summary of timing model status in the current version of the Quartus II software.

Preliminary Timing Models

The following table shows the devices with preliminary timing models in the current version of the Quartus II software:

Devices with Preliminary Timing Models

Device Family	Device	
Arria GX	EP1AGX20	EP1AGX35
	EP1AGX50	EP1AGX60
	EP1AGX90	
HardCopy II	HC210	HC210W
	HC220	HC230
	HC240	
Cyclone III	EP3C10	EP3C16
	EP3C25	EP3C40
	EP3C55	EP3C80
	EP3C120	
Stratix III	EP3SE50	EP3SL50
	EP3SL70	EP3SE80
	EP3SE110	EP3SL110
	EP3SL150	EP3SL200
	EP3SE260	EP3SL340

Final Timing Models

The following table lists the devices with final timing models that are available in the current version of the Quartus II software:

Devices with Final Timing Models

Device Family	Device	Timing Models Final in Quartus II Version Number
Cyclone II	EP2C5	6.0
	EP2C8	5.1 SP2
	EP2C20	5.1 SP2
	EP2C35	5.1 SP2
	EP2C50	6.0
	EP2C70	5.1 SP2
MAX [®] II	EPM240	5.0
	EPM1270	5.0
	EPM570	5.0 SP1
	EPM2210	5.0 SP1
Stratix II	EP2S15	5.0 SP1
	EP2S30	5.0
	EP2S60	5.0
	EP2S90	5.0 SP1
	EP2S130	5.0 SP1
	EP2S180	5.1
Stratix II GX	EP2SGX30	7.0
	EP2SGX60	7.0
	EP2SGX90	6.1
	EP2SGX130	6.1

The current version of the Quartus II software also includes final timing models for the ACEX[®] 1K, APEX[®] 20K, APEX 20KE, APEX 20KC, APEX II, Cyclone, FLEX[®] 6000, FLEX 10K, FLEX 10KA, FLEX 10KE, and MAX 7000S, Stratix, and Stratix GX device families. Timing models for these device families became final in versions 4.1 and earlier.

Power Models

This section contains a summary of power model status for recent devices in the current version of the Quartus II software.

Device Family	Power Model Status
Stratix	Final – 5.1
Stratix GX	Final – 5.1
Stratix II	Final – 6.0
Stratix II GX	Final – 7.1
Stratix III	Preliminary
Cyclone	Final – 5.1
Cyclone II	Final – 6.0
Cyclone III	Preliminary
MAX 3000A	Final – 5.1
MAX 7000AE	Final – 5.1
MAX 7000B	Final – 5.1
MAX II	Final – 5.0 SP1
HardCopy II	Preliminary
Arria GX	Preliminary

Changes in Device Support

Correct program_done Bit in SVF File for MAX II Devices

SVF files created with the Quartus II software version 7.1 for programming MAX II devices are incorrect for MAX II device designs. As a result, devices programmed using those SVF files may not enter user mode after power-up. To correct the problem, create a new SVF file using the Quartus II software version 7.1 SP1. It is not necessary to recompile the design POF file; just create a new SVF file. Refer to the Solution on the Altera website at the following URL: www.altera.com/support/kdb/solutions/rd05072007_743.html

Applies to: MAX II devices

Enhanced Reference Clock for 3G/6G Basic Modes Including SRIO to 125 MHz

The Quartus II software version 7.1 SP1 allows M=25 for all basic modes. This permits a 125 MHz reference clock for a 3.125 Gbps data rate for all basic modes.

Applies to: Stratix II GX and Arria GX devices

Quartus II Pin-out File Changes for Stratix II GX and Arria GX

The Quartus II Pin-out File has been updated to reflect a change in the recommended connections for power pins and unused pins. For transceiver I/O banks (Bank 13, 14, 15, 16 and 17), connect each pin marked GND* either individually through a 10 KOhm resistor to GND or tie all pins together and connect through a single 10 KOhm resistor to GND. For non-transceiver I/O banks, connect each pin marked GND* directly to GND or leave it unconnected. Connect each pin marked GXB_VCC* either individually through a 10 KOhm resistor to VCCT/VCCR (1.2V) or tie all pins together and connect through a single 10 KOhm resistor to VCCT/VCCR (1.2V). Power pins marked VCCH_B [] may be connected to 1.2V or 1.5V.

Applies to: Stratix II GX and Arria GX devices

M and N Counter Value Fixed for altpll_reconfig Megafunction

Designs that use PLL reconfiguration may cause incorrect functionality in hardware even though the design successfully simulates in software. This condition is due to an incorrect mapping used in the PLL reconfiguration scan chain where the M and N counter locations were swapped. Cyclone III designs using PLL reconfiguration created with versions of the Quartus II software earlier than 7.1 SP1 should be updated by regenerating the altpll_reconfig Megafunction instantiations and the accompanying MIF files.

Applies to: Cyclone III devices

Fixed EP3C25 M9K Memory Block Read Issue

Altera has identified a read issue when using M9K memory blocks in Cyclone III EP3C25 devices in a certain configuration. In this case memory reads may produce incorrect data. At the device level, this issue only occurs in True Dual-Port mode, with dual clocks (for Port A and Port B), with dual clock enables, with one clock enable signal connected to VCC in the design, and with a certain register packing. Due to memory packing optimization in the Quartus II software, memory blocks that appear in the user's code as any supported memory mode such as Single-Port Mode or ROM Mode may actually utilize the M9K memory block in True Dual-Port Mode. This issue is caused by incorrect routing of the clock enable signals. You can avoid this issue if you do not use clock enables on any memory in your design. For example, if you use the RAM MegaWizard Plug-In Manager, you must not turn on the **Create one clock enable for each clock signal** option for any memory in the design. You should recompile the design using the Quartus II software version 7.1 SP1 or later.

Applies to: Cyclone III devices

Known Issue: Stratix III Vertical Migration Issue

This issue arises when migrating within the 780-pin package from EP3SE50 / EP3SL50 / EP3SL70 to EP3SE80 / EP3SE110 / EP3SL110 / EP3SL150. Due to missing legality checks in the Quartus II software, if a PLL is locked down to location PLL_B1 and the DLL it is feeding is locked down to location DLL3 (bottom-right), the design will fit on the EP3SE50 / EP3SL50 / EP3SL70 devices but will fail to fit on the EP3SE80 / EP3SE110 / EP3SL110 / EP3SL150 devices. Because the Quartus II software versions 7.1 SP1 and earlier do not perform the necessary checks, you must make pin assignments manually to accommodate the migration. Refer to Table 6-10 (Stratix III Device PLL Availability) and Table 8-7/8-8 (DLL Reference Clock Input) in the Stratix III device handbook to select a valid pair of locations for the PLL and the DLL it is feeding. This issue is corrected in the Quartus II software version 7.2 and later.

Applies to: Stratix III devices

Revision History

Revision	Description
1.0	Initial Release

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