



Quartus II Device Support Release Notes

October 2007

Quartus II version 7.2

This document provides late-breaking information about device support in this version of the Altera® Quartus® II software. For information about memory, disk space, and system requirements, refer to the **readme.txt** file in your `\altera\quartus<version number>` directory. For information about New Features, EDA Tool version support, and existing and resolved software issues, refer to the *Quartus II Software Release Notes*.

Device Support & Pin-Out Status	2
Full Device Support	2
Advance Device Support	2
Timing Models	3
Preliminary Timing Models.....	3
Final Timing Models	4
Power Models	5
Changes in Device Support	6
Change in Timing Models for Stratix II, Stratix II GX, and Arria GX Output Pin t_{CO} Derating.....	6
New Cyclone III Industrial Ordering Codes.....	6
Fixed Intermittent Corruption of Initial Memory Content.....	7
Configuration Voltage Constraint for Cyclone III Devices.....	7
I/O Standards Requiring External Resistor Not Supported on Cyclone III	7

Device Support & Pin-Out Status

This section contains information about the status of support in the Quartus II software for the devices listed.

Full Device Support

Full compilation, simulation, timing analysis, and programming support is now available for the following new devices and device packages:

Devices with Full Support

Device Family	Devices	
Arria™ GX	EP1AGX20CF484	EP1AGX35CF484
	EP1AGX50CF484	EP1AGX60CF484
Cyclone® III	EP3C5E144	EP3C5F256
	EP3C5U256	EP3C10E144
	EP3C10F256	EP3C10U256
	EP3C55F484	EP3C55F780
	EP3C55U484	
Stratix III	EP3SL150F780ES	EP3SL150F1152ES

Advance Device Support

Compilation, simulation, and timing analysis support is provided for the following devices that will be released in the near future. Although the Compiler generates pin-out information for these devices, it does not generate programming files for them in this release.

Devices with Advance Support with Pin-out Support

Device Family	Devices	
Stratix® III	EP3SL200F780	EP3SE260H780
	EP3SL340H1152	

Timing Models

This section contains a summary of timing model status in the current version of the Quartus II software.

Preliminary Timing Models

The following table shows the devices with preliminary timing models in the current version of the Quartus II software:

Devices with Preliminary Timing Models

Device Family	Device	
HardCopy II	HC210	HC210W
	HC220	HC230
	HC240	
Cyclone III	EP3C10	EP3C16
	EP3C25	EP3C40
	EP3C55	EP3C80
	EP3C120	
Stratix III	EP3SE50	EP3SL50
	EP3SL70	EP3SE80
	EP3SE110	EP3SL110
	EP3SL150	EP3SL200
	EP3SE260	EP3SL340

Final Timing Models

The following table lists the devices with final timing models that are available in the current version of the Quartus II software:

Devices with Final Timing Models

Device Family	Device	Timing Models Final in Quartus II Version Number
Arria GX	EP1AGX20	7.2
	EP1AGX35	7.2
	EP1AGX50	7.2
	EP1AGX60	7.2
	EP1AGX90	7.2
Cyclone II	EP2C5	6.0
	EP2C8	5.1 SP2
	EP2C20	5.1 SP2
	EP2C35	5.1 SP2
	EP2C50	6.0
	EP2C70	5.1 SP2
MAX [®] II	EPM240	5.0
	EPM1270	5.0
	EPM570	5.0 SP1
	EPM2210	5.0 SP1
Stratix II	EP2S15	5.0 SP1
	EP2S30	5.0
	EP2S60	5.0
	EP2S90	5.0 SP1
	EP2S130	5.0 SP1
	EP2S180	5.1
Stratix II GX	EP2SGX30	7.0
	EP2SGX60	7.0
	EP2SGX90	6.1
	EP2SGX130	6.1

The current version of the Quartus II software also includes final timing models for the ACEX[®] 1K, APEX[®] 20K, APEX 20KE, APEX 20KC, APEX II, Cyclone, FLEX[®] 6000, FLEX 10K, FLEX 10KA, FLEX 10KE, and MAX 7000S, Stratix, and Stratix GX device families. Timing models for these device families became final in versions 4.1 and earlier.

Power Models

This section contains a summary of power model status for recent devices in the current version of the Quartus II software.

Device Family	Power Model Status
Stratix	Final – 5.1
Stratix GX	Final – 5.1
Stratix II	Final – 6.0
Stratix II GX	Final – 7.1
Stratix III	Preliminary
Cyclone	Final – 5.1
Cyclone II	Final – 6.0
Cyclone III	Preliminary
MAX 3000A	Final – 5.1
MAX 7000AE	Final – 5.1
MAX 7000B	Final – 5.1
MAX II	Final – 5.0 SP1
HardCopy II	Correlated ⁽¹⁾ – 7.2
Arria GX	Final – 7.2

⁽¹⁾ HardCopy II power models are fully correlated to silicon in this release.

Changes in Device Support

Change in Timing Models for Stratix II, Stratix II GX, and Arria GX Output Pin t_{CO} Derating

The timing models for Stratix II, Stratix II GX, and Arria GX devices have been corrected. In previous releases, the output pin t_{CO} derating due to capacitive loading on LVCMOS outputs with Non-Calibrated 50-Ohm termination selected was incorrectly specified as 0. The change in t_{CO} derating in ps per pF of capacitive load is provided in the following table:

Device family*	Stratix II			Stratix II GX			Arria GX
	Speed Grade	-3	-4	-5	-3	-4	
t_{CO} derating (ps/pF)	55	63	64	55	63	64	64

* applies to both commercial and industrial grade devices

Applies to: All Stratix II, Stratix II GX, and Arria GX device families

New Cyclone III Industrial Ordering Codes

The following ordering codes have been added to the Quartus II software to support new Cyclone III devices.

EP3C5E144I7	EP3C5F256I7	EP3C5U256I7
EP3C10E144I7	EP3C10F256I7	EP3C10U256I7
EP3C16E144I7	EP3C16F256I7	EP3C16F484I7
EP3C16U256I7	EP3C16U484I7	EP3C25E144I7
EP3C25F256I7	EP3C25F324I7	EP3C25U256I7
EP3C40F324I7	EP3C40F484I7	EP3C40F780I7
EP3C40U484I7	EP3C55F484I7	EP3C55F780I7
EP3C55U484I7	EP3C80F484I7	EP3C80F780I7
EP3C80U484I7	EP3C120F484I7	EP3C120F780I7

Applies to: Cyclone III device family

Fixed Intermittent Corruption of Initial Memory Content

Corruption of initial memory content may occur in M4K memory blocks when the write enable signal is used and connected directly to VCC, and the clock enable signal is not used. The data corruption occurs immediately after device configuration. This issue is fixed in version 7.2.

Applies to: Cyclone, Cyclone II, Cyclone III, Stratix, Stratix II, Stratix III, Stratix II GX, and Arria GX devices

Configuration Voltage Constraint for Cyclone III Devices

In an Active Serial (AS) configuration scheme, the VCCIO of IOBANK 1 of the Cyclone III device must be 3.3 V. In an Active Parallel (AP) configuration scheme, the VCCIO of IOBANK 1, 6, 7 and 8 must be the same and must be 1.8, 2.5, 3.0 or 3.3V.

Altera recommends that you not use level shifters between a configuration device and the Cyclone III device in any active configuration scheme.

Applies to: Cyclone III devices

I/O Standards Requiring External Resistor Not Supported on Cyclone III

This version of the Quartus II software does not support differential I/O standards requiring external resistor network for Cyclone III on row I/O banks 1, 2, 5 and 6. The affected I/O standards are labeled in the Quartus II software as LVDS_3R, RSDS_1R, RSDS_3R, MINI_LVDS_3R, PPDS_3R.

You can use the I/O standards that do not require external resistors and are labeled in the Quartus II software as LVDS, RSDS, mini-LVDS and PPDS. The I/O standards requiring external resistor network are supported on the column I/O banks.

Applies to: Cyclone III devices

Revision History

Revision	Description
1.0	Initial Release

Copyright © 2007 Altera Corporation. All rights reserved. Altera, The Programmable Solutions Company, the stylized Altera logo, specific device designations and all other words and logos that are identified as trademarks and/or service marks are, unless noted otherwise, the trademarks and service marks of Altera Corporation in the U.S. and other countries. All other product or service names are the property of their respective holders. Altera products are protected under numerous U.S. and foreign patents and pending applications, mask work rights, and copyrights.