



Quartus II Device Support Release Notes

March 2008

Quartus II version 7.2 Service Pack 3

This document provides late-breaking information about device support in this version of the Altera® Quartus® II software. For information about memory, disk space, and system requirements, refer to the **readme.txt** file in your `\altera\quartus<version number>` directory. For information about New Features, EDA Tool version support, and existing and resolved software issues, refer to the *Quartus II Software Release Notes*.

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Device Support & Pin-Out Status

This section contains information about the status of support in the Quartus II software for the devices listed.

Full Device Support

Full compilation, simulation, timing analysis, and programming support is now available for the following new devices and device packages:

Devices with Full Support

Device Family	Devices	
MAX [®] II	EPM240ZM100	
Cyclone [®] II	EP2C5AT144	EP2C5AF256
Cyclone III	EP3C5M164	EP3C10M164
	EP3C16M164	
	EP3C16E144	EP3C16F256
	EP3C16U256	EP3C16F484
	EP3C16U484	EP3C40Q240
	EP3C40F324	EP3C40F484
	EP3C40U484	EP3C40F780
	EP3C80F484	EP3C80U484
	EP3C80F780	
Stratix [®] III	EP3SL50F780	EP3SL50F484
	EP3SL70F780	EP3SL70F484
	EP3SL110F1152	EP3SL110F780
	EP3SL150F1152	EP3SL150F780
	EP3SL200F1152	EP3SL200F1517
	EP3SL200H780	EP3SL340F1517
	EP3SE50F780	EP3SE50F484
	EP3SE80F780	EP3SE110F780
	EP3SE80F1152	EP3SE110F1152
	EP3SL340H1152	
	EP3SL340F1760	EP3SE260F1152
	EP3SE260F1517	EP3SE260H780

Advance Device Support

Compilation, simulation, and timing analysis support is provided for the following devices that will be released in the near future. Although the Compiler generates pin-out information for these devices, it does not generate programming files for them in this release.

Devices with Advance Support with Pin-out Support

Device Family	Devices	
MAX II	EPM240ZM68	EPM570ZM100
	EPM570ZM144	EPM570ZM256

Timing Models

This section contains a summary of timing model status in the current version of the Quartus II software.

Preliminary Timing Models

The following table shows the devices with preliminary timing models in the current version of the Quartus II software:

Devices with Preliminary Timing Models

Device Family	Device	
HardCopy [®] II	HC210	HC210W
	HC220	HC230
	HC240	
Cyclone III	EP3C10	EP3C16
	EP3C40	EP3C55
	EP3C80	
Stratix III	EP3SE50	EP3SL50
	EP3SL70	EP3SE80
	EP3SE110	EP3SL110
	EP3SL150	EP3SL200
	EP3SE260	EP3SL340
MAX II	EPM240Z	EPM570Z

Final Timing Models

The following table lists the devices with final timing models that are available in the current version of the Quartus II software:

Devices with Final Timing Models

Device Family	Device	Timing Models Final in Quartus II Version Number
Arria® GX	EP1AGX20	7.2
	EP1AGX35	7.2
	EP1AGX50	7.2
	EP1AGX60	7.2
	EP1AGX90	7.2
Cyclone II ⁽¹⁾	EP2C5	6.0
	EP2C8	5.1 SP2
	EP2C15	6.0
	EP2C20	5.1 SP2
	EP2C35	5.1 SP2
	EP2C50	6.0
	EP2C70	5.1 SP2
Cyclone III	EP3C25	7.2 SP1
	EP3C120	7.2 SP1
Stratix II	EP2S15	5.0 SP1
	EP2S30	5.0
	EP2S60	5.0
	EP2S90	5.0 SP1
	EP2S130	5.0 SP1
	EP2S180	5.1
Stratix II GX	EP2SGX30	7.0
	EP2SGX60	7.0
	EP2SGX90	6.1
	EP2SGX130	6.1

⁽¹⁾ Automotive (“A”) temperature grade EP2C15 device timing models were preliminary in the Quartus II software version 7.2 SP1.

The current version of the Quartus II software also includes final timing models for the ACEX® 1K, APEX® 20K, APEX 20KE, APEX 20KC, APEX II, Cyclone, FLEX® 6000, FLEX 10K, FLEX 10KA, FLEX 10KE, MAX II, MAX 7000S, Stratix, and Stratix GX device families. Timing models for these device families became final in versions 5.0 and earlier.

Power Models

This section contains a summary of power model status for recent devices in the current version of the Quartus II software.

Device Family	Power Model Status
Stratix	Final – 5.1
Stratix GX	Final – 5.1
Stratix II	Final – 6.0
Stratix II GX	Final – 7.1
Stratix III	Preliminary
Cyclone	Final – 5.1
Cyclone II	Final – 6.0
Cyclone III	Preliminary
MAX 3000A	Final – 5.1
MAX 7000AE	Final – 5.1
MAX 7000B	Final – 5.1
MAX II	Final – 5.0 SP1
HardCopy II	Correlated ⁽¹⁾ – 7.2
Arria GX	Final – 7.2

⁽¹⁾ HardCopy II power models are fully correlated to silicon in this release.

Changes in Device Support

M144K RAM block preliminary timing model change

The Stratix III M144K RAM block timing performance has changed for memory blocks using fast write mode. Fast write mode is used for M144K memories when the Read-During-Write option is set to “Don't Care” or “New Data”. The timing model change does not affect memories using ECC mode or ROM mode or for which the Read-During-Write option is set to “Old Data” or “Old memory contents appear”. To apply the updated timing model for M144K RAM blocks, recompile the design with the Quartus II software version 7.2 SP3.

Applies to: Stratix III ES and production devices

MLAB RAM block size changed from 64x10 or 32x20 (640 bits) to 16x20 (320 bits)

The Stratix III MLAB RAM block size has changed from 64x10 or 32x20 (640 bits) to 16x20 (320 bits) and no longer has native byte enable signals. The MLAB block in ROM mode is not affected and remains at 64x10 or 32x20 (640 bits).

If your design uses MLAB blocks, you must recompile your design with the Quartus II software version 7.2 SP3. The Quartus II software version 7.2 SP3 includes the changes to the MLAB blocks as well as automatic fixes to ensure device functionality when targeting MLAB blocks. To determine whether your design uses MLAB blocks, check the Quartus II Fitter Report.

There are two reasons your design may contain MLAB blocks. The first reason is due to an explicit (hard) assignment to the MLAB block type. This assignment is made either through an EDA synthesis tool or through the Quartus II RAM MegaWizard by setting the block type to MLAB. The second reason your design may contain MLAB blocks is due to a determination that is made at the discretion of the Quartus II software synthesizer or Fitter during compilation. The Quartus II software version 7.2 SP3 will automatically use MLAB blocks in the new configuration when appropriate as well as promote larger RAM blocks to M9K blocks where necessary.

Recompile your design with the Quartus II software version 7.2 SP3.

Applies to: Stratix III ES and production devices

Changes to Cyclone III Timing Models

This timing issue affects only Cyclone III designs. The difference in timing manifests itself when moving from the Quartus II software version 7.2 SP1 to version 7.2 SP2, or version 7.2 SP3.

If your design contains a PLL-generated clock, especially one with a large internal PLL compensation delay (such as the normal mode of the PLL), then any register-to-register transfer within this clock domain exhibits erroneous pessimism of 200 to 400ps (both f_{MAX} and t_H paths) in version 7.2 SP1. The problem is caused by excessive min/max variation introduced into the Cyclone III clock timing models and the absence of a pessimism-removal feature in the TimeQuest timing analyzer (the feature is turned off by default) in the Quartus II software version 7.2 SP1.

Version 7.2 SP2 fixes this problem by removing the unwarranted min/max from the PLL compensation model. The performance of any Cyclone III design compiled in version 7.2 SP2 is correct, and may be better than the performance resulting from compilation in previous versions of the software.

Applies to: Cyclone III devices

Stratix III Cannot Have Calibrated Rt on bidir When OE is Connected to Non-GND but (OCTRT) is Not Connected

- If parallel termination (Rt) is used on a bidir pin, the dynamic termination control for that pin must be connected.
- If the dynamic termination control is connected on an input or bidir pin, then parallel termination (Rt) for that pin must be used.

The Quartus II software will not issue an error or warning if these constraints are violated.

Applies to: Stratix III devices

Changed Transceiver PLL Settings for Stratix II GX and Arria GX Devices

The Quartus II software has updated the CMU PLL loop filter resistor control and charge pump settings used for 3G and 6G basic modes in Stratix II GX devices and 3G basic modes in Arria GX devices. This change improves the CMU PLL performance for some configurations. No design change is needed; the Quartus II software will apply the updated settings during compilation.

Applies to: Stratix II GX and Arria GX devices

New Automotive Temperature Grade Devices Available

The following devices are now available in “A” temperature grade for automotive applications:

- **Cyclone:** EP1C3T100A8, EP1C3T144A8
- **Cyclone II:** EP2C5AF256A7, EP2C5AT144A7, EP2C8AF256A7, EP2C15AF256A7, EP2C15AF484A7, EP2C20AF256A7, EP2C20AF484A7
- **MAX 7000:** EPM7032AETA44-10, EPM7064AETA44-10, EPM7064AETA100-10, EPM7128AETA100-10, EPM7128AETA144-10

- **MAX II:** EPM240T100A5, EPM570T100A5, EPM570T144A5, EPM1270F256A5, EPM1270T144A5, EPM2210F256A5, EPM2210F324A5
- **HardCopy II:** HC210WF484A

Device Specification Change for EP3SL200 Devices

The device specifications for EP3SL200 devices have changed, including resource counts, pin-outs, speed grades and package options. Projects that use EP3SL200 devices should be compiled with the Quartus II software version 7.2 SP1 or later. Updated device specifications are provided in the Stratix III Device Handbook.

Applies to: Stratix III EP3SL200 devices

Incorrect Delay Chain Setting for Cyclone III Devices with DQS Interface

Device characterization has determined that the correct delay chain value for hybrid memory interfaces (i.e., those with multiple DQS pins placed on adjacent sides of the device) should be 0. The Quartus II software version 7.2 and earlier incorrectly set the value to 1. The incorrect setting causes a performance decrease.

To correct the setting, either recompile your design using the Quartus II software version 7.2 SP1 or manually set the delay chain value to 0 with a delay chain assignment in the version 7.2 or earlier software.

Applies to: Cyclone III devices

Incorrect f_{MAX} Reporting for Some Stratix II GX Designs

Designs that targeted the Stratix II GX C5 speed grade, and used the DSP block in 36x36-bit multiply mode and used dynamic control of the signed / unsigned behavior of the multiplier had an overly low f_{MAX} limit in the Quartus II software version 7.2 (197 MHz). The Quartus II software version 7.2 SP1 corrects the f_{MAX} limit for this mode to 305 MHz, which matches the limit in the Quartus II software releases earlier than 7.2.

No design that closed timing in the Quartus II software version 7.2 will be affected by this change, because it can only increase the operating speed of a design. If your design matches the case listed above, and your operating frequency was limited by the DSP block, you should re-run timing analysis in the Quartus II software version 7.2 SP1 to obtain a corrected and less conservative timing report.

Applies to: Stratix II GX devices in C5 grades

User Pin Assignments to PGM Pins Do Not Function Correctly Under Some Circumstances

Programming pins do not function correctly as user I/O pins when remote update is enabled in an Active Serial Configuration scheme. No Compiler warning is issued by the Quartus II software version 7.2 SP1 and earlier.

Applies to: Arria GX, Stratix II, and Stratix II GX device families

Change in Clock Management Unit PLL Multiplication Factors

This change affects the (OIF) CEI PHY interface protocol for Stratix II GX instantiations of the alt2gxb megafunction. In the Quartus II software version 7.2 and earlier, you could specify a data rate to input clock frequency ratio of 10, 20, or 40 when operating in the 4.7–5.7 Gbps range. Beginning in version 7.2 SP1, that ratio can be only 10 or 20.

Applies to: Stratix II GX

Memory Block Power Optimization Change

The ability to use separate clock enable signals for the input clock and the core clock to save power on Stratix III M9K and M144K memory blocks has been temporarily disabled in the Quartus II software version 7.2 SP2. If you are using Quartus II native synthesis, this change is transparent. If you are using a 3rd party EDA synthesis tool, the Quartus II software may generate an error during compilation. Use the MegaWizard Plug-In Manager or your 3rd-party tool to regenerate the netlist and recompile the design in the latest version of the Quartus II software. This change results in an average core dynamic power increase of 1% for designs that use embedded memory.

Applies to: Stratix III

Revision History

Revision	Description
1.0	Initial Release

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