



Quartus II Software Release Notes

July 2008

Quartus II software version 8.0 Service Pack 1

This document provides late-breaking information about the following areas of this version of the Altera® Quartus® II software. For information about memory, disk space, and system requirements, refer to the **readme.txt** file in your `\altera\<version number>\quartus` directory. For information about device support in this version of the Quartus II software, along with the latest information about timing and power models, refer to the *Quartus II Device Support Release Notes* on the Altera website at <http://www.altera.com/literature/lit-qts.jsp>.

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New Features & Enhancements

The Quartus II software version 8.0 SP1 includes full device support for low-voltage devices (C4L and I4L speed grades) for all Stratix III devices.

EDA Interface Information

The current version of the Quartus II software supports the following EDA tools.

Supported EDA Tools

Synthesis Tools	Version	NativeLink Support
Synopsys Synplify & Synplify Pro	9.4	✓
Mentor Graphics Precision RTL Synthesis	2007a update + S4 overlay	✓
Mentor Graphics LeonardoSpectrum	2007b	✓
Synopsys Design Compiler	2004.12-SP4	
Magma Design Automation PALACE	2.4	✓
Agility DK Design Suite	5.0 SP4	
Simulation Tools	Version	NativeLink Support
Mentor Graphics ModelSim	6.1g	✓
Mentor Graphics ModelSim-Altera	6.1g	✓
Cadence NC-Sim (UNIX)	IUS 6.2 (UNIX only)	✓
Synopsys VCS / VCS MX	Y-2006.06- SP1 (UNIX only)	✓
Aldec Active-HDL	7.3	✓
Formal Verification Tools (Equivalence Checking)	Version	NativeLink Support
Cadence Encounter Conformal	7.1	
Chip Level Static Timing Analysis	Version	NativeLink Support
Synopsys PrimeTime	Z-2007.06	✓
Board Level Static Timing Analysis	Version	NativeLink Support
Mentor Graphics TAU	3.7	
Board Level Symbol/Pin-out Management	Version	NativeLink Support
Mentor Graphics I/O Designer	7.3	

Changes to Software Behavior

This section documents instances in which the behavior and default settings of this release of the Quartus II software have been changed from earlier releases of the software.

Items listed in the following table represent cases in which the behavior of the current release of the Quartus II software is different from a previous version.

Description	Workaround
Version 8.0 SP1	
Exporting a Memory Initialization File (.mif or .hex) to a RAM Initialization File (.rif) format is no longer supported in Quartus II software versions 8.0 and later.	

Description	Workaround
Version 8.0	
<p>The ALTMEMPHY megafunction for DDR3 SDDRAM in the Quartus II software version 8.0 has following hardware, compilation, and simulation support.</p> <p>Hardware support:</p> <ul style="list-style-type: none"> • x8 DDR3 SDRAM in UDIMM, SODIMM, and MicroDIMM format • x8 DDR3 SDRAM device support up to and including 80-bit interface widths. DDR3 SDRAM memory interfaces using devices must follow Altera-recommended layout guidelines • Single chip select support • 360MHz to 533MHz full hardware calibration <p>Compilation support:</p> <ul style="list-style-type: none"> • x4 and x8 DDR3 SDRAM device compilation support for pinout checking and timing closure • 300MHz to 533MHz compilation support. Full DDR3 SDRAM interface calibration on hardware is currently supported only using x8 DDR3 SDRAM device-based interfaces between 360MHz and 533MHz <p>Simulation support:</p> <ul style="list-style-type: none"> • Skip calibration simulation mode between 300MHz and 533MHz for x4 and x8 DDR3 SDRAM device based modules • Quick calibration simulation mode between 300MHz and 533MHz for x8 DDR3 SDRAM device-based modules only • Full calibration simulation mode between 360MHz and 533MHz for x8 DDR3 SDRAM device-based modules only 	

Description	Workaround
Version 7.2 SP2	
<p>In the Quartus II software version 7.2 SP2, the SOPC Builder Component Editor properly analyzes a VHDL-based component with generics regardless of the case of the entity (lowercase, capitals, or mixed). In the Quartus II software versions 7.2 and 7.2 SP1, it failed to process VHDL-based components with entity names that were not all lowercase.</p>	
Version 7.2	
<p>The Generate back-annotation data for time closure option in the Design Entry/Synthesis page under EDA Tool Settings in the Settings dialog box is no longer available.</p>	
<p>Constraining cells or routing causes problems for designs ported from the Quartus II software version 7.1 or 7.1 SP1 to the Quartus II software version 7.2, because location assignments to the following block types are incompatible:</p> <p>IOPAD IOIBUF IOOBUF FF DDIOOUTCELL DDIOOCELL PSEUDODIFFOUT CLKCTRL (if specified as X,Y,N instead of as a user string)</p>	<p>To prevent this incompatibility, remove the location assignments and the routing constraints.</p>
<p>For the alt2gxb megafunction, when adaptive equalization is activated for a specific channel, <code>rx_eqctrl</code> writes to that channel do not have any effect.</p>	
<p>In the Quartus II software version 7.2, there is no support for DQSB pins in Arria GX devices, but some Quartus II version 7.2 designs require DQSB pins.</p>	
<p>The Quartus II software no longer supports Synopsys Formality software.</p>	

Description	Workaround
The Quartus II software no longer supports the Synopsys PrimeTime VHDL software.	Use the PrimeTime Verilog software to perform timing analysis for your design. To generate the PrimeTime Verilog files, select Verilog in the Format for output netlist list on the Timing Analysis page under EDA Tool Settings .
The TimeQuest Timing Analyzer supports clock-as-data analysis in the Quartus II software version 7.2, while previous versions of the Quartus II software did not. This results in the TimeQuest analyzer reporting new timing paths where the start point (from node) of the path is a clock node (the target of a create_clock or a create_generated_clock command. The Classic Timing Analyzer does not support clock-as-data analysis.	The behavior, which is correct, is documented in “The Quartus II TimeQuest Timing Analyzer” chapter in the <i>Quartus II Handbook</i> . You may need to modify your constraints to compensate for the clock-as-data analysis support if new timing violations are listed for your design, and you believe these violations are overly conservative for your design.
The functionality of the earlier TimeQuest SDC File Editor has been merged into the main Quartus II Text Editor. The Constraints menu from the earlier TimeQuest SDC File Editor is now located in the Quartus II Text Editor on the Edit menu on the Insert Constraints submenu.	
Starting in the Quartus II software version 7.0, when you use OC-12 with 155.52 Mhz inclock, the alt2gxb megafunction generates a design with incorrect data rate. The incorrect data rate is double of what you designed.	Starting in the Quartus II software version 7.2, when you use the SONET OC-12 protocol with the input clock frequency of 155.52 Mhz, refclk divider is generated by the alt2gxb megafunction in order to obtain the correct data rate.
The TimeQuest Timing Analyzer now performs multicorner timing analysis by default during full compilation. This behavior can be changed in the TimeQuest Timing Analyzer page in the Settings dialog box.	
Version 7.1 SP1	
If you instantiated the alt2gxb megafunction for the (OIF) CEI PHY interface protocol, there is an update that exists that will lower jitter.	To reduce jitter, reopen the existing alt2gxb MegaWizard, and in the General tab, select (OIF) CEI PHY Interface in Which protocol will you be using? The CEI tab appears in the MegaWizard. On the CEI tab, turn on Use central clock divider to improve transmitter jitter .

Description	Workaround
Version 7.1	
<p>When using the SignalTap II Logic Analyzer, if you select a signal to be tapped that cannot be found in the netlist, the Quartus II software will give a critical warning and proceed with compilation. This is a change of behavior from version 6.1 in which compilation would stop with an error message.</p>	<p>To remove the warnings, remove non-existent nodes from the SignalTap II Logic Analyzer. To revert to the behavior of version 6.1 and earlier, you can promote all critical warnings to error messages in the Messages section of the Options dialog box.</p>
<p>The altlvds_tx megafunction shows the actual phase shift of the tx_outclock generated instead of the core clock frequency. This change is only a change in the information that is displayed, and does not change the actual implementation.</p>	
<p>PLLs in Stratix II and Cyclone II devices now have a new parameter, <code>sim_gate_lock_device_behavior</code>, that is OFF by default. This new parameter uses a fixed, internal value of 7 to simulate the gate lock feature. If the value is set to ON, you can simulate the actual device behavior for gated lock using the parameter value <code>gate_lock_counter</code>, as you could in earlier versions of the Quartus II software.</p>	
<p>The Quartus II software version 7.1 Power Analyzer enhances the accuracy of the maximum static power estimate for Stratix II and Stratix II GX devices. The maximum static power drawn from the VCCPD power supply for Stratix II and Stratix II GX devices utilizing maximum power characteristics increases in the Power Analyzer power estimate by at most 15mW (depending on the device size.)</p>	

Description	Workaround
<p>The Quartus II software version 7.1 issues the error:</p> <pre>"Error (10621): VHDL Use Clause error at <location>: more than one Use Clause imports a declaration of simple name "<name>" -- none of the declarations are directly visible."</pre> <p>However, the Quartus II software version 7.0 and earlier did not issue the error for the same design.</p> <p>This changed behavior arises when a design imports overloaded subprograms with the same signature from different packages such as <code>STD_LOGIC_UNSIGNED</code> and <code>STD_LOGIC_SIGNED</code>. Both these packages define binary operations on <code>STD_LOGIC_VECTOR</code> arguments. Earlier versions of the software incorrectly favored the first imported declaration.</p>	<p>Remove one of the conflicting Use Clauses. For example, use either <code>STD_LOGIC_SIGNED</code> or <code>STD_LOGIC_UNSIGNED</code>, but not both.</p>

Description	Workaround
<p>The format for Conversion Setup Files (.cof) has changed. The element defined below (in DTD syntax) has been introduced:</p> <pre data-bbox="251 426 797 785"> <!ELEMENT hex_block (hex_filename,hex_addressing, hex_offset)> <!ELEMENT hex_filename (#PCDATA)> <!ELEMENT hex_addressing (#PCDATA)> <!--hex_addressing value is either relative or absolute --> <!ELEMENT hex_offset (#PCDATA)> </pre> <p>In addition the following elements have been deprecated:</p> <pre data-bbox="251 942 761 1155"> <!ELEMENT bottom_boot_block (bottom_boot_filename,bottom_ addressing)> <!ELEMENT main_block (main_filename, main_addressing)> </pre>	
<p>A key change since SOPC Builder version 7.1 is the new file format for storing system design data. Previously, SOPC Builder used a proprietary file format (PTF) to store system designs, while SOPC Builder version 7.1 uses an industry-standard XML file format for data storage. By convention, these files are given the extension .sopc. When you open an SOPC Builder system created in a previous version of the tools, you are asked to upgrade the system to the new format. Click More Information in that dialog box for details on migrating your projects and the changes in SOPC Builder file formats.</p>	

Description	Workaround
Version 6.1	
<p>A minor change has been made to the power breakdown between I/O power and Core power in the PowerPlay Power Analyzer report. The total power dissipated on the device and the total current drawn from each voltage supply are unaffected. I/O routing power refers to the power dissipated by device core routing resources that are driven by input I/O cells. In Quartus II software versions 6.0 and 6.0 SP1, I/O routing power was reported on the PowerPlay Power Analyzer Summary report section as I/O power rather than core dynamic power. For a typical design, the net change is less than 2% of power from I/O Power to Core Dynamic Thermal Power Dissipation in the Summary report section of the PowerPlay Power Analyzer. Also, the Core Dynamic Thermal Power Dissipation by Clock Domain report section did not enumerate the I/O routing power.</p>	
<p>Designs that contain a user-edited Memory Initialization File (.mif) that compile successfully in earlier versions of the Quartus II software may fail with the error "File <filename>.mif contains illegal syntax at line <num>" in the Quartus II 6.1 software. These Memory Initialization Files contain illegal syntax. Illegal Memory Initialization Files were ignored by previous releases of the software.</p>	<p>Correct the syntax of the Memory Initialization File by referring to the Memory Initialization File syntax description in the Quartus II Help, or create a new Memory Initialization File with the Quartus II software.</p>
Version 6.0 SP1	
<p>In the Quartus II software version 6.0 and earlier, when you created a receiver-only instance of the alt2gxb megafunction, a CMU PLL was created that has pll_inclk and pll_locked ports. These ports prevented the combination of two receiver-only implementations at different data rates in the same quad.</p>	<p>In the Quartus II software version 6.0 SP1, a CMU PLL is no longer created when you create a receiver-only instance. You must recreate the megafunction instance with the MegaWizard Plug-In Manager or manually remove the pll_inclk and pll_locked ports from the wrapper file.</p>

Description	Workaround
Version 6.0	
<p>The TimeQuest Timing Analyzer's QSF2SDC conversion utility cannot properly convert all Classic Timing Analyzer timing assignments. The results from the TimeQuest Timing Analyzer may also be different from the Classic Timing Analyzer due to other default behavior differences.</p>	<p>The QSF2SDC conversion utility is considered a guide to help reduce the time to switch to the TimeQuest analyzer, and it is not intended to make the TimeQuest analyzer a plug-in replacement for the Quartus II Classic Timing Analyzer. You should review all converted SDC constraints for correctness and completeness. Refer to the <i>Switching To the TimeQuest Timing Analyzer</i> chapter in the Quartus II Software Handbook for more information.</p>
<p>For designs that target Stratix II GX devices, that use the alt2gxb megafunction in a transmitter-only configuration, the loop_filter_resistor_control value was not correctly written to the megafunction instance.</p>	<p>Use the MegaWizard Plug-In Manager in the Quartus II software version 6.0 to generate a new instance of the alt2gxb megafunction.</p>
<p>If you created a Verilog Quartus Mapping File (.vqm) for a design containing the alt2gxb megafunction in its XAUI configuration with the Quartus II software version 5.1 SP2 or earlier, the setting for Force Signal Detect was incorrectly set to false.</p>	<p>You should regenerate the alt2gxb instantiation in a XAUI configuration using the Quartus II software version 6.0.</p>
<p>Beginning in the 6.0 release, the Quartus II Parallel Flash Loader megafunction (altparallel_flash_loader) erases flash memory blocks before programming them.</p>	<p>No action is required.</p>
<p>Beginning in the 6.0 release, Quartus II integrated synthesis handles bidirectional pins differently. For example if <code>bidir1</code> and <code>bidir2</code> are declared as <code>inouts</code>, the assignment <code>bidir1 <= bidir2</code> creates a directional connection in which data flows from <code>bidir2</code> to <code>bidir1</code>. In the Quartus II software version 5.1 and earlier, a bidirectional connection was created.</p>	<p>If your design requires that data flow in both directions, you must directly connect the bidirectional pins together without using an assignment statement. Assignment statements always produce a unidirectional data flow.</p>

Description	Workaround
<p>The method the Quartus II NativeLink interface uses to locate other EDA tools changed in this release. You might receive a message indicating that the tool cannot be found when you launch it through the NativeLink interface.</p>	<p>You must specify the path to the EDA tool program file on the EDA Tool Options page of the Options dialog box, or with the <code>set_user_command</code> Tcl command.</p>
<p>Version 5.1 SP2 and earlier</p>	
<p>The following primitives now use a new library instead of the altera_mf library:</p> <p>CARRY CARRY_SUM CASCADE CLKLOCK EXP GLOBAL LUT_INPUT LUT_OUTPUT ROW_GLOBAL TRI SOFT OPNDRN DFF DFFE DFFEAS JKFF JKFFE DFFEAS LATCH SRFF SRFFE TFF TFFE ALT_INBUF ALT_IOBUF ALT_OUTBUF ALT_OUTBUF_TRI</p>	<p>To perform functional simulations in Verilog HDL, you must use the altera_primitives.v library located in the <i><Quartus II installation directory>\eda\sim_lib</i> directory. For VHDL, you must use the altera_primitives.vhd library located in the <i><Quartus II installation directory>\eda\sim_lib</i> directory. The VHDL component declaration file is located in the altera_primitives_components.vhd library in the <i><Quartus II installation directory>\eda\sim_lib</i> directory.</p>
<p>In the Quartus II software version 5.0 and later, you can assign the Allow XOR Gate Usage logic option to individual nodes and entities. In previous versions, you could apply this logic option only to the entire design (that is, it was a global logic option).</p>	

Description	Workaround
<p>The following megafunctions have clear box models that contain assignments that are not stored in the Quartus Settings File (.qsf) and are not written out to a Verilog Quartus Mapping File (.vqm):</p> <ul style="list-style-type: none"> altdqs altdq altddio_bidir altddio_out altddio_input altlvds_rx altlvds_tx altufm_i2c dcfifo alt2gxb_reconfig 	<p>Do not save your atom netlist file as a Verilog Quartus Mapping file if you are using these megafunctions.</p>
<p>When you are using formal verification tools with a design that contains LogicLock regions that was compiled with the Quartus II software version 3.0 or earlier, under certain circumstances when you open the design in the Quartus II software version 4.0 and later, the LogicLock regions will not be handled properly.</p>	<p>Redefine the LogicLock regions in the Quartus II software version 4.0 or later to eliminate the errors.</p>

Known Issues & Workarounds

General Quartus II Software Issues

Issue	Workaround
Version 8.0 SP1	
<p>The State Machine Viewer may not display the state machine correctly if the state machine logic uses the “less than or equal to” operator.</p>	<p>Although the synthesis results will be correct, the State Machine Viewer may not display the state machine correctly if the state machine logic uses the “less than” operator. So if you want to change the display in the State Machine Viewer, you should replace the “less than or equal to” operator in the state machine logic with the “less than” operator and adjust the counter accordingly. For example, the State Machine Viewer may not be able to display the following state logic correctly:</p> <pre data-bbox="824 934 1266 997">If change_state <= 1 then state = new_state;</pre> <p>However, it can correctly handle the following (equivalent) logic:</p> <pre data-bbox="824 1123 1266 1186">If change_state < 2 then state = new_state;</pre>
Version 8.0	
<p>If you compile a project in the command line, and you open the Quartus II software GUI on that project, you may experience unexpected and/or incorrect results.</p>	<p>While compiling a project in the command line, do not open the Quartus II software GUI on that project.</p>
<p>The Open dialog box does not display all files.</p>	<p>Restart the Quartus II software to see all the files.</p>
<p>Creating a new project from the TimeQuest Timing Analyzer GUI can crash the TimeQuest analyzer GUI.</p>	<p>Because the TimeQuest analyzer GUI depends on the open project in the main Quartus II software GUI, create or change projects in the main Quartus II software GUI and not the TimeQuest analyzer GUI.</p>
<p>If you run Analysis & Elaboration after a successful compilation and then run Partition Merge, you may receive an Internal Error or see unexpected behavior due to the loss of assignments.</p>	<p>Run Analysis & Synthesis or run a full compilation before running Partition Merge.</p>

Issue	Workaround
<p>The following error occurs when you manually connected the <code>seriesterminationcontrol</code> and <code>parallelterminationcontrol</code> ports on an output buffer atom, but did not make a termination assignment to the corresponding I/O that uses calibrated on-chip termination: "Output buffer atom <name> has port <name> connected, but does not use calibrated on-chip termination"</p>	<p>Disconnect the <code>seriesterminationcontrol</code> and <code>parallelterminationcontrol</code> ports on the specified output buffer atom, or make an Input Termination or Output Termination assignment to the corresponding pin that uses a value that includes With Calibration.</p>
<p>When you connect the dynamic termination control port on the output buffer of a dedicated output I/O, the error "Output I/O <name> has dynamic termination control connected" occurs in a design with no previous errors.</p>	<p>If the I/O was generated as part of an IP block, regenerate the IP block. If the I/O was user generated, then disconnect the <code>dynamicterminationcontrol</code> port, or connect it to 0 or logical ground.</p>
<p>An error is issued saying that an output is inverted when feeding the <code>dynamicterminationcontrol</code> port of an output buffer atom.</p>	<p>Remove the specified inversion.</p>
<p>If there are Dynamic Termination Control Group assignments to two different I/Os in the design that have different dynamic termination controls but are assigned to the same group, you will receive the following error: "Atoms <name> and <name> are assigned to the same dynamic termination control group, but their dynamic termination controls are not compatible"</p>	<p>Remove all Dynamic Termination Control Group assignments from the design, because they are no longer necessary. If the assignments were created by an IP block, regenerate the block.</p>
<p>The Merged Registers and the Inverter Push-Back Through Register report panels under the Analysis & Synthesis Formal Verification report may be missing or incomplete in the Quartus II software version 8.0.</p>	<p>The information is available in the following two report panels in the Analysis & Synthesis Optimization Results report under Register Statistics:</p> <ul style="list-style-type: none"> • Registers Removed During Synthesis (for merged registers) • Inverted Register Statistics (for inverted registers)

Issue	Workaround
<p>In the Quartus II software version 8.0, I/O primitives do not support exact pin location assignments for designs targeting Cyclone III, Stratix III, and Stratix IV devices. If your design contains I/O primitives with exact pin location assignments, you will see the following error:</p> <pre>The location assignment on the I/O Primitive instance "inst1" specifies an exact pin location</pre>	<p>Instead of using an I/O primitive you can set an exact location using the <code>chip_pin</code> attribute, or through the Assignment Editor.</p>
<p>When two PLLs that both use dynamic reconfiguration are cascaded, dynamic configuration may not work correctly.</p>	<p>Assign the <code>preserve_pll_counter_order</code> assignment to both PLLs. Using this assignment will prevent the Fitter from reordering PLL clock outputs. If the Quartus II software cannot route the clock outputs because the Fitter cannot reorder PLL clock outputs, manually change the clock ordering in the MegaWizard Plug-In Manager.</p>
<p>Projects created in versions of the Quartus II software earlier than version 8.0 that use Incremental Compilation will not work properly with the smart compilation feature in the Quartus II software version 8.0. A message specifying a detected change in the <code>partition_hierarchy</code> assignment is issued and all stages of the flow are executed. Design Space Explorer, which leverages smart compilation technology, is also affected.</p>	<p>Open the project in the Quartus II software version 8.0 GUI and re-save the project before using the Design Space Explorer or smart compilation.</p>
<p>In a design that uses LogicLock regions, when the live I/O check in the Pin Planner is turned on, it may immediately turn off again.</p>	<p>Remove LogicLock regions from the design and turn live I/O check on again.</p>
<p>In the Quartus II software version 8.0, the HSSI rx/tx_coreclk megafunction inputs have to come from HSSI clocks (<code>clkout</code>, <code>coreclkout</code>, and so on), and not from user I/Os or GPLLs unless the <code>coreclk</code> input has a GX 0 PPM core clock setting on it.</p>	

Issue	Workaround
<p>Compiling a PLL in external feedback mode with its compensated clock output connected to a virtual pin triggers an Internal Error.</p>	<p>In external feedback mode, always connect a PLL compensated clock output to an output pin.</p>
<p>In the Quartus II software version 8.0 and earlier, designs using the phase-stepping feature may see situations where the wrong output clock is phase adjusted due to a bug with setting the PLL counter re-mapping LUTs. This issue can occur if the altpll phasecounterselect [] port is fed by constant GND bits or by standalone inverters, and the PLL counters are rotated to improve routability.</p>	<p>If this situation occurs, insert extra logic in front of the altpll phasecounterselect [] port to ensure it is not a constant GND or standalone inverter. For example insert a wire (in Verilog) or a signal (in VHDL) with attribute keep to prevent it from being synthesized away by Analysis & Synthesis.</p>
<p>In the Quartus II software version 8.0, synchronization registers have been added in the altlvds_rx megafunction. The number of registers added depends on the device family selected and the number of bits per channel (deserialization factor). However, these changes have not been propagated to the formal verification model.</p>	
<p>A new assignment check was introduced in Quartus II software version 8.0 that checks whether I/Os are fully constrained.</p> <p>Any I/Os that are not fully constrained appear as a line in a table in the Fitter report under I/O Assignment Analysis Warnings. The reason for the warning appears in the table.</p> <p>Certain conditions are warnings; others are errors. For example, an I/O with no assignments at all will have a reason of "Incomplete set of assignments" and an I/O with only an I/O standard assignment will have a reason of "Missing drive strength and slew rate".</p>	<p>Fully constrain I/Os to remove these warnings.</p>

Issue	Workaround
<p>In the Design Assistant, you can receive an incorrect error R101 even though your design does not contain errors when you use the TimeQuest timing analyzer, your design targets a Stratix IV device, and a clock control (clkctrl) feeds a reset port.</p>	
<p>In the Design Assistant, you can receive an incorrect error D103 even though your design does not contain errors when you use the TimeQuest Timing Analyzer, you use Linux, your design targets a Stratix II GX device, and there is a proper synchronizer.</p>	
<p>The Quartus II software caches the content of the Quartus II Settings File (.qsf). It refreshes the cache only if the Quartus II Settings File changed or the <code><tcl script></code> it includes changes (example: <code>source <tcl script></code>). However, the Quartus II software does not refresh the cache when the Quartus II IP File (.qip) specified by the <code>QIP_FILE</code> assignment changes, even when you close and reopen the project while keeping the GUI open, so that the changes you made to the Quartus II IP File will not get reflected in the GUI.</p>	<p>To make the Quartus II IP File changes show in the GUI, modify the timestamp of the Quartus II Settings File (run <code>touch <revision>.qsf</code>) after you modify the Quartus II IP File, and the cache will reset.</p>

Issue	Workaround
<p>The documentation for the Quartus II software version 8.0 does not include the following information about the Enable Beneficial Skew Optimization logic option:</p> <ul style="list-style-type: none"> • The default value of <code>auto</code> for the project-wide <code>enable_beneficial_skew_optimization</code> assignment is equivalent to <code>off</code>. • The value of <code>auto</code> for instance level <code>enable_beneficial_skew_optimization</code> assignments means that the node in question adopts the value of the project-wide setting. • The HardCopy series of device families does not support the beneficial skew optimization feature. • Instance level <code>enable_beneficial_skew_optimization</code> assignments can be made to any node that is a clock source or destination, including pins, PLL outputs, outputs of user-instantiated clock control blocks, combinational nodes made global automatically, and any register node. 	
<p>All PLL scan chain reconfig Memory Initialization Files (.mif) that were generated in the Quartus II software versions 7.2 SP3 and earlier will have an incorrect bit setting value for the VCO post scale bit.</p>	<p>Re-generate or update the Memory Initialization Files with the Quartus II software version 8.0.</p>
<p>Quartus II Settings File (.qsf) assignments to node names in an imported partition may not be honored or may cause those names to be displayed incorrectly in the Project Navigator or the Node Finder.</p>	<p>Add all assignments to the lower-level project that creates the Quartus II Exported Partition File (.qxp) for the imported partition and while importing the partition turn off Import Assignments in the Advanced Import Settings dialog box.</p>

Issue	Workaround
Beneficial skew benefits can be lost when using incremental compilation.	When using the beneficial skew optimization feature together with incremental compilation, make sure that the top partition preserves routing. Otherwise, performance preservation is not guaranteed and may possibly lead to f_{MAX} degradation. That is, in the Design Partitions window, set Netlist Type to Post-Fit . Set Fitter Preservation Level to Placement and Routing or Placement .
When you export a version-compatible database and then import it back, the SignalTap II Logic Analyzer may not be able to display Finite State Machine debugging tables.	
<p>If you have a JTAG chain with multiple devices that use Serial Flash Loaders to program Active Serial Flash devices, you could get an error when trying to do a verify operation.</p> <p>If a verify operation is attempted on any Active Serial Flash devices in the chain while any operation is selected on any other Serial Flash Loader device in the chain, you can get an access violation.</p>	When doing a verify operation, do not perform any operations on other Serial Flash Loader devices in the chain.
The Quartus II online Help does not include a Rule attribute element for custom Design Assistant rules.	<p>The CUT element is an additional optional element for the Rule attribute declaration:</p> <p>CUT--This optional, string-type attribute can have the values <code>on</code> or <code>off</code>. Setting this attribute to <code>on</code> causes the Design Assistant not to check the rule on a user cut path or false path. The default value is <code>off</code>.</p>

Issue	Workaround
<p>The Quartus II online Help refers to the <LOCAL_DECLARE> and </LOCAL_DECLARE> tags for the Rule definition attribute for custom Design Assistant rules.</p>	<p>You can specify local nodes in the Rule definition <BASIC>, <REQUIRED>, <REQUIRED_EXCEPTION>, <FORBID> or <FORBID_EXCEPTION> subsections with the command <NODE NAME=<node name> . . . ></p> <p>A local node declaration can exist more than once within a rule definition section. If more than one local node declaration exists for a given node, the last occurrence is the declaration honored. If no local node declaration exists, global node declarations are honored.</p>
<p>The syntax for the Reporting declarations has been enhanced.</p>	<p>For further assistance defining Reporting syntax for custom Design Assistant rules, contact Altera Technical Support by creating a Service Request at www.altera.com/mysupport and provide them the reference number rd05272008_575.</p>
<p>Custom Design Assistant rules operate with a specific list of conditions that were not included in Quartus II online Help.</p>	<p>For a list of these conditions, contact Altera Technical Support by creating a Service Request at www.altera.com/mysupport and provide them the reference number rd05272008_582.</p>
<p>Version 7.2 SP1</p>	
<p>When reading a Memory Initialization File (.mif), Quartus II software versions 7.2 and later generate “uninitialized memory addresses” messages, such as:</p> <pre>Warning: 2 out of 32 addresses uninitialized. Initializing them to "0". 2 warnings found. Warning: Address 1 is not initialized. Warning: Address 3 is not initialized.</pre> <p>Quartus II software versions earlier than version 7.2 do not have this issue.</p>	<p>Open the affected Memory Initialization File and search for the “%” character.</p> <p>Because the Quartus II software version 7.2 supports multiline commenting beginning with a “%” and ending with a “%”, if the “%” character is found in the Memory Initialization File, ensure that it does not act as a multiline separator that treats the address data as a comment, or remove the “% in the Memory Initialization File.</p>

Issue	Workaround
Version 7.2	
Live I/O check may produce an error if reserved pin directions are changed while live I/O check is enabled.	Turn live I/O check off and back on again to remove the error.
The Quartus II software unexpectedly exits when importing more than one partition containing JTAG logic.	Keep all JTAG logic within one imported partition, or define the logic in the top-level project instead of importing from another project.
Routing constraints are not compatible from the Quartus II software version 7.1 or 7.1 SP1 to version 7.2. The Quartus II software version 7.2 warns "Info: Error on line number <number> in Routing Constraints File".	No action is required, but you can remove the routing constraints to avoid the warning.
When you compile a project with GXB and LVDS blocks and assigned pins, and click Generate Bottom-up Design Partition Scripts , the bottom-up scripts do not contain pin assignments from the top level.	If you use the Generate Bottom-up Design Partition Scripts command, you must manually copy pin locations for GXB and LVDS blocks into their lower-level scripts.
Using Parallel Flash Loader IP optimized for speed adversely affects the CFI device programming time when using the EthernetBlaster download cable.	Use the USB Blaster or ByteBlaster II download cable instead of the EthernetBlaster Download Cable, or use the Parallel Flash Loader IP optimized for area instead of speed.
Version 7.1	
On Windows, the following cores may fail to run when the PERL5LIB environment variable is set: <ul style="list-style-type: none"> • 8B10B Encoder-Decoder • POS-PHY Level 4 • RapidIO • SerialLite II 	Delete the PERL5LIB environment variable: <ol style="list-style-type: none"> 1. Right-click My Computer and click Properties. 2. Click the Advanced tab, and then click Environment Variables. 3. Delete PERL5LIB under both User variables and System variables. 4. Restart the Quartus II software.

Issue	Workaround
<p>The Quartus II software can reduce RAM by modifying control signals while maintaining functionality. For example, in many cases a read enable can be converted into a clock enable.</p>	<p>This optimization is performed in Analysis & Synthesis, and can be controlled by the <code>optimize_power_during_synthesis</code> Quartus II Settings File (.qsf) variable. For Cyclone III, Stratix III, and Stratix IV devices, the optimization is also performed by the Fitter, and can be controlled by the <code>optimize_power_during_fitting</code> setting. Both the <code>optimize_power_during_synthesis</code> and the <code>optimize_power_during_fitting</code> variables are global settings and may also be applied to particular instances using the Assignment Editor.</p>
<p>If you open the Print dialog box or the Page Setup dialog box in the Quartus II software, and if you use an HP Business Inkjet 1200 series printer, the Quartus II software may produce an unexpected error.</p>	<p>If you have this printer, Altera recommends updating to the latest version of the drivers, available for free download from the HP website.</p>
<p>Altera recommends that all soft-CDR channels driven by a PLL are within a distance of 25 SERDES rows (including the unbonded SERDES) from that PLL.</p>	
<p>When you launch documentation (PDF and HTML files) from the MegaWizard Plug-In Manager, the MegaWizard uses the Web browser option in the Internet Connectivity page of the Quartus II Options dialog box. The MegaWizard will sometimes use a setting from a previous version of the Quartus II software than the present version. This can lead to errors if the web browser does not exist on your machine.</p>	<p>Manually edit the <code>WEB_BROWSER</code> variable in the <code>quartus2.ini</code> file and remove the reference to the non-existent web browser.</p>

Issue	Workaround
Version 6.1	
<p>You may get one or more messages "Error: Can't generate programming files for project because design file "<name>" is encrypted. It does not have license file support that allows generation of programming files" from the Assembler when compiling a design that is using Altera IP with the OpenCore Plus evaluation feature when your design has VHDL source files that have the construct "use work.all;".</p>	<p>The errors are reported for IP source files that were added to your project by IP Toolbench, but which are not actually used during compilation. Remove the files listed in the error messages from your project file list and recompile the design.</p>
<p>The Quartus II software version 6.1 may run out of memory when Formal Verification is turned on and you are using the Quartus II Integrated Synthesis flow. This happens only when Quartus II Integrated Synthesis extracts finite state machines from the design.</p>	<p>To avoid the out of memory issue in the Quartus II software version 6.1, turn off state machine extraction and rerun synthesis. To turn off state machine extraction, use the following settings in the Quartus II project:</p> <pre>set_global_assignment -name EXTRACT_VERILOG_STATE_MACHINES OFF set_global_assignment -name EXTRACT_VHDL_STATE_MACHINES OFF</pre> <p>You can also use the Quartus II GUI:</p> <ol style="list-style-type: none"> 1. On the Assignments menu, click Settings. 2. Select Analysis & Synthesis Settings, and click More Settings. 3. Turn off Extract Verilog State Machines and Extract VHDL State Machines.
<p>When a design contains IP that is evaluated using the OpenCore Plus hardware evaluation feature, the Quartus II software produces a sequence of Info messages beginning with Info: Elaborated megafunction instantiation "pzdyqx:nabboc".</p>	<p>These messages can be safely ignored.</p>

Issue	Workaround
Version 6.0 SP1	
Running multiple instances of the Quartus II software using the same Quartus Project File (.qpf) may cause unpredictable results or may cause the Quartus II software to crash.	Altera recommends that you not open multiple instances of the Quartus II software using the same project.
Version 6.0	
In the classic Timing Analyzer, when a clock (base or derived) is assigned to an internal register, then data paths to and from the register are not analyzed for clock setup and clock hold analysis.	First, analyze the design with the clock settings assigned to the internal registers. Then remove the clock settings from the internal registers and perform a second analysis, checking only paths to and from those registers. The other resolution is to use the TimeQuest Timing Analyzer instead of the classic Timing Analyzer.
The TimeQuest Timing Analyzer erroneously analyzes paths to the asynchronous data pins of registers (that is, the <code>adata</code> pin) during a recovery/removal analysis.	Apply the <code>set_false_path</code> command from the asynchronous data signal's source port or register to declare these paths as false paths.
If you change the type of a parameter setting in the Quartus II Settings File (.qsf) or a Block Design File (.bdf) and recompile your design, your change appears to have no effect. The type of a parameter is denoted by appending a prefix such as "B" (binary), "D" (decimal). For example, B"10101" represents the binary string "10101", but D"10101" represents the decimal number 10101.	Delete the <code><project>\db</code> directory and recompile the design.
Version 5.1 SP2 and earlier	
Due to a limit of the Windows operating system, path names longer than 229 characters can cause an internal error in the Quartus II software.	Make sure that all path names do not exceed 229 characters. This limitation applies to UNIX and Linux installations also.
If you make a single-point CUT=ON assignment to a node, and then override it with a point-to-point CUT=OFF assignment on a specific path, the OFF assignment will not be honored.	
You may receive a "License not found..." error if the path to the license file contains non-ASCII characters.	Change or remove any non-ASCII characters from the license file path.

Issue	Workaround
There is no distinction between output ports and bidirectional ports in AHDL Function Prototypes; instead, all ports listed after the RETURNS keyword are treated as output ports. As a result, if you specify a bidirectional port in a logic function's Function Prototype Statement and do not connect the port to a top-level bidirectional pin or to other logic in the design where you instantiate the logic function, an error can occur.	Connect the port to a top-level bidirectional pin or to other logic in the design.
Context-sensitive Help is not available for some items in the Quartus II software.	To locate Help on those items, click Search on the Help menu, and type the name of the item.
The Classic Timing Analyzer does not recognize non-PLL clock signals when using any PLL megafunction.	Make clock settings assignments to all non-PLL clocks.
The Waveform Editor does not allow you to create a bus with nodes that are nonconsecutive members of a bus.	Create buses only with nodes that are consecutive members of a bus. Or, use the Group command on the Edit menu to create groups of arbitrary nodes.
If you are using the altcam, altclklock, altlvds_rx, or altlvds_tx megafunctions, the equations shown in the Equations Section of the Compilation Report are not complete.	To view the complete equations for any of these megafunctions, use the Equations window of the Timing Closure Floorplan.
The Quartus II software does not support design file names with more than one extension. For example, you cannot use the file name file.eda.edif .	Use design file names with only one extension.
If you install the Quartus II software for PCs on a UNIX server that exports shares with the Samba software version 1.9.18p10, you may experience problems accessing project files that are also on the network.	Altera recommends using version 1.9.16p11 or 2.0 of the Samba software.
If you make assignments to reserve pins as a group or with group notation (debug [7..0]), the Quartus II software does not correctly generate simulation output files, and you receive a warning message saying "Unsupported data type in the top-level module."	Reserve the pins using single-name notation (for example, debug [7] , debug [6] , and so on).

Issue	Workaround
Do not change the file permissions (such as changing “read-only” to “read and write”) of Quartus II Settings File (.qsf) and Quartus II Project File (.qpf) while a Quartus II project is open.	Close the Quartus II project before making changes to the file permissions.
Node names containing numbers greater than 2 ³¹ -1 (2147483647) will cause an Internal Error in the Quartus II software.	Do not use node names containing large numbers.
Occasionally the Programmer does not allow you to use a MAX 7000AE Programmer Object File (.pof) with a MAX 7000AE device. This error sometimes occurs after a compatible MAX 7000B device is used with the MAX 7000AE POF.	Do not switch between compatible MAX 7000B and MAX 7000AE devices when a MAX 7000AE POF is loaded, or reload the MAX 7000AE POF.
Routing back-annotation may fail if the back-annotated locations do not match the location assignments in the Quartus II Settings File (.qsf) or if the location assignments are missing. This problem can occur if you change devices, or if you remove some location assignments by using the Assignment Editor on the Assignments menu or by manually editing the Quartus II Settings File.	If you experience a “no fit” or an Internal Error while using routing back-annotation, delete the Routing Constraints File (.rcf) and back-annotate the design again after a successful compilation.
Occasionally, the Quartus II software may crash or hang with no error message immediately upon opening a project.	Delete the Quartus II Workspace File (.qws) <project name>.qws from the project directory. If the problem persists, delete the \<project directory>\db directory and recompile the design.
When you are setting phase shift and duty cycle values for clock signals using the altpll megafunction, some combinations of settings may result in values that cannot be synthesized exactly. Under certain circumstances, the Quartus II software attempts to synthesize the phase shift parameter before the duty cycle parameter.	You should first select values for the parameter (phase shift or duty cycle) that is most important for your design.
During compilation or simulation, the Quartus II software may “hang” and not proceed to the next module if a menu or modal dialog box is open at the time the current module finishes running.	Close any open menus or modal dialog boxes before the compilation or simulation reaches the next stage.

Issue	Workaround
Running individual Quartus II software executables (quartus_map , quartus_fit , and so on) from within the Quartus II Tcl Console may cause the Quartus II software to crash.	Run individual executables either from within the Quartus II scripting shell (quartus_sh) or directly at a command prompt.
The time shown in the Status window may not agree with the processing times reported in the Compilation Report. This difference is due to differences in how the times are calculated during processing.	
If you type a name in the entity column of the Assignment Editor that differs from an existing name only by case, the Assignment Editor's "auto-completion" feature always uses the existing name.	Type the new entity name in another application, such as a text editor, copy it to the clipboard, and paste the name from the clipboard into the Assignment Editor.
Altera recommends that you do not use node or entity names that differ only by case if you are using the Quartus II Simulator or Waveform Editor.	
Under certain circumstances, a design that uses Virtual Pin assignments may fail to fit after back-annotation. This situation occurs because the clock signals chosen automatically for the first compilation do not match those chosen for the second compilation.	Manually assign your clock signals, using Virtual Pin Clock assignments before the first compilation, or use Advanced Back-Annotation to explicitly write out the virtual clock assignments before the second compilation.
If you use the <code>dcfifo</code> or <code>scfifo</code> megafunctions in an AHDL design, you may receive an error message similar to "The parameter <code>LPM_WIDTHU</code> has been set to an invalid value..."	Either remove the <code>LPM_WIDTHU</code> parameter arguments from your AHDL <code>dcfifo</code> or <code>scfifo</code> megafunction instantiation, or explicitly set the <code>LPM_WIDTHU</code> parameter to <code>ceil(log2(LPM_NUMWORDS))</code> .
Do not open, change permissions, or delete the <code>/<project directory>/db</code> directory or any file therein while any Quartus II executable is running.	

Issue	Workaround
<p>Under certain circumstances, back-annotation of routing in unreserved LogicLock regions can cause unsatisfiable routing constraints for signals going to clock and clock-enable ports of LABs. This can occur when other portions of the design are not back-annotated, and the Fitter populates empty LCELLs in the back-annotated LogicLock region during subsequent compilations.</p> <p>For example, assume that on the initial compilation, LogicLock region L contains register A, which uses the CLK1 and ENA1 ports of a LAB. When the design is recompiled, the Fitter may place register B, which is not part of region L, and uses the SLOAD input, in the same LAB as register A (assuming that the LAB has sufficient empty space to accommodate it).</p> <p>The LAB control signal generation block does not allow use of both ENA1 and SLOAD in the same LAB; therefore, register A must use the CLK0 and ENA0 ports, rather than CLK1 and ENA1. To avoid a no-route situation, the Fitter will ignore the routing constraints for the clock and enable signals, and re-route the signals using the appropriate control signal multiplexing for the CLK0 and ENA0 ports of the LAB. The Fitter picks the most appropriate routing and, in the majority of cases, the circuit's timing is not adversely affected. When the Fitter is forced to ignore routing constraints, info messages of the form "Info: Can't route signal <name> to atom <name>" are displayed to inform the user; the appearance of such messages is not a cause for alarm.</p>	<p>This situation can be avoided entirely by marking all LogicLock regions as Reserved, thereby preventing the Fitter from placing new items in a region. The tradeoff, of course, is that should a Reserved LogicLock region be under-utilized, the Fitter will be unable to place other logic items in the unused portion of the region.</p>

Platform-Specific Issues

Windows Platforms Only

Issue	Workaround
Version 8.0	
The ByteBlaster driver is no longer installed automatically on a PC running Windows Vista 32-bit.	If you want to use a ByteBlaster cable on a PC running Windows Vista 32-bit, install the ByteBlaster driver manually.
USB T-guards are not usable with the Quartus II software on a PC running Windows 64-bit over remote desktop.	
When you open a new design file in the Quartus II software on a PC running Windows 64-bit, then open the Page Setup dialog box, and click Cancel , the Quartus II software hangs.	
Version 7.2 SP1	
When you install the Quartus II software version 7.2 SP1, the Nios II IDE, or any Altera-provided patches on Windows Vista with User Account Control (UAC) turned on, the Program Compatibility Assistant issues the warning: "This program might not have installed correctly."	You can safely ignore this message by selecting This program installed correctly or you can turn off UAC before installing the software.
Version 6.1	
If the Quartus II software is installed on a network drive, Windows is unable to start the JTAG server service because it does not have rights to read from the network drive (services run before users are logged in). If this service is not running, it is not possible for other computers to use JTAG cables on this machine. Occasionally it is not possible for the Quartus II software to use JTAG cables attached to the same machine.	You can either install the Quartus II software locally or run <code><full-path-to>/jtagserver --install <username> <password></code> to specify the username and password that Windows should use when running the JTAG server service.

Issue	Workaround
Version 6.0	
If you are running the Quartus II software on the Windows XP64 operating system with a USB Software Guard, you may receive a message that there is no license found.	You must install the Sentinel driver for the Software Guard by browsing to the quartus/drivers/sentinel/win_xp64 directory when asked for the location of the driver.
Version 5.1 SP2 and earlier	
The introduction of Microsoft Security Update MS05-026 prevents the proper display of Quartus II Help across a network, including displaying popups.	To properly display HTML Help files, you must access them from a local PC. If you are unable to access Help files locally, go to Microsoft Knowledge Base Article 896054 (support.microsoft.com/?kbid=896054) for more information about possible workarounds.
The keyboard accelerators (underlines) for Alt+ key combinations do not appear in the Quartus II user interface until the Alt key is pressed the first time.	This behavior is a Windows 2000 and later Microsoft operating systems user-specified preference. To change to the previous behavior in Windows 2000 and XP, follow these steps: <ol style="list-style-type: none"> 1. On the Start menu, click Control Panel. 2. Click Display properties. 3. Click the Appearance tab. 4. Click Effects. 5. Turn off Hide underlined letters for keyboard navigation until I press the Alt key.
If you use Windows 2000 as a software server to serve the Quartus II software to a client computer running Windows XP, running the Quartus II software on the Windows 2000 server at the same time clients are running the Quartus II software, will cause the Quartus II software on the server to crash.	Do not run the Quartus II software on the Windows 2000 server.
You cannot access the web-based PowerPlay Early Power Estimator on the Altera web site if you have installed Windows XP SP2 because the service pack blocks the active content. email teck huat 4.2	Refer to the Altera Knowledge Database on the Altera website for more information on enabling your browser to access the PowerPlay Early Power Estimator spreadsheets.
Some dialog box title bar text is not displayed correctly when the Quartus II software is installed on a computer running the Chinese version of Windows XP.	Change the font in the Active Title Bar section of the Windows Appearance Control Panel.

Issue	Workaround
<p>If you do not have Administrator privileges when you install the Quartus II software, certain features of the software, particularly the online Help, will not work properly, for example:</p> <ul style="list-style-type: none"> • Software guards (parallel and USB) • Programming with JTAG server 	<p>Altera recommends that you have Administrator privileges when installing the Quartus II software.</p>
<p>Under certain circumstances, the Quartus II installation program may crash or you may receive an error message immediately upon launching the installation program.</p>	<p>Reinstall the stdole32.tlb file from the original Windows distribution disks. To reinstall the file, type the appropriate command at a command prompt. (Note: the command must be typed on one line.)</p> <p>Windows 2000: <CD-ROM drive letter>:\i386\expand.exe stdole32.tl_%SystemRoot%\System32\stdole32.tlb <Enter></p> <p>Windows XP: <CD-ROM drive letter>:\i386\expand.exe stdole32.tl_%SystemRoot%\System32\stdole32.tlb <Enter></p>
<p>If the full, hierarchical name of an instance exceeds 247 characters, it may not be displayed properly in the Quartus II user interface. This problem occurs most often with EDIF netlist files generated by other EDA synthesis tools.</p>	<p>Limit the full, hierarchical instance name to fewer than 247 characters if possible.</p>
<p>If you are running the Quartus II software from a network server, the Quartus II software will not run properly on the client computer if you share the \quartus\bin directory.</p>	<p>You must share the \quartus directory, not the \quartus\bin directory.</p>
<p>The Quartus II software is not compatible with the MATLAB web server.</p>	<p>Turn off the MATLAB web server in the Services Control Panel on the Start menu before running the Quartus II software.</p>

Issue	Workaround
<p>Under some circumstances, the Quartus II splash screen appears and the Quartus II icon appears in the Taskbar, but the graphical user interface does not appear. Under other circumstances, the user interface appears but windows and/or toolbars do not appear correctly.</p>	<p>The registry settings controlling the position of the Quartus II windows may have become corrupted. If the user interface appears, click the Reset All button on the Toolbars page of the Customize dialog box, or, if the user interface does not appear, type the following command at a command prompt: <code>quartus -reset_desktop <Enter></code></p>
<p>If you install the stand-alone Quartus II Programmer and the Quartus II software, and then uninstall either one, the Programmer may report "JTAG Server -- internal error code 82 occurred" when you click the Add Hardware button in the Hardware Setup dialog box on the Edit menu. This error occurs because uninstalling the software has disabled the JTAG Server service.</p>	<p>Manually restart the JTAG Server service by locating the jtagserver.exe program and at a command prompt for that directory, type <code>jtagserver --install <Enter></code></p>
<p>If you choose to uninstall a previous version of the Quartus II software during installation, and there is a "locked" file or directory, the installation program will not reboot the computer as is necessary to successfully complete the installation.</p>	<p>Exit from the installer and reboot the computer manually after the removal of the previous version is complete, before completing the installation of the new version.</p>

Solaris

Issue	Workaround
<p>Version 8.0</p>	
<p>On Solaris, for all cores, when you close the About This Core dialog box, the focus goes to the Quartus II software and not to the IP core. This behavior can put the core behind the Quartus II window and you cannot see it unless you move or minimize the window. Additionally, automation can fail because it cannot find the core to finish testing.</p>	<p>.</p>

Solaris & Linux

Issue	Workaround
Version 8.0	
<p>On Solaris and Linux, there are no syntax highlighting, no tooltips, no support for lock mode (that is, the text will always be editable), and no power-up trigger flow control expression conformance enforcement in the State-based Trigger Flow tab in the SignalTap II Logic Analyzer. However, lack of conformance enforcement does not mean you can freely change the expression, and an acquisition error will occur if changed inappropriately.</p>	<p>.</p>
<p>When you run one of the ALTFTP_CONVERT, ALTDLL, or RAM init MegaWizards on Solaris or Linux, a cancellation and/or normal termination (finish) of the MegaWizard may result in an unexpected error if the calculation of the resource estimate has not been completed.</p>	<p>Wait until the resource estimation process is complete and the result is displayed in the lower left part of the symbol area before an attempt is made to cancel or finish the MegaWizard.</p>
Version 6.1	
<p>Under some circumstances, your web browser software may fail to launch correctly from the IP MegaStore MegaWizard Plug-In Manager. The web browser defined in the MegaWizard Plug-In Manager for the IP MegaStore inherits the environment settings from the Quartus II software. Specifically, the LD_LIBRARY_PATH environment variable may contain entries that conflict with web browsers such as FireFox, preventing them from starting correctly.</p>	<p>Edit the script that launches the web browser to make sure the Quartus II directories are the last entries in the LD_LIBRARY_PATH variable.</p>
Version 6.0	
<p>While any shortcut menu is open from an undocked dockable window, if you right-click the title bar, then all activity in the title bar (left-click and drag, shortcut menu, 'X' close button) stops working.</p>	<p>Display a shortcut menu again and perform any action except right-clicking in the title bar to restore normal operation.</p>

Issue	Workaround
Version 5.1 SP2 and earlier	
If the operating system crashes, and the file system in \$TMP is rebuilt automatically, the data in the \$TMP/Mw_<user ID> file is corrupted, the Quartus II software may fail to start correctly.	Delete the \$TMP/Mw_<user ID> file and restart the Quartus II software.
If you are using the Exceed X server software for Windows while running the Quartus II software, the font size may be larger than the line height. This problem occurs most often if you installed the Exceed software while running at a screen resolution greater than 1024 × 768.	Reinstall the Exceed software while running at a screen resolution of 1024 × 768. You can then switch back to your normal, higher resolution setting.
You cannot launch the AXD Debugger software from within the Quartus II software.	Launch the AXD Debugger software from outside the Quartus II software.
Under some circumstances, the Internet connectivity features of the Quartus II software are not functional.	Specify the full path to your web browser software on the Internet Connectivity page of the Options dialog box. If you access the Internet through a proxy server, you must also specify the address of the proxy server and its port number.
Under some circumstances you cannot access the Quartus II online Help in the user interface.	To access Help, type hh <quartus dir>/common/help/quartus.chm <Return> at a command prompt.
If you are accessing the Quartus II software through one of the following versions of the Hummingbird Exceed software (6.2, 7.0, 7.1, or 8.0) and have any Microsoft Office application or Internet Explorer open, the Quartus II user interface may start very slowly.	Contact Hummingbird Software at www.hummingbird.com for a patch for the Exceed software.
The stand-alone Quartus II Programmer and SignalTap® II programs are not available on Solaris and Linux workstations.	

Linux Only

Issue	Workaround
Version 7.2	
Using the Quartus II software with Linux kernel 2.4 results in slower performance than Linux kernel 2.6.	For improved performance, use Red Hat Enterprise Linux 4 or later, which is a 2.6-based kernel.
Version 7.1	
On the SUSE Linux platform, the Quartus II software opens in the lower right side of the screen, even after you re-position it.	Set the environment variable QUARTUS_MWWM to the value allwm.
Version 7.0	
When you are running the Quartus II software on Red Hat Enterprise Linux 4.0 and using the GNOME desktop, you may receive an internal error when you create a LogicLock region, and then use the Add Path dialog box to add a node for the source name with the Node Finder, and then click Cancel in the Add Path dialog box.	Do not click Cancel in the Add Path dialog box after you add a node for the source name with the Node Finder.
Version 6.0	
The Quartus II software may crash with a core dump if you close the Quartus II software while a properties dialog box is open from any link in Help.	Do not open the properties dialog box on any link in Help.
Your programming hardware is not shown in the Add Hardware dialog box when running under Red Hat Enterprise Linux 64.	Only the EthernetBlaster is supported for programming on 64-bit platforms.
Version 5.1 SP2 and earlier	
If you run a remote Linux desktop session in a Windows client such as Exceed, depending on your configuration, the SignalTap II Logic Analyzer may be unstable and could crash with a segmentation fault.	Use an Xterm window to access the Quartus II software instead of a remote desktop session.

Issue	Workaround
<p>If the MasterBlaster download cable is not listed in the Available hardware items list in the Hardware Settings tab of the Hardware Setup dialog box, but it is connected properly, you may not have read/write permission for the serial (<code>dev/ttySx</code>) port to which the MasterBlaster cable is connected.</p>	<p>Have a system administrator assign read/write permission for the appropriate port. This change can be accomplished by adding you to the “uucp” group, or by giving read/write permission for the serial port to everyone, using the following command: <code>chmod o+rw /dev/ttySx</code> where <i>x</i> is the serial port affected.</p>
<p>If you are using the ReflectionX X-server software as your display on a Linux workstation, the Quartus II software may hang and a white box may appear.</p>	<p>Set the <code>QUARTUS_MWWM</code> environment variable to <code>allwm</code> and then start the Quartus II software without the splash screen by typing the following commands at a command prompt: <code>setenv QUARTUS_MWWM allwm <Return></code> <code>quartus -no_splash <Return></code></p>
<p>Under certain circumstances, the Quartus II software may not start properly.</p>	<p>On a system with a static IP address, ensure that the <code>/etc/hosts</code> file has an entry for the host name of the machine on which you are running. For example, if the workstation is named “orange,” there should be an entry in <code>/etc/hosts</code> with the IP address of the “orange” workstation as shown below: <code><IP address of orange> orange</code> In addition, the network configuration (hostname, DHCP host name, DNS search path, and domain names) must be correct or the Quartus II software will abort on startup.</p>
<p>If you are running the Quartus II software version 4.0 and later using VNC software, the Quartus II software may terminate unexpectedly whenever you open any file or browse any directory from within the Quartus II software.</p>	<p>Make sure your VNC server software is version 3.3.4 or later.</p>

Device Family Issues

Arria GX

Issue	Workaround
The Verilog simulation netlist generated for a design that targets an Arria GX device is incorrect when the reconfiguration feature is used from the ALTGX or ALT2GXB MegaWizard Plug-in Manager.	Modify the netlist by moving the parameter <code>starting_channel_number</code> definition to the line above.

Stratix II GX & Stratix IV

Issue	Workaround
When the live I/O check feature of the Pin Planner is turned on and transceiver pins are present in the design, errors similar to the following occur even though the design will pass I/O assignment analysis: "Pin <name> does not support I/O standard <default I/O standard> for <name>"	Manually assign the proper transceiver I/O standard to the pin.

Cyclone, Stratix & Stratix GX

Issue	Workaround
Version 6.0	
The method used to report power for clock networks is different between the Quartus II PowerPlay Power Analyzer and the PowerPlay Early Power Estimator (EPE). The Quartus II PowerPlay analyzer reports the power for the resource (pin or PLL) that drives the network, while the EPE reports the power in the Clock Network section of the spreadsheet.	No action is necessary.

Issue	Workaround
Version 5.1 SP2 and earlier	
<p>When you use a Routing Constraints File (.rcf) to control fitting after performing Routing Back-Annotation, your timing analysis results may change slightly due to parasitic and other effects. Any change will be very small.</p>	

Cyclone III and Stratix III

Issue	Workaround
Version 7.1	
<p>Location and other assignments made to the altpll megafunction name and intended only for the PLL WYSIWYG are also applied to logic cells created by the altpll megafunction. As a result, you may see errors indicating PLL assignments do not apply to logic cell nodes.</p>	<p>Make assignments intended only for the PLL on the PLL WYSIWYG name only and not on the higher-level altpll hierarchy name.</p>

Cyclone III, Stratix III, and Stratix IV

Issue	Workaround
Version 8.0 SP1	
<p>In the Quartus II software version 8.0, incorrect behavior results in designs targeting Cyclone III, Stratix III, or Stratix IV devices when the register has an inverted <code>sload</code> signal and the <code>sdata=GND</code>, and register is packed into either the output register or input register, then the inversion is lost. This behavior is seen as incorrect because the register clears at the wrong times.</p>	<p>This issue is fixed in the Quartus II software version 8.0 SP1.</p>
Version 8.0	
<p>In the Quartus II software version 8.0, the I/O primitives do not support exact pin location assignments in designs that target Stratix III, Cyclone III, and Stratix IV devices.</p>	<p>Set the pin location assignment using the Assignment Editor. Note that this issue is present only when an exact pin location is specified. The location assignment is honored correctly when an IOBANK location or an EDGE location is specified.</p>

Stratix and Stratix GX

Issue	Workaround
Version 6.0	
<p>The Quartus II PowerPlay Power Analyzer reports PLL, XGMII state machine, GXB transceiver, and I/O pin power as contributors to the power reported for High Speed Transceiver blocks. However, the PowerPlay Early Power Estimator (EPE) spreadsheet reports this power in a “High Speed Transceiver Blocks” section as well as an entry in the “Clock Networks” section. Similarly, the PLL, SERDES blocks, and I/O pins of an LVDS block are reported in the PowerPlay Power Analyzer, and as entries in the Clock Networks and HSDI sections of the EPE spreadsheet.</p>	

Stratix

Issue	Workaround
<p>Designs compiled for Stratix EP1S40ES devices must be recompiled for the EP1S40 device before programming.</p>	

Stratix II

Issue	Workaround
Version 8.0	
<p>Compiling a Stratix II PLL in external feedback mode with its compensated clock output connected to a virtual pin triggers an Internal Error.</p>	<p>In external feedback mode, always connect Stratix II PLL compensated clock output to an output pin.</p>

Issue	Workaround
Version 6.0 and earlier	
<p>Due to changes in the altlvds_tx and altlvds_rx megafunctions in the Quartus II software version 5.0, user-created timing assignments to the megafunctions are changed. The megafunctions now make most timing assignments automatically.</p>	<p>Check your assignments to make sure that the Quartus II software implemented them correctly.</p>
<p>The Quartus II software version 5.0 does not support programming file generation for some Stratix II devices when M-RAM blocks are used in some memory modes, and if the STRATIXII_MRAM_COMPATIBILITY option is turned off.</p>	<p>For more information about programming file support for Stratix II devices, refer to the <i>Stratix II FPGA Family Errata Sheet</i>, which is available on the Altera website.</p>

Stratix GX

Issue	Workaround
Version 6.0	
<p>Timing simulation performed in the Quartus II software on designs that use the altgxb megafunction in Stratix GX devices is not accurate on the rx_clkout and rx_out outputs. The simulation is functionally correct, but the relative timing delays between the signals are not accurate.</p>	<p>Perform your timing simulation in another tool such as ModelSim.</p>

Stratix II GX

Issue	Workaround
Version 7.2	
<p>The VCS flag <code>-ntb_opts +check</code> can produce the following error when running Synopsys VCS simulation using stratixiigx_hssi_atoms.v (alt2gxb simulation library):</p> <p>Error: Illegal array access.</p> <p>This out-of-bound/illegal array access at time 0 happens at unused channels/blocks where default parameter values and initial values of ports are not consistent.</p>	<p>Remove the <code>+check</code> option when compiling stratixiigx_hssi_atoms.v. The check is to report specifically out-of-bound or illegal array access (no other type of checking).</p>
<p>Stratix II GX post-fit compiler databases created in the Quartus II software version 7.1 are not backwards compatible with the Quartus II software version 7.2.</p>	<p>Rerun the Fitter after importing Stratix II GX projects compiled in the Quartus II software version 7.1.</p>
Version 6.0	
<p>The latency of alt2gxb megafunction simulations on Stratix II GX is not accurate in comparison to the device. This is due to approximation used in the Quartus II simulation in modeling the analog portion of the hardware. The latency on the digital portion is within the range of a few clock cycles of the device. The latency is an exact match with the hardware when input vectors are carefully made and do not contain any race conditions.</p>	<p>The Stratix II GX handbook has specified latency range information. The latency information from Quartus II simulations is a good approximation.</p>

Stratix II and Stratix II GX

Issue	Workaround
Version 8.0 SP1	
<p>In Quartus II software versions 8.0 and earlier, the altlvds_tx simulation model for EDA simulation shows that the tx_outclock signal is edge aligned with the tx_out signal when OUTCLOCK_ALIGNMENT is 180_DEGREES and USE_EXTERNAL_PLL is ON.</p>	<p>Simulate the design in the Quartus II software version 8.0 SP1.</p>
Version 7.2	
<p>The mode 2 DLL frequency range for Cyclone III devices is improved from 200-310 MHz to 200-350 MHz. Other modes are not changed. Other speed grades are not changed. No existing design will have worse timing and you do not need to run timing analysis again.</p>	

Stratix III

Issue	Workaround
Version 8.0	
<p>The Stratix III MLAB models in the PrimeTime netlist whose instances use an ena0 input pin do not have setup and hold arcs for an ena0 input pin. The MLAB instances can be identified in the netlist by their instance names and their location in an MLAB as specified on the line preceding the MLAB instance line.</p>	<p>Using the TimeQuest Timing Analyzer, verify all timing paths ending on ena0 pins of MLABs.</p>
<p>You may see an Internal Error during timing analysis on a design targeting a Stratix III device to an I/O with a current strength setting of Minimum Current or Maximum Current.</p>	<p>Replace the current strength setting on the I/O with a correct current strength setting (for example, 12mA), instead of a maximum or minimum.</p>

Issue	Workaround
Version 7.2	
<p>In the Quartus II software version 7.2, Stratix III devices do not support the following three primitives: ALT_OUTBUF_TRI_DIFF ALT_IOBUF_DIFF ALT_BIDIR_DIFF</p>	
Version 7.1	
<p>If a design that targets Stratix III devices uses LVDS RX in an I/O row, you cannot use half-rate DDR on the TX pins of the same I/O row. As a result, you cannot use DQ pins of a DDR memory interface together with LVDS RX in any Horizontal I/O row.</p>	

Stratix III and Stratix IV

Issue	Workaround
Version 8.0	
<p>Using the altlvds_rx megafunction in designs that target Stratix III and Stratix IV devices and not registering the output does not generate the correct warning.</p>	
<p>For designs targeting Stratix III or Stratix IV devices, the following warning message is obsolete, and can be safely ignored: Warning: delay_chain_length parameter of DLL atom <name> is set to 8, but should only be set to 10, 12, or 16 when delay_buffer_mode is set to low</p>	

Stratix IV

Issue	Workaround
Version 8.0 SP1	
<p>Back-annotating a design that targets a Stratix IV device with transceivers and then compiling might result in the following error: "Error: Can't fit design in device -- nodes in regions on the device require more global signals than are available."</p>	<p>Remove the location assignments on the registers or logic specified in the submessages.</p>
Version 8.0	
<p>Transceiver blocks will not be included when you generate a PowerPlay Early Power Estimator file from the Quartus software for a Stratix IV device. Only transceiver blocks are ignored; all the other blocks (logic, RAM, I/O, and so on) are still included.</p>	
<p>Disabling the output termination assignment on a Stratix IV transmitter transceiver pin (Example: <code>set_instance_assignment -name output_termination OFF -to tx_dataout</code>) without a valid transceiver I/O standard assignment on the pin will result in the following error: "Error: One or more pins are missing I/O standard assignments"</p>	<p>Make a valid HSSI transceiver I/O standard assignment on the pin or enable the <code>output_termination</code> setting.</p>
<p>You will receive a warning when you use an MLAB as a synchronizer in designs targeting Stratix IV devices.</p>	

Issue	Workaround
<p>In the alt4gxb megafunction, which is instantiated when using the ALTGX MegaWizard), channels with the following configurations will have rate_match_back_to_back parameters set to false:</p> <ul style="list-style-type: none"> • Basic protocol • Double deserialization block width • Enable rate match FIFO <p>GXB Receiver channel PCS rate_match_back_to_back parameters refer to the back-to-back insertion and deletion of rate match characters. Two characters will be inserted or deleted to re-center the register.</p>	<p>Change the file manually:</p> <ol style="list-style-type: none"> 1. Open the MegaWizard Plug-In Manager-generated megafunction file. 2. Change the rate_match_back_to_back parameter to true. <p>For example, <pre>receive_pcs0.rate_match_back_to_back = "true",</pre> </p>
<p>PCIE Gen 2 x8 will have 8 rateswitch control ports (if 8 channels are used) and only rateswitch[0] will control the operation. rateswitch[7:1] does not have any affect. The same applies to PCIE Gen2 x4 mode (rateswitch[3:1] has no affect).</p>	
<p>Quads that use the PCI Express hard IP blocks cannot be merged with quads that do not use the PCI Express hard IP blocks.</p>	
<p>In designs that contain the alt4gxb megafunction, which is available through the ALTGX MegaWizard Plug-In, and that target Stratix IV devices, simulation on the output port rx_phase_comp_fifo_error is incorrect.</p>	
<p>When you create a design that contains an alt4gxb megafunction and targets the Stratix IV family, and in 6G basic mode, two words are used in byte order pattern, the Quartus II simulation of the bytesyncstatus output is incorrect. It aligns to the lower word only in word alignment and ignores the upper word of the byte order alignment pattern.</p>	
<p>You may be able to compile memory interface designs exceeding the <i>Stratix IV Device Handbook</i> limits.</p>	<p>You cannot go to production with Quartus II software version 8.0 compilation limit. Refer to the <i>Stratix IV Device Handbook</i> for actual device maximum performance.</p>

Issue	Workaround
Designs with Stratix IV transceivers containing PCI Express hard IP atoms might not fit and might give errors related to transceiver blocks. The errors might not be specific to PCI Express hard IP-related transceivers.	Manually lock down at least one pin of transceivers that use PCI Express hard IP blocks.
Back-annotating designs with transceivers might produce the error "Can't fit design in device -- nodes in regions on the device require more global signals than are available." This error could occur if transceiver clock signals are driving output pins.	Alter the designs so that the clock signals are not driving output clock pins.

Cyclone

Issue	Workaround
Altera recommends that the frequency of the external clock output of the PLLs be limited to 312 MHz.	
The PLL lock circuit does not function correctly for PFD (Phase Frequency Detector) frequencies below 200 MHz when the temperature is below -20°C.	If operation at temperatures below -20°C is required, choose a higher input frequency and clock division (N) factor such that the PFD input frequency is higher than 200 MHz.

Cyclone II

Issue	Workaround
Version 5.1 SP2 and earlier	
A write error has been detected on Cyclone II M4K RAMs when using dual ports and dual clocks for designs compiled with Quartus II software version 5.0 SP1 and earlier.	A software workaround is available to address this issue in the Quartus II software version 5.0 SP2 and Quartus II software version 5.1. To learn more, refer to the Cyclone II Errata on the Altera website.
Back-annotating some designs targeted to a Cyclone II device with the Demote cell assignments to option set to LABs may prevent the design from fitting.	Back-annotate the design with Demote cell assignments to turned off.

Cyclone III

Issue	Workaround
<p>If you use DDR or DDR2-SDRAM memory interfaces in designs targeting Cyclone III devices, you may receive the following warning from the TimeQuest Timing Analyzer: Critical Warning: The register <name> fed by pin <DQ or CK0 pin> must be placed in adjacent LAB <name of adjacent LAB> instead of <name of current FF location> to the result.</p>	<p>If the adjacent LAB is already used by DDIO input registers for other pins, you may receive this warning because no more than two global clocks (inverted clocks are counted separate from non-inverted clocks) may feed a LAB. To fix the warning, you need to move the CK0/CK0# pins to a location with a free adjacent LAB. A possible solution is to swap CK0/CK0# with CK1/CK1# or CK2/CK2#.</p>
<p>When you receive the following message, there is a timing violation issue that needs to be fixed: Critical Warning: The register <name> fed by pin <DQ or CK0 pin> must be placed in adjacent LAB <name of adjacent LAB> instead of <name of current FF location> to the result</p>	<p>Fix the problem to avoid violating assumptions made with the macro timing analysis used for Cyclone III devices. A possible solution is to swap CK0/CK0# with CK1/CK1# or CK2/CK2#.</p>

HardCopy II

Issue	Workaround
Version 8.0	
<p>Behavior of region constraints on HardCopy II is changed in the Quartus II software version 8.0 such that all HCell-based logic must be placed within the region boundaries. In Quartus II software versions 7.2 SP3 and earlier, this restriction was not necessary, and there was a 20 HCell tolerance at region boundaries. This new behavior allows you to enable more advanced incremental compilation flows.</p>	<p>The change in behavior can cause no-fits because the available area for a region constraint is now smaller than in earlier releases. You may need to increase region sizes in order to achieve a fit.</p>

Issue	Workaround
Version 7.2	
<p>When compiling a HardCopy II design and using the HardCopy II Advisor to compare timing against the Stratix II FPGA flow, the timing for the I/Os may be different. This difference is because the FPGA compilation used Advanced I/O Timing, which is unsupported for HardCopy II devices, to get I/O delays.</p>	<p>When compiling the FPGA, disable Advanced I/O Timing by setting the Quartus II Settings File (.qsf) assignment <code>ENABLE_ADVANCED_IO_TIMING</code> to OFF or turn off Enable Advanced I/O Timing in the Timing Quest Timing Analyzer page in the Settings dialog box.</p>
Version 6.0	
<p>Under certain circumstances, you may receive the following error message when migrating your Stratix II design that contains RAM blocks to HardCopy II: "Error: Source file <file> in directory <dir> was compiled at <time> and saved at <time>. The problem reported for the file is: Only in HardCopy II (<design>)."</p>	<p>Turn off the Auto RAM Block Balancing option for your Stratix II design and recompile the design. Then proceed with the migration process.</p>
Version 5.1 SP2 and earlier	
<p>PCI core designs compiled with versions of the PCI Compiler earlier than 4.0.0 will cause numerous spurious differences to be reported in the Companion Revision Compare section of the Compilation Report, even though the source files are correct.</p>	<p>Recompile the PCI core with the PCI Compiler version 4.0.0 or later.</p>

EPC2 Configuration Devices

Issue	Workaround
Version 6.0	
<p>When using the EPC2 configuration device to configure an Altera FPGA using a compressed configuration bit stream, you may encounter a configuration failure due to the CONF_DONE error checking feature. The failure mode occurs when the FPGA releases the CONF_DONE signal outside the acceptable time window. The reason this may occur is because the compression ratio varies depending on the design file. Since the configuration file size varies due to compression there may be insufficient padding at the end of the configuration file. This issue can result in a configuration failure, as indicated by the nSTATUS pin transitioning low near the end of configuration. The error occurs because the CONF_DONE signal is released by the FPGA before the EPC2 device expects it to be released.</p>	<p>For assistance implementing the workaround, contact Altera Technical Support at www.altera.com/mysupport and provide the reference number rd01232008_817.</p>

Design Flow Issues

Verilog HDL Integrated Synthesis

Issue	Workaround
<p>A Verilog HDL design that compiles successfully in earlier versions fails in the Quartus II software version 5.1 with the message "Formal port <port_name> must be connected to a structural net expression."</p>	<p>The Verilog language requires that a module instance output port be connected to a net, and not to a reg variable or to a constant. Previous versions of the Quartus II software did not enforce this restriction. Change the variable connected to the module instance output port to a wire datatype.</p>

SOPC Builder Issues

Issue	Workaround
Version 8.0	
<p>The system interconnect fabric that is automatically created when you generate your system in SOPC Builder does not correctly resolve the bytes that are not selected by the byteenable lines on a 64-bit write to a 32-bit Avalon-MM slave interface with no byteenable capability. If a master module sends a 64-bit write request to a system component 32-bit Avalon-MM slave interface, the write arrives at the slave port as two separate 32-bit writes to consecutive addresses. If the byteenable lines indicate a single 32-bit write to the destination address, because the byte enables are not asserted for the second half of the 64 bits, the write nevertheless occurs at both addresses. Therefore, if the byteenable lines for the second half of the 64-bit write are not asserted, the address following the destination address is written erroneously.</p>	<p>Perform the following workaround for each 32-bit, byteenable-free slave port in your SOPC Builder system component:</p> <ol style="list-style-type: none"> 1. In SOPC Builder, on the System Contents tab, add an Avalon-MM Pipeline Bridge component. 2. In the Avalon-MM Pipeline Bridge editor, under Pipeline options, configure the pipeline bridge with all three pipeline options turned off. 3. Under Data options, set Data width to 32 bits. 4. Under Burst options, turn on Allow bursts and set the Maximum burst size to 2. 5. Connect the Avalon Memory-Mapped Master Port of the pipeline bridge to the slave port in your SOPC Builder system component. 6. Connect the Avalon Memory-Mapped Slave Port of the pipeline bridge to the master module that would otherwise be connected directly to the slave module.
<p>A component originally provided and created with SOPC Builder component version 7.2 with multiple clock ports generates an error in the Quartus II software version 8.0.</p>	<p>Edit the Tcl Script File (.tcl) associated with the component to remove any derived clocks. This clocking scheme is not supported for the component.</p>
<p>You cannot run multiple instances of the System Console if an already existing instance has a JTAG-based service open.</p>	<p>Open as many System Consoles as are required before issuing any commands to any of them.</p>
<p>The System Console hangs with the message <code>NIOS20CI::internal_unlock(): Assertion 'm_locked' failed.</code> when accessing a service provided by a Nios II processor and services provided by other modules simultaneously.</p>	<p>Open as many System Consoles as are required before issuing any commands to any of them.</p>
<p>If a Tcl script puts the System Console into an infinite loop, the console may hang and it will not close when you click the Close button.</p>	<p>Use the operating system to stop the process.</p>

Issue	Workaround
When masters execute write transactions to narrower-data width slaves, unintended write transactions can occur. The problem can occur only for dynamically-aligned slaves that do not have byteenable ports.	When possible, dynamically-aligned slaves should be provided with byteenable ports. In cases where the slave component cannot be modified, a simple workaround for this problem is to insert an Avalon-MM pipeline bridge in between the master and slave. (If this bridge is configured with all three of its pipeline options turned off, the component consists only of wires, and thus consumes no logic resources.)
The Launch Altera's ALTPLL MegaWizard button in the Edit Module wizard for the PLL component has no effect when the path to the project directory contains a space.	Instantiate the ALTPLL megafunction outside the SOPC Builder system, or move the project to a location that does not contain a space.
The System Console cannot launch when a nios2-terminal is already running.	Open the System Console first, and then start a nios2-terminal.
Tooltip information entered into Component Editor is not saved in the component's Tcl Script File (.tcl).	The tooltip can be added to the Tcl Script File manually as the last argument to the add_parameter command.
If VHDL components have a generic of type 'std_logic_vector' , the width of the vector cannot be greater than 32 bits.	Use generics of type integer , or that are less than 32 bits wide.
On systems where adapters are inserted in front of the widest Avalon-MM slave in the system, generation may fail with the following message: Base address for module_name must be a multiple of its span	Manually readdress the slaves according to the span provided in the error message.
On Windows Vista-64, when using the 64-bit version of the Quartus II software, SOPC Builder occasionally hangs while generating the system, or while upgrading SOPC Builder system version 6.2 or earlier.	Use 32-bit version of the Quartus II software instead of the 64-bit version.
When using an Altera IP component with a Verilog functional simulation model in the Mentor Graphics ModelSim-Altera Edition simulator, the altera_mf library is compiled instead of being referenced, causing the simulator to exceed the instance count limit, and run very slowly.	Remove the <code>`include</code> line from the top-level generated Verilog Design File (.v) for any file in quartus/eda/sim_lib .

Issue	Workaround
<p>The Nios II processor is configurable and may or may not include an MMU, MPU, and extra exception (EE) handling. However, the System Console always presents all registers from these modules as a response to processor_get_register_names, even when these registers don't exist. Reading MMU, MPU, and extra exception handling registers when they don't exist returns the value of other registers.</p>	<p>Don't read registers in the MMU, MPU, or EE modules when the Nios II processor does not include these options.</p>
<p>Sourcing pci_constraints.tcl for the PCI Lite component will fail if Simulation is not turned on in the SOPC System Generation tab.</p>	<p>Turn on Simulation in the SOPC System Generation tab before sourcing pci_constraints.tcl.</p>
<p>The "PCI Lite Core" chapter in Volume 5 of the <i>SOPC Builder Handbook</i> states incorrect command lines.</p>	<p>Instead of the command lines in page 13-20, step 4 of the Simulation Flow under the Simulation Considerations section, use the following lines:</p> <pre> `include "<quartus_root>/ip/sopc_builder_ip /altera_avalon_pci_lite/pci_sim/ve rilog/pci_lite/pci_tb.v" `include "<quartus_root>/ip/sopc_builder_ip /altera_avalon_pci_lite/pci_sim/ve rilog/pci_lite/clk_gen.v" `include "<quartus_root>/ip/sopc_builder_ip /altera_avalon_pci_lite/pci_sim/ve rilog/pci_lite/arbiter.v" `include "<quartus_root>/ip/sopc_builder_ip /altera_avalon_pci_lite/pci_sim/ve rilog/pci_lite/pull_up.v" `include "<quartus_root>/ip/sopc_builder_ip /altera_avalon_pci_lite/pci_sim/ve rilog/pci_lite/monitor.v" `include "<quartus_root>/ip/sopc_builder_ip /altera_avalon_pci_lite/pci_sim/ve rilog/pci_lite/trgt_tranx.v" `include "mstr_tranx.v" </pre>

Issue	Workaround
Version 7.2 SP1	
The Scatter-Gather DMA component in SOPC Builder does not support unaligned transfers for a 16-bit data width.	
Access to bursting components, such as DDR SDRAM, may fail in SOPC Builder.	The cause for some bursting failures is related to the different bursting capabilities of Avalon-MM master and slave ports. DDR SDRAM supports burst wrapping whereas other components do not. To resolve this issue, ensure that burst boundaries are not crossed during burst transactions.
Version 7.2	
In a Nios II system, if you turn on Enable bursts for the Data master settings in the Nios II processor, data master burst reads of size > 1 from unassigned locations result in system lockup.	Avoid making data master reads from unassigned locations.
The gray drag boxes next to HDL file names in the Component Editor do not change the order of the files.	To change the order of the files, remove them and re-add them in the correct order.
You may get a SEVERE : [Error.Other] Error writing cache error when SOPC Builder tries to cache components on Windows and the absolute path to the component is longer than the windows maximum file name size. The component loads after a short delay.	Move the component such that it's in a shorter path to shorten the load time.
When a latent-aware Avalon master does a read access to a nonexistent location, the Avalon bus fabric returns a dummy response so that the reading master does not stall. However, only a single response (readdatavalid pulse) is returned. If a burst read is done to a nonexistent location, the bursting master receives only the single response, and stalls while awaiting the remaining readdatavalid pulses.	

Issue	Workaround
SOPC Builder generation may fail with Java errors when the system is generated from the command line using a Tcl script. These errors occur if no Xserver is running on your machine.	Set up an Xserver on your machine and regenerate the SOPC Builder system.
The SOPC Builder may generate errors regarding address span overlap when generating systems with bursting masters and wide data path widths of 32 bits or more.	Move the native addressing components farther apart so that base addresses won't overlap even if the span grows by a factor of 2 (or 4 if the data width is 128 bits).
Version 7.1	
Custom components created in versions of SOPC Builder earlier than 7.1 that have data widths that are not multiples of two and greater than 8 bits will not upgrade properly.	Import your custom logic into Component Editor and specify a data width that is at least eight bits wide and a multiple of two (8, 16, 32, 64, etc...) If you increase the width of your component to comply with these limits, the Quartus II software automatically removes any unused bits during synthesis.
An Avalon-MM master connected through an Avalon-MM pipeline bridge or Avalon-MM clock crossing bridge to Avalon-MM slaves that use native addressing will fail if the bridge is wider than the master.	Do not connect a narrow Avalon-MM master to a wider Avalon-MM bridge if that master accesses an Avalon-MM slave that uses native addressing through the bridge.
The Component Editor in SOPC Builder does not support Verilog HDL design files (.v) that have multiple modules or VHDL design files (.vhd) with multiple entities.	Use only one module for each Verilog HDL design file and one entity for each VHDL design file.
If a module dependency loop is reported between the DMA controller and pipeline bridge, the resulting system may still be functional.	The system can be generated by holding down Ctrl and clicking the Generate button.
Version 7.0	
If a one-bit port on a VHDL component is defined as a STD_LOGIC_VECTOR (0 downto 0) the port width will be misinterpreted during SOPC Builder system generation.	Define all single-bit ports as STD_LOGIC.

Issue	Workaround
Version 6.1	
<p>Compiling an SOPC Builder design generates the following message:</p> <p>"Warning: Found invalid timing assignments -- see Ignored Timing Assignments report for details."</p> <p>SOPC Builder erroneously applies an invalid timing assignment as an embedded attribute in the HDL code it generates.</p>	<p>You can ignore these warnings for the SOPC Builder system.</p>
Version 6.0	
<p>If multiple masters control a slave that asserts <code>endofpacket</code>, both masters will see the asserted <code>endofpacket</code>. This may cause problems in systems where masters take action upon <code>endofpacket</code>.</p>	<p>Use <code>endofpacket</code> only in the case that a single master of the asserting slave will take action on the <code>endofpacket</code>.</p>
Version 5.1 SP2 and earlier	
<p>Under some circumstances, the automatic addressing feature does not function correctly.</p>	<p>Assign the base address for the component manually.</p>
<p>Under some circumstances, the SOPC Builder does not display correctly on systems in which the graphics card uses hardware acceleration.</p>	<p>Turn off, or reduce the level of hardware acceleration.</p>
<p>SOPC Builder fails to open on UNIX when invoked from the MegaWizard Plug-In Manager.</p>	<p>Open SOPC Builder by clicking SOPC Builder on the Quartus II Tools menu.</p>
<p>The SOPC Builder and Nios II Software Development Kit shell may "hang" and become unresponsive if you run either program while the Frisk antivirus software is running.</p>	<p>Turn off the Dynamic Virus Checking feature of the Frisk software before running SOPC Builder or the Nios II SDK shell.</p>

EDA Integration Issues

Issue	Workaround
Version 8.0	
The Quartus II software version 8.0 lists PALACE as an EDA tool for physical synthesis.	If you use the Magma Design Automation Blast FPGA software, you can use the PALACE flow for physical synthesis.
The clock path delays reported by the PrimeTime software may not be accurate for Stratix III family, due to a limitation in min/max clock path modeling. The clock path delays reported by the PrimeTime software may be off by a few hundred picoseconds, compared to those reported by the TimeQuest Timing Analyzer.	
The Quartus II software may show false errors when you exit the Aldec Active-HDL 7.3 GUI containing the waveform window, when the Active-HDL 7.3 GUI was launched via the NativeLink interface.	Set waveform mode to standard waveform in Active-HDL 7.3 GUI by running the command waveformmode awf , either from the Active-HDL console window or from within the do file, before initializing simulation. You need to complete this process only once because the waveform mode is stored in the registry.
If you want to upgrade to Mentor Graphics ModelSim 6.3f release, which is more recent than the Altera-supported version of 6.1g, you can expect some speed up in simulation time. However, there are known issues with the 6.3f release.	Possible solutions include the following: <ul style="list-style-type: none"> For designs that are giving incorrect simulation results, turn off the optimizer by commenting out the following line in the modelsim.ini file: <pre>; VoptFlow = 1</pre> If you use altera_mf.vhd and simulate altsyncram model, avoid the known bug in version 6.3f by typing the following: <pre>vcom -opt=-clkOpt altera_mf.vhd</pre> instead of the normal compilation: <pre>vcom altera_mf.vhd</pre>
Version 7.2	
When reporting timing, the Synopsys PrimeTime software issues an error message (UITE-461) that states that rise_edge or fall_edge cannot be satisfied, and assumes zero source latency for certain derived clocks.	Set variable timing_edge_specific_source_latency to false in the PrimeTime shell before reporting timing.

Issue	Workaround
<p>Mentor Graphics ModelSim Altera Edition 6.1g and the ModelSim SE 6.1g software may run out of memory with an error on the Windows platform, when compiling or simulating a large post-fit netlist.</p>	<p>Use a 64-bit computer running the Linux operating system to compile and simulate the design. Contact Mentor Graphics for additional support.</p>
<p>Version 7.1</p>	
<p>If your design contains WYSIWYG atoms, and you select another family in the Quartus II project, RTL Simulation using NativeLink results in errors.</p>	<p>If your design contains a clear box netlist generated for a specific device family, and you target a different device family in the Quartus II project, regenerate the clear box netlist for the correct device family. If your design contains IP, check IP documentation to verify whether it supports NativeLink simulation.</p>
<p>Version 6.1</p>	
<p>If there are virtual I/O pin assignments at the time of generating board-level timing files in the STAMP format, and if there is any other tool or format selected in any EDA tool category on the EDA Tool Settings page, you may receive an error when you run the EDA Netlist Writer.</p>	<p>If the design has virtual I/O pin assignments, and you want to generate board-level timing files in the STAMP format, then either remove the virtual I/O pin assignments from the Quartus II Settings File (.qsf) and recompile the design, or make sure the following is true before running quartus_eda: All tool and format settings in all categories are set to None with the exception of Board-Level timing analysis tool category. STAMP is selected as the EDA format in the Board-Level Timing Analysis tool category in the Board-Level page under EDA Tool Settings. Or, you can run the following command at a system command prompt:</p> <pre>quartus_eda --format=stamp -- board_timing <project> -c <revision></pre>

Issue	Workaround
Version 6.0	
The ModelSim software may fail to simulate a design if Glitch Filtering is turned on in the EDA Simulation Settings page and the <code>+nospecify</code> option is passed to the ModelSim <code>vsim</code> command.	Remove the <code>+nospecify</code> option from the ModelSim <code>vsim</code> command.
If you add or change a component in a Library Mapping File (<code>.lmf</code>), the Quartus II software does not recognize the changes upon the next compilation.	Delete the project database (<code>db</code>) directory and recompile.
Version 5.1 SP2 and earlier	
FIFO Partitioner instances can only be simulated in 3 rd party simulators using the original VHDL source files from the <code>quartus/libraries/megafunctions/</code> directory, and NativeLink integration is not supported.	Perform simulation manually as described in the FIFO Partitioner User Guide available from the Literature page of the Altera web site.
The current version of the Quartus II software allows you to select the Synplicity Amplify software as a physical optimization tool. However, this setting is for an automated mode called ATOPS, which is currently not supported by the Amplify software.	Contact Synplicity for the support schedule for the Amplify software ATOPS mode.
NativeLink support does not work with versions of Mentor Graphics Precision RTL Synthesis Software earlier than version 2003b due to a change in the Precision project interface.	

Memory Interfaces Issues

Issue	Workaround
Version 8.0 SP1	
Designs with the QDRII ALTMEMPHY megafunction could fail due to an incorrect <code>mem_doff_n</code> operation. Calibration could begin before the required 2048 clock cycles (to allow the DLL on the memory device to lock) following the deassertion of <code>mem_doff_n</code> .	The ALTMEMPHY megafunction in the Quartus II software version 8.0 SP1 contains logic to ensure this condition will not occur. Regenerate the QDRII ALTMEMPHY megafunction with the Quartus II software version 8.0 SP1.

Issue	Workaround
<p>Designs with the ALTMEMPHY megafunction generated in the Quartus II software version 8.0 or earlier and that target Stratix III devices for DDR or DDR2 SDRAM interfaces have insufficient SDC timing constraints on the datapath reset logic. This may cause the design to fail power up calibration in some cases.</p>	<p>Re-generate the memory controller or ALTMEMPHY interface with the Quartus II software version 8.0 SP1 to update the SDC timing constraints.</p>
<p>Designs with the ALTMEMPHY megafunction or the DDR/DDR2 SDRAM High Performance Controller IP created in the Quartus II software version 8.0 that target DDR or DDR2 SDRAM could fail to calibrate correctly in hardware under certain conditions. All variations and device families are potentially affected by this issue.</p>	<p>Regenerate the memory controller or ALTMEMPHY interface with the Quartus II software version 8.0SP1.</p>
<p>Version 8.0</p>	
<p>The SDC and Tcl scripts generated in Quartus II software versions 7.2 SP3 and earlier for all ALTMEMPHY-based memory interfaces (including the DDR High Performance Controller, the DDR2 High Performance Controller, and the DDR3 High Performance Controllers for all device families) are incompatible with the Quartus II software version 8.0. Compilation may fail in the Fitter with the error: Error: can't read "pll_ref_clk": no such variable and timing analysis will not run. This error occurs because the node types in the timing netlist generated by the TimeQuest Timing Analyzer in the Quartus II software version 8.0 are different from those generated in version 7.2. An SDC update is required to traverse it correctly.</p>	<p>Regenerate the ALTMEMPHY megafunction with the Quartus II software version 8.0.</p>

Issue	Workaround
<p>When you compile an ALTPMEMPHY QDRII/QDRII+ SRAM interface in the Quartus II software version 8.0, you may receive this error: Error: Bidirectional I/O "mem_dqsn[0]" uses parallel termination but does not have dynamic termination control connected</p>	<p>Regenerate the ALTMEMPHY megafunction with the Quartus II software version 8.0, or change the bidir pins mem_dqs, mem_dqsn, and mem_dq into input-only pins.</p>
<p>The ALTMEMPHY megafunction does not support DDR3 SDRAM with a row address width of 12 bits. The MegaWizard Plug-In Manager does not enforce this restriction, and selecting this option will create a non-working design.</p>	<p>Select a row address width of 13 bits and make sure your design accesses only row addresses in the DDR3 SDRAM within the supported 12-bit address space.</p>
<p>The default t_{DS}, t_{DH}, t_{IS}, and t_{IH} parameters in the ALTMEMPHY and DDR2/DDR3 High Performance Controller MegaWizard Plug-in Manager may be too optimistic, and so the timing analysis is too optimistic. These values need to be adjusted based on the specifications of the memory device and their board slew rates.</p>	<p>Make sure that the memory parameters t_{DS}, t_{DH}, t_{IS}, and t_{IH} entered into the Megawizard are referenced to VREF instead of to VIH or VIL. Referencing to VREF should include the time for the signal to go from VREF to VIH/VIL. The nominal slew rate for our devices is 1 V/ns for single-ended outputs and 2 V/ns for differential outputs. The computation should be:</p> <p>(differential DQS) $t_{DS} = t_{DSa}(\text{base}) + \text{VIH}(\text{ac})_{\text{min}} / \text{DQ_slew_rate}$ (differential DQS) $t_{DH} = t_{DHa}(\text{base}) + \text{VIH}(\text{dc})_{\text{min}} / \text{DQ_slew_rate}$</p> <p>(single-ended DQS) $t_{DS} = t_{DS1a}(\text{base}) + (\text{VIH}(\text{ac})_{\text{min}} / \text{DQ_slew_rate}) + (\text{VIH}(\text{dc})_{\text{min}} / \text{DQS_slew_rate})$ (single-ended DQS) $t_{DH} = t_{DH1a}(\text{base}) + (\text{VIH}(\text{dc})_{\text{min}} / \text{DQ_slew_rate}) + (\text{VIH}(\text{dc})_{\text{min}} / \text{DQS_slew_rate})$</p> <p>$t_{IS} = t_{IS}(\text{base}) + \text{VIH}(\text{ac})_{\text{min}} / \text{addr_cmd_slew_rate}$ $t_{IH} = t_{IH}(\text{base}) + \text{VIH}(\text{dc})_{\text{min}} / \text{addr_cmd_slew_rate}$</p>

Issue	Workaround
<p>The calibration sequencer in the ALTMEMPHY megafunction for QDRII SRAM interfaces has been updated to make the calibration algorithm more robust under certain hardware conditions.</p>	<p>To guarantee reliable calibration, regenerate all QDRII and QDRII+ SRAM ALTMEMPHY variations in the Quartus II software version 8.0.</p>
<p>If you generate a DDR/DDR2/DDR3 HP Controller or ALTMEMPHY with Enable dynamic parallel on-chip termination (OCT) turned on, and then re-generate with it turned off, you will have the old OCT assignments still preset.</p>	<p>To avoid this issue, either remove all assignments from your project before running the assignments script from the re-generated project, or use the Pin Planner to apply the assignments in the first instance, and re-generate the assignments. The Pin Planner should then remove the old assignments when you update the IP instance.</p>
<p>If the PLL reference clock IO voltage does not match the IO voltage of your memory interface, you receive “no fit” errors on DDR/DDR2/DDR3 HP Controller or ALTMEMPHY of the form:</p> <pre>Error: Can't use clock type External Clock Output at location CLKCTRL PLLL2E1 for clock control block or source node <snip>altmemddr2_phy_alt_mem_phy_ clk_reset_siii:clk mem_clk_2x with clock type Dual-Regional Clock -- clock types do not match</pre>	<p>To resolve the issue, make sure to set an I/O standard on the PLL input clock that has the same voltage as that for your memory interface.</p>
<p>Cyclone III DDR/DDR2-SDRAM High Performance Controller IP generated prior to the Quartus II software version 8.0 will show the following warning message:</p> <pre>Read and write timing characteristics of memory interface <instance name> are preliminary .</pre>	<p>To remove the message, re-generate the memory interface using the IP generated in the Quartus II software version 8.0.</p>

Issue	Workaround
<p>Designs with the ALTMEMPHY megafunction created in the Quartus II software version 7.2 SP3 and earlier that target Stratix III devices for full-rate DDR or DDR2 SDRAM interfaces incorrectly handle incomplete write bursts causing the remaining write operations in the burst not to be masked due to the DM signals not being returned to the high state.</p>	<p>Re-generate the memory controller or ALTMEMPHY interface with the Quartus II software version 8.0.</p>
<p>Selecting Empty in the Netlist Type in the Design Partitions window for partitions containing the ALTMEMPHY megafunction is not supported for the Quartus II software version 8.0 and can lead to the following errors:</p> <p>Error: The following External Memory Interface related assignments are incorrect or inconsistent</p> <p>Error: The following External Memory Interface related assignments on "mem_dqs[XX]" are incorrect or inconsistent</p>	<p>Design partitions containing the ALTMEMPHY megafunction should not be assigned Empty in Netlist Type.</p>
<p>The Quartus II software does not automatically place the CK/CK# pins for DDR/DDR2/DDR3 memory interfaces on the same edge as the interface's DQ pins. As a result, you may see the following warning message:</p> <p>Critical Warning: Pin <CK pin> must be placed on a <edge> I/O to match the path of the read data pins</p>	<p>Place the specified CK pin on the specified edge of the device.</p>
<p>You cannot achieve timing closure for designs targeting Stratix III and Stratix IV devices running DDR3 SDRAM at 533MHz in -2 speed grades, and DDR2 SDRAM at 333MHz in -C4, -C4L, and -I4L speed grades at 1.1V.</p>	<p>These designs can be used for prototyping and testing but you should not go to production until Altera releases IP able to achieve these speeds. To meet timing at 333MHz in -C4, -C4L, and -I4L speed grades at 1.1V, use 400MHz-rated DDR2 memory and underclock it to run at 333MHz.</p>

Issue	Workaround
<p>The ALTMEMPHY megafunction does not guarantee timing closure when address and command signals are on a side that is across from the DQS/DQ pins (for example, DQS/DQ pins are on the top side and address/commands are on the bottom side of the device).</p>	<p>Some of the Stratix IV GX devices do not have user I/Os on the left/right I/O banks as the banks are used for transceivers, forcing the address and command signals to be in the same bank as the DQS/DQ pins limiting the width of your memory interface.</p>
<p>RLDRAM II Controller MegaCore functions that were generated in the Quartus II software versions 7.2 SP3 and earlier are missing timing constraints for the capture data between IOE and the FPGA fabric.</p>	<p>Regenerate the RLDRAM II Controller MegaCore function, and rerun DTW. For detail information, please refer to the <i>MegaCore IP Library Release Notes and Errata</i> on the Altera website.</p>
<p>The output toggling rate derating factors for the Differential 1.5-V, 1.8V, and 2.5-V SSTL-2 Class I and II I/O standards and the 1.2-V, 1.5-V, and 1.8-V Differential HSTL Class I and II I/O standards are too pessimistic when using 50 Ohms or 25 Ohms termination. This issue occurs when the output pin load is larger than 0. This may cause the TimeQuest Timing Analyzer to report minimum pulse width violations that should not be reported for these I/O standards and termination combinations. The minimum pulse width violation with type Port Rate can be ignored for the I/O with these I/O standards and termination combination.</p>	
<p>Stratix III designs using external memory interfaces may cause a compilation error if the data pins of your external memory interface use I/O pins on more than one side of the device. External memory interfaces with DQ pins exclusively bound in top, bottom, left, or right side I/O pins are not affected. The error message is "Error: Cannot place DQ I/O "mem_dq[nn]" to I/O location Pin Nn since its memory interface I/O group cannot be placed."</p>	<p>Altera recommends that data groups for external memory interfaces be grouped on a single side of your Stratix III FPGA. If you cannot group your DQ pins on a single side or if you want more information on this issue, contact Altera Technical Support at www.altera.com/mysupport and provide the reference number rd05232008_407.</p>
<p>The ALTMEMPHY megafunction does not currently support the Instantiate DLL externally option for DDR3 SDRAM. The MegaWizard does not enforce this restriction, and selecting this option will create a non-working design.</p>	

Issue	Workaround
Version 7.2 SP1	
<p>Designs with the ALTMEMPHY megafunction and that target Stratix II devices for 333 MHz DDR2 SDRAM interfaces may not meet setup timing on the postamble paths in a default compilation.</p>	<p>Re-generate the memory controller or ALTMEMPHY interface with the Quartus II software version 7.2 SP2. Place the registers manually on the resynchronization and postamble paths close to the I/O pins. Postamble setup slacks may be further increased in ~50 ps increments by applying the DQS Bus to Input Register Delay logic option in the Assignment Editor to the DQS pin names to increment the slack to the DQS pins in the interface, but with the trade-off cost of decreased postamble enable/disable setup slack. If you use the logic option to increase the delay, make sure your design meets timing on all postamble and postamble enable/disable paths.</p>
<p>The ALTMEMPHY megafunction does not support DDR SDRAM with CAS Latency setting 2.0 or 2.5 on the Stratix III device family. The MegaWizard does not enforce this restriction, and selecting this option will create a non-working design.</p>	<p>Use a CAS Latency setting of 3.0.</p>
Version 7.2	
<p>Automatic placement of the mimic path register in designs that contain ALTMEMPHY megafunctions may be sub-optimal.</p> <p>The DDR timing report shows a failing path from the CK memory clock output port to the mimic data metastable register. The Report DDR command in the TimeQuest Timing Analyzer labels this path as Mimic (Setup).</p>	<p>The destination register for this path needs to be placed manually:</p> <ol style="list-style-type: none"> 1. Make sure the mem_clk pins have been given location constraints. 2. Locate the destination register of the path by viewing the failing path in the TimeQuest analyzer and right-click Locate Path. Click Chip Planner. 3. Then find the mimic path register (its name ends in ...mimic_data_in_metastable) and drag it into a core register location, close to the mem_clk pin that drives it. 4. Recompile, and the path should now meet timing.

Issue	Workaround
<p>If you have, in the same project, more than one ALTMEMPHY variation generated in different versions of the Quartus II software, you may see a Verilog syntax error reported by synthesis. This error is caused by a common file used by all ALTMEMPHY variations, that has changed from an earlier version of the Quartus II software.</p>	<p>Open all the variations in the ALTMEMPHY MegaWizard in the latest version of the Quartus II software and regenerate them.</p>
<p>The Quartus II software version 7.2 does not support automatic placement of the write data clock output pins when you use the ALTMEMPHY megafunction.</p> <p>For Stratix III DDR/DDR2/DDR3 SDRAM High Performance Controllers, the Quartus II software automatically places the write data clock output pins correctly, but not for the QDRII+/QDRII SRAM ALTMEMPHY interface.</p>	<p>If your design targets Cyclone III or Stratix III devices, fix this issue by regenerating the memory interface IP in the Quartus II software version 8.0.</p> <p>However, if you use Pseudo x 36 mode for QDRII-SRAM or QDRII+-SRAM on Stratix III devices, place the mem_clk pin for clocking write data on a DQS pin for QDRII+/QDRII SRAM memory interfaces.</p>
<p>The Quartus II software version 7.2 does not support automatic placement of the clock output pins when you use the ALTMEMPHY megafunction.</p> <p>For Cyclone III devices, the Quartus II software does not correctly place the clock output pins for any memory interface type.</p>	<p>Place the mem_clk and mem_clk_n memory clock pins on DIFFOUT p- and n-pins.</p>
<p>Designs with the ALTMEMPHY megafunction that target Stratix II devices for 333MHz DDR2 SDRAM interfaces may not meet timing on the postamble paths in a default compilation.</p>	<p>Place the registers manually on the resynchronization and postamble paths close to the I/O pins. Some designs may require additional modification. For further assistance, contact Altera Technical Support by creating a Service Request at www.altera.com/mysupport and providing the reference number rd10182007_886.</p>

Issue	Workaround
Version 6.1	
<p>The assignments generated for the ALTMEMPHY megafunction, in the <code><variation_name>_pin_assignments.tcl</code> file, assume that the top-level pin names match the pins on the ALTMEMPHY variation. Using different names for your top level pins, including using single bit signals instead of one-bit busses, will result in incorrect behavior.</p>	<p>Use the Assignment Editor or Pin Planner to change the assignments to match the top-level pin names in your design.</p>

Simulation Model Changes

altera_mf Models

Model	Changes
altshift_taps	<ul style="list-style-type: none"> Added port <code>aclr</code> to asynchronously clear the memory, the <code>taps</code>, and <code>shiftout</code> output ports.
altsquare	<ul style="list-style-type: none"> Added support for new parameter <code>result_alignment</code> to specify the alignment on the result port.
dcfifo_mixed_widths	<ul style="list-style-type: none"> Added mixed-widths implementation support for LE based fifo.
altlvds_rx	<ul style="list-style-type: none"> Added support for port <code>rx_data_align_reset</code> in flexible LVDS in order to reset the data alignment circuitry. Added extra synchronization registers for flexible LVDS according to device families and deserialization factor. Increase the maximum number of supported LVDS channel for Stratix II device families to 132.
altlvds_tx	<ul style="list-style-type: none"> Use synchronization logic in the flexible LVDS to guarantee the bit position doesn't get varied each time PLL is reset.
altsyncram	<ul style="list-style-type: none"> Added "don't care" as read during write setting in BIDIR DUAL PORT mode for Stratix III and Cyclone III.

220model

Model	Changes
lpm_latch, lpm_counter, lpm_ff, lpm_shiftreg	<ul style="list-style-type: none"> Added more than 32 bits value support for parameter <code>lpm_avalue</code>, <code>svalue</code>, and <code>pvalue</code>.

Latest Known Quartus II Software Issues

For more information about known software issues, look for information in the **Quartus II Software Support** page at the following URL:

<http://www.altera.com/support/software/sof-quartus.html>

Software Issues Resolved

This section list the numbers of the Customer Service Requests that were fixed or otherwise resolved in this version of the Quartus II software.

Customer Service Request Numbers Resolved in this Release				
10548607	10599272	10621074	10624457	10624710
10626863	10631397	10632676	10636076	10639571
10640453	10640752	10642621	10644164	10644264
10644381	10644454	10644565	10645476	10645479
10645508	10645522	10645853	10647364	10648044
10648060	10648577	10648729	10648752	10648900
10648996	10649144	10649151	10649409	10649656
10649673	10649856	10650054	10650082	10650539
10650570	10650586	10650726	10651105	10651558
10652155	10652232	10652428	10653334	10653393
10654051				

Revision History

Revision	Description
1.0	Initial Release

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