



Quartus II Device Support Release Notes

October 2008

Quartus II version 8.1

This document provides late-breaking information about device support in this version of the Altera® Quartus® II software. For information about memory, disk space, and system requirements, refer to the **readme.txt** file in your **altera/<version number>/quartus** directory. For information about New Features, EDA Tool version support, and existing and resolved software issues, refer to the *Quartus II Software Release Notes*.

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Device Support & Pin-Out Status

This section contains information about the status of support in the Quartus II software for the devices listed.

Advance Device Support

Compilation, simulation, and timing analysis support is provided for the following devices that will be released in the near future. Although the Compiler generates pin-out information for these devices, it does not generate programming files for them in this release.

Devices with Advance Support

Device Family	Devices	
Stratix® IV	EP4SGX70	EP4SGX110
	EP4SGX230	EP4SGX290
	EP4SGX360	EP4SGX530

Initial Information Support

Compilation, simulation, and timing analysis support is provided for the following devices that will be released in the near future. Programming files and pin-out information, however, are not generated for these devices in this release.

Devices with Initial Information Support

Device Family	Devices
Stratix IV	EP4SE530

Timing and Power Models

This section contains a summary of timing and power model status in the current version of the Quartus II software.

Devices with Timing and Power Models (Part 1 of 3)

Device Family	Device	Timing Model Status	Power Model Status
Arria® GX	EP1AGX20	Final – 7.2	Final – 7.2
	EP1AGX35	Final – 7.2	
	EP1AGX50	Final – 7.2	
	EP1AGX60	Final – 7.2	
	EP1AGX90	Final – 7.2	

Devices with Timing and Power Models (Part 2 of 3)

Device Family	Device	Timing Model Status	Power Model Status
Cyclone® II ⁽¹⁾	EP2C5	Final – 6.0	Final – 6.0
	EP2C8	Final – 5.1 SP2	
	EP2C15	Final – 6.0	
	EP2C20	Final – 5.1 SP2	
	EP2C35	Final – 5.1 SP2	
	EP2C50	Final – 6.0	
	EP2C70	Final – 5.1 SP2	
Cyclone III	EP3C5	Final – 8.0 SP1	Final – 8.1
	EP3C10	Final – 8.0 SP1	
	EP3C16	Final – 8.0 SP1	
	EP3C25	Final – 7.2 SP1	
	EP3C40	Final – 8.0	
	EP3C55	Final – 8.0	
	EP3C80	Final – 8.0	
	EP3C120	Final – 7.2 SP1	
HardCopy® II	HC210	Correlated – 8.0	Correlated – 7.2
	HC210W		
	HC220		
	HC230		
	HC240		
MAX® IIZ	EPM240Z	Preliminary	Preliminary
	EPM570Z		
Stratix II	EP2S15	Final – 5.0 SP1	Final – 6.0
	EP2S30	Final – 5.0	
	EP2S60	Final – 5.0	
	EP2S90	Final – 5.0 SP1	
	EP2S130	Final – 5.0 SP1	
	EP2S180	Final – 5.1	
Stratix II GX	EP2SGX30	Final – 7.0	Final – 7.1
	EP2SGX60	Final – 7.0	
	EP2SGX90	Final – 6.1	
	EP2SGX130	Final – 6.1	

Devices with Timing and Power Models (Part 3 of 3)

Device Family	Device	Timing Model Status	Power Model Status
Stratix III ⁽²⁾	EP3SE50	Preliminary	Preliminary
	EP3SE80	Final – 8.1	
	EP3SE110	Final – 8.1	
	EP3SE260	Preliminary	
	EP3SL50	Preliminary	
	EP3SL70	Preliminary	
	EP3SL110	Final – 8.1	
	EP3SL150	Final – 8.1	
	EP3SL200	Preliminary	
	EP3SL340	Final – 8.1	
Stratix IV	EP4SGX70	Preliminary	Preliminary
	EP4SGX110	Preliminary	
	EP4SGX230	Preliminary	
	EP4SGX290	Preliminary	
	EP4SGX360	Preliminary	
	EP4SGX530	Preliminary	
	EP4SE530	Preliminary	

⁽¹⁾ Automotive (“A”) temperature grade EP2C15 device timing models were preliminary in the Quartus II software version 7.2 SP1.

⁽²⁾ For the listed Stratix III devices, portions of the timing models used for DDR3 timing analysis are not final in the Quartus II software version 8.1.

The current version of the Quartus II software also includes final timing models for the ACEX[®] 1K, APEX[®] 20K, APEX 20KE, APEX 20KC, APEX II, Cyclone, FLEX[®] 6000, FLEX 10K, FLEX 10KA, FLEX 10KE, MAX 7000S, MAX II, Stratix, and Stratix GX device families. Timing models for these device families became final in the Quartus II software versions 5.0 and earlier.

The current version of the Quartus II software also includes final power models for the Cyclone, MAX 3000A, MAX 7000AE, MAX 7000B, MAX II, Stratix, and Stratix GX device families. Power models for these device families became final in the Quartus II software versions 5.1 and earlier.

The Quartus II software version 8.1 delivers final timing models for automotive grade devices in the MAX, MAX II, and Cyclone device families.

Changes in Device Support

DPA lock issue

In the Quartus II software version 8.1, LVDS receivers using DPA mode must use the `FIFORESET` port to clear the DPA FIFO upon DPA lock; otherwise, the Quartus II software issues error messages relating to LVDS/DPA `FIFORESET` connectivity. If using the soft-DPA lock generated by the MegaWizard Plug-In Manager, you must regenerate the LVDS receivers using DPA in the Quartus II software version 8.1. For more information, refer to the Stratix III Device Handbook.

Applies to: Stratix III devices

DDR memory interface timing model updated

The timing model for DDR memory interfaces for Cyclone III devices in industrial grade has been updated for greater accuracy and higher performance. No design change is needed.

Applies to: Cyclone III devices

PLL settings update

The Quartus II software has removed the 12uA from the valid charge pump settings for M=3 to M=15 (both inclusive) for PLLs in Stratix II, Stratix II GX, Arria GX, and HardCopy II devices. This change improves the compensation variability seen in certain PLL configurations. No design change is needed. The Quartus II software will apply the updated settings during compilation.

Applies to: Stratix II, Stratix II GX, Arria GX, and HardCopy II devices

DSP block performance

The Cyclone III timing models are updated to provide higher performance in DSP blocks. This change affects timing models that were previously finalized. No design change is needed.

Applies to: Cyclone III devices

Voltage drop in single-ended I/O standards when using dedicated differential I/O pins on sides

The Quartus II software version 8.0 incorrectly enables an internal resistor between two I/Os of a side-dedicated differential input I/O pair when each I/O is used as a single-ended I/O and the current strength is not specified, or the input or output **Termination** option for the I/O is enabled. If both I/Os in this pair are input only, the internal resistor is enabled incorrectly only if an input

Termination option for either input is enabled. This resistor may cause the I/O pin to malfunction when it is single ended by reducing the complementary pin voltage. This issue is fixed in the Quartus II software version 8.0 SP1.

Applies to: Stratix III devices

Stratix III and Stratix IV LVDS Data Rate specification

The Quartus II software version 8.0 has incorrect LVDS data rate specifications for Stratix III and Stratix IV devices that use C4, I4L, and C4L speed grades (high and low core voltage). These specifications should be 1040 Mbps, not 1250 Mbps. This issue is fixed in the Quartus II software version 8.0 SP1.

Applies to: Stratix III and Stratix IV devices

Stratix IV LAB counts changed

The Quartus II software version 8.0 shows incorrect LAB counts for Stratix IV devices. This issue is fixed in the Quartus II software version 8.0 SP1.

Applies to: Stratix IV devices

Stratix III pseudo LVDS toggling rate updated

The Stratix III Row I/O output toggling rate of pseudo LVDS standards (**LVDS 1R and 3R, RSDS 1R and 3R, mini-LVDS 1R and 3R**) has been updated in the Quartus II software version 8.0 SP1.

Applies to: Stratix III devices

Revision History

Revision	Description
1.0	Initial Release

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