

This document provides late-breaking information about device support in this version of the Altera® Quartus® II software. For information about disk space and system requirements, refer to the **readme.txt** file in your **altera/<version number>/quartus** directory. For information about New Features, EDA Tool version support, and existing and resolved software issues, refer to the *Quartus II Software Release Notes*.

This document contains the following sections:

- “Device Support & Pin-Out Status” on page 1
- “Memory Requirements/Recommendations” on page 2
- “Timing and Power Models” on page 4
- “Cyclone III Timing Analysis Updates” on page 6
- “Stratix III Timing Model Changes” on page 7
- “Changes in Device Support” on page 8

## Device Support & Pin-Out Status

This section contains information about the status of support in the Quartus II software for the devices listed.

### Advance Device Support

Compilation, simulation, and timing analysis support is provided for the following devices that will be released in the near future. Although the Compiler generates pin-out information for these devices, it does not generate programming files for them in this release.

#### Devices with Advance Support

Device Family	Devices	
Arria® II GX	EP2AGX20	EP2AGX30
	EP2AGX45	EP2AGX65
	EP2AGX95	EP2AGX125
	EP2AGX190	EP2AGX260
Stratix® IV	EP4SE230	EP4SE530
	EP4SGX70	EP4SGX110
	EP4SGX180	EP4SGX290
	EP4SGX230(1)	EP4SGX360
	EP4SGX530(1)	

(1) Full compilation, simulation, timing analysis, and programming support is now available for EP4SGX230 ES and EP4SGX530 ES.

## Initial Information Support

Compilation, simulation, and timing analysis support is provided for the following devices that will be released in the near future. Programming files and pin-out information, however, are not generated for these devices in this release.

### Devices with Initial Information Support

Device Family	Devices	
Stratix IV	EP4S40G2	EP4S40G5
	EP4S100G2	EP4S100G5

## Compilation Support

Compilation support with preliminary timing and power analysis support is provided for the following HardCopy III and HardCopy IV devices.

### Devices with Compilation Support

Device Family	Devices	
HardCopy III	HC311	HC321
	HC322	HC331
	HC332	HC351
	HC352	HC361
	HC362	HC371
	HC372	
HardCopy IV	HC4E31	HC4E62

## Memory Requirements/Recommendations

A full installation of the Altera Complete Design Suite version 9.0 SP1 requires approximately 7.8 GB of available disk space on the drive or partition where you are installing the Altera Complete Design Suite and approximately 30 MB of available space on the drive that contains your TEMP directory (Windows only).

The Quartus II Stand-Alone Programmer requires a minimum of 1 GB of RAM plus additional memory, based on the size and number of SOF files and the size and number of devices being configured.

Altera recommends that your system be configured to provide swap space (virtual memory) equal to the recommended physical RAM that is required to process your design.

The following table shows the memory required to process designs targeted for Altera devices.

**Table 1.** Memory Requirements/Recommendations (Part 1 of 2)

Device	Recommended Physical RAM	
	32-bit	64-bit
All ACEX <sup>®</sup> 1K APEX <sup>™</sup> 20K, APEX 20KE & APEX 20KC (EP20K30E, EP20K60E, EP20K100/100E, EP20K160E, EP20K200/200C/200E, EP20K300E, EP20K400/400C/400E, EP20K600C/600E) APEX II (EP2A15, EP2A25, EP2A40) Arria GX (EP1AGX20C) Cyclone <sup>®</sup> (EP1C3, EP1C4, EP1C6, EP1C12, EP1C20) Cyclone II (EP2C5, EP2C8, EP2C20) Cyclone III (EP3C5, EP3C10, EP3C16, EP3C25, EP3C40) All FLEX <sup>®</sup> 6000, FLEX 10KE, FLEX 10KA HardCopy <sup>®</sup> Stratix (HC1S25) All MAX <sup>®</sup> 3000A All MAX 7000 All MAX 7000AE All MAX 7000B All MAX 7000S All MAX series and MAX II device families Stratix (EP1S10, EP1S20) Stratix GX (EP1SGX10) Stratix II (EP2S15)	512 MB	512 MB
Cyclone III (EP3C55, EP3C80)	768 MB	1.0 GB
APEX 20KE & APEX 20KC (EP20K1000C/1000E, EP20K1500E) Cyclone II (EP2C35, EP2C50) Cyclone III (EP3C120) HardCopy Stratix (HC1S30, HC1S40, HC1S60) Stratix (EP1S25, EP1S30, EP1S40, EP1S60) Stratix GX (EP1SGX25, EP1SGX40) Stratix II (EP2S30) Stratix II GX (EP2SGX30, EP2SGX60) Stratix III (EP3SL50, EP3SE50, EP3SL70) Arria GX (EP1AGX35C, EP1AGX35D, EP1AGX50D, EP1AGX60C, EP1AGX60D, EP1AGX60E)	1.0 GB	1.5 GB

**Table 1.** Memory Requirements/Recommendations (Part 2 of 2)

Device	Recommended Physical RAM	
	32-bit	64-bit
APEX II (EP2A70) Cyclone II (EP2C70) HardCopy Stratix (HC1S80) HardCopy II (HC210) Stratix (EP1S80) Stratix II (EP2S60, EP2S90) Stratix II GX (EP2SGX90) Stratix III (EP3SE80) Arria GX (EP1AGX90E) Stratix IV (EP4SGX70)	1.5 GB	2.0 GB
Stratix II (EP2S130, EP2S180) Stratix II GX (EP2SGX130) HardCopy II (HC220, HC230, HC240) Stratix III (EP3SL110, EP3SE110, EP3SE150, EP3SL200) Stratix IV (EP4SGX110, EP4SGX230)	3.0 GB	4.0 GB
Stratix III (EP3SE260, EP3SL340) Stratix IV (EP4GS290)	4.0 GB	6.0 GB
Stratix IV (EP4SGX360, EP4SGX530, EP4SE530) HardCopy III HardCopy IV (HC4E31)	N/A	8.0 GB
HardCopy IV (HC4E62)	N/A	12.0 GB

## Timing and Power Models

This section contains a summary of timing and power model status in the current version of the Quartus II software.

**Table 2.** Devices with Timing and Power Models (Part 1 of 3)

Device Family	Device	Timing Model Status	Power Model Status
Arria GX	EP1AGX20	Final – 7.2	Final – 7.2
	EP1AGX35	Final – 7.2	
	EP1AGX50	Final – 7.2	
	EP1AGX60	Final – 7.2	
	EP1AGX90	Final – 7.2	

**Table 2.** Devices with Timing and Power Models (Part 2 of 3)

Device Family	Device	Timing Model Status	Power Model Status
Aria II GX	EP2AGX20	Preliminary	Preliminary
	EP2AGX30		
	EP2AGX45		
	EP2AGX65		
	EP2AGX95		
	EP2AGX125		
	EP2AGX190		
	EP2AGX260		
Cyclone II(1)	EP2C5	Final – 6.0	Final – 6.0
	EP2C8	Final – 5.1 SP2	
	EP2C15	Final – 6.0	
	EP2C20	Final – 5.1 SP2	
	EP2C35	Final – 5.1 SP2	
	EP2C50	Final – 6.0	
	EP2C70	Final – 5.1 SP2	
	Cyclone III	EP3C5	
EP3C10		Final – 8.0 SP1	
EP3C16		Final – 8.0 SP1	
EP3C25		Final – 7.2 SP1	
EP3C40		Final – 8.0	
EP3C55		Final – 8.0	
EP3C80		Final – 8.0	
EP3C120		Final – 7.2 SP1	
HardCopy II	HC210	Correlated – 8.0	Correlated – 7.2
	HC210W		
	HC220		
	HC230		
	HC240		
	HardCopy III		
HardCopy IV-E	(All)	Preliminary	Preliminary
MAX IIZ	EPM240Z	Final – 9.0 SP1	Final – 9.0 SP1
	EPM570Z		
Stratix II	EP2S15	Final – 5.0 SP1	Final – 6.0
	EP2S30	Final – 5.0	
	EP2S60	Final – 5.0	
	EP2S90	Final – 5.0 SP1	
	EP2S130	Final – 5.0 SP1	
	EP2S180	Final – 5.1	

**Table 2.** Devices with Timing and Power Models (Part 3 of 3)

Device Family	Device	Timing Model Status	Power Model Status
Stratix II GX	EP2SGX30	Final – 7.0	Final – 7.1
	EP2SGX60	Final – 7.0	
	EP2SGX90	Final – 6.1	
	EP2SGX130	Final – 6.1	
Stratix III (2)	EP3SE50	Final – 9.0	Final – 9.0
	EP3SE80	Final – 8.1	
	EP3SE110	Final – 8.1	
	EP3SE260	Final – 9.0	
	EP3SL50	Final – 9.0	
	EP3SL70	Final – 9.0	
	EP3SL110	Final – 8.1	
	EP3SL150	Final – 8.1	
	EP3SL200	Final – 9.0	
	EP3SL340	Final – 8.1	
Stratix IV	EP4SE230	Preliminary	Preliminary
	EP4SGX70		
	EP4SGX110		
	EP4SGX180		
	EP4SGX230		
	EP4SGX290		
	EP4SGX360		
	EP4SGX530		
	EP4SE530		

(1) Automotive (“A”) temperature grade EP2C15 device timing models were preliminary in the Quartus II software version 7.2 SP1.

(2) See also “Stratix III Timing Model Changes”.

The current version of the Quartus II software also includes final timing models for the ACEX 1K, APEX 20K, APEX 20KE, APEX 20KC, APEX II, Cyclone, FLEX 6000, FLEX 10K, FLEX 10KA, FLEX 10KE, MAX II, MAX 7000S, Stratix, and Stratix GX device families. Timing models for these device families became final in the Quartus II software versions 5.0 and earlier.

The current version of the Quartus II software also includes final power models for the Cyclone, MAX II, MAX 3000A, MAX 7000AE, MAX 7000B, Stratix, and Stratix GX device families. Power models for these device families became final in the Quartus II software versions 5.1 and earlier.

The Quartus II software version 8.1 delivers final timing models for automotive grade devices in the MAX, MAX II, and Cyclone device families.

## Cyclone III Timing Analysis Updates

This section details all Cyclone III timing analysis updates in the Quartus II software.

## Changes in the Quartus II version 9.0 SP1

The Cyclone III timing analysis has been updated in the Quartus II software version 9.0 SP1. The clock enable path to the M9K was not analyzed in the Quartus II software version 9.0 and earlier for certain M9K configurations. This issue has been fixed in the Quartus II software version 9.0 SP1. The performance of most designs is not significantly affected by this change.

For details, search the Altera Knowledge Database with Solution ID [rd04302009\\_15](#).

**Applies to:** Cyclone III devices

## Stratix III Timing Model Changes

This section details all Stratix III timing model updates in the Quartus II software.

### Changes in the Quartus II software version 9.0 SP1

The Stratix III timing models have been updated in the Quartus II software version 9.0 SP1 for the following reasons:

- Added a clock enable path to the M9K and M144K timing models that was missing in the Quartus II software version 9.0 and earlier.
- Corrected the T4 (DDIO\_MUX) timing models to accurately analyze timing on DDIO output paths.
- Corrected the write leveling delay chain timing models to eliminate the possibility of hardware functional failures in designs implementing DDR3 interfaces with leveling.

For details, search the Altera Knowledge Database with Solution ID [rd04292009\\_804](#).

**Applies to:** Stratix III devices

### Changes in the Quartus II software version 9.0

The Stratix III timing models have been updated in the Quartus II software version 9.0 to allow for the following:

- Enable faster 800MHz PLL performance on C2 parts (vs. 717MHz)
- Enable superior 1.6Gbps LVDS/DPA performance (vs. 1.25Gbps)
- Enable committed high performance DDR3 up to 533MHz

The Stratix III timing model updates require a recompilation of existing designs with the Quartus II software version 9.0 in order to achieve the following:

- Eliminate significant possibility of functional failure for 3S340 LVDS Rx SERDES designs
- Eliminate possible functional failures for those designs using MLAB in New Data or Old Data modes with a skewed or locally routed clock

Refer to the *Stratix III Device Family Errata Sheet* on the Altera website for more information.

**Applies to:** Stratix III devices

## Changes in Device Support

### Downgraded Memory Interface Hybrid support on Arria II GX

In the Quartus II software version 9.0, fitting is supported for “hybrid” memory designs—designs in which DQ/DQS pin groups are split between VIO and HIO for a single memory interface. However, the I/O performance is degraded in this mode compared to using only VIO or only HIO.

**Applies to:** Arria II GX devices

### Cyclone III Maximum Clock Rate updated

The maximum clock rate for DDR2 memory interfaces with Hybrid mode for the -6 speed grade has been updated from 150 to 167 MHz.

**Applies to:** Cyclone III devices

### Change in HardCopy II Minimum Timing for Internal DSP transfers on the Military speed grade

The timing models for internal DSP transfers have had some pessimism removed on the Military minimum timing corner.

This change does not have any negative impact on any designs because these paths are internal to the DSP, but may remove false failures in the reported timing for internal DSP transfers on the Military minimum timing corner.

**Applies to:** HardCopy II devices

### LVDS\_RX and LVDS\_TX minimum period incorrect

The Minimum Pulse Width (MPW) for the LVDS\_RX and LVDS\_TX blocks of the Stratix III C2 parts under the faster corner timing model of all densities are incorrectly reported in the Quartus II software version 8.1. The MPW should be set to 625ps (to support 1.6Gbps), but the value is incorrectly set to 800ps (to support 1.25Gbps.) Designs that target Stratix III C2 parts and use LVDS\_RX or LVDS\_TX with data rates between 1.25Gbps and 1.6Gbps will see erroneous MPW violations reported by the TimeQuest Timing Analyzer. Designs that use the Stratix III C2 parts and have LVDS\_RX or LVDS\_TX will now have the correct MPW value and have more slack at the fast corner timing analysis. In the updated timing models, designs without LVDS\_RX or LVDS\_TX are not affected.

**Applies to:** Stratix III devices

### DPA lock issue

In the Quartus II software version 8.1 and later, LVDS receivers using DPA mode must use the FIFORESET port to clear the DPA FIFO upon DPA lock; otherwise, the Quartus II software issues error messages relating to LVDS/DPA FIFORESET connectivity. If using the soft-DPA lock generated by the MegaWizard Plug-In Manager, you must regenerate the LVDS receivers using DPA in the Quartus II software version 8.1. For more information, refer to the *Stratix III Device Handbook*.

**Applies to:** Stratix III devices

## Stratix IV timing model updated

The Stratix IV EP4SE530 and EP4SGX530 device timing for the C2 speed grade reported by the Quartus II software version 9.0 SP1 is 5% faster than the device actual performance. As a result, the timing should be derated by 5% after a design timing analysis to ensure device functionality. The timing models for these devices will be corrected in a future release of the Quartus II software.

**Applies to:** Stratix IV devices

## Migration devices with PCI Express hard IP

When one of the Stratix IV GX EP4SGX530KH40 devices (1517 pin count) is used with migration to smaller devices (180, 230, 290, 360), the Quartus II software does not automatically restrict the number of usable PCI Express hard IP blocks. In order to successfully migrate to smaller devices, the top two hard IP blocks (one per side), as seen in the floorplan, should not be used by the design. The location names of those hard IP blocks are PCIEHIP\_X0\_Y52\_N134 and PCIEHIP\_X185\_Y52\_N134.

**Applies to:** Stratix IV devices

## VCCH issues for Stratix IV GT devices

In Stratix IV GT devices, if a quad has no transmit channels, the receivers in that quad call for VCCH voltage setting of 1.5 V. Although this behavior is legal, it creates an extra power plane on your board, and so you should use VCCH voltage setting of 1.4 V for all Stratix IV GT devices.

In Stratix IV GT devices, if a quad has transmit channels, it is possible to make a **1.5-V PCML** I/O standard assignment to those channels. This assignment causes VCCH voltage setting of 1.5 V, which in turn causes an internal error in the PowerPlay Power Analyzer, although normal compilation runs without errors. To avoid this internal error, do not make an I/O standard assignment to those channels, or use a **1.4-V PCML** I/O standard assignment.

**Applies to:** Stratix IV GT devices

## PCI Express Gen2 Signal Detect Issue

In the Quartus II software version 9.0, the software used incorrect settings to configure the Receiver Signal Detect feature for PCI Express Gen2 applications. The issue is fixed in the Quartus II software version 9.0 SP1.

**Applies to:** Stratix IV GX devices

## Power down settings ignored

The **VCCHIP\_R power** and **VCCHIP\_L power** options are not supported in the Quartus II software version 9.0 SP1. The **Opportunistically power off** setting is not available; the **Power on** setting will be used instead.

**Applies to:** Stratix IV GX and Stratix IV GT devices

## **Stratix IV ES Errata restrictions enforced**

The Quartus II software version 9.0 SP1 enforces frequency and bonding limits for Stratix IV GX and Stratix IV GT ES devices as described in the "x8 and xN Clock Line Timing Issue for Transceivers" entry in the Stratix IV GX ES Errata Sheet and the Stratix IV GT ES Errata Sheet. The PCI Express (PIPE) limitations are not enforced.

**Applies to:** Stratix IV GX and Stratix IV GT devices