

This document provides late-breaking information about the following areas of the Altera® Quartus®II software version 9.1. For information about memory, disk space, system requirements, and device support in this version of the Quartus II software, along with the latest information about timing and power models, refer to the Quartus II Device Support Release Notes on the Altera website at: <http://www.altera.com/literature/lit-rn.jsp>.

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## New Features & Enhancements

The Quartus II software version 9.1 includes the following new features and enhancements:

- The Rapid Recompile option, which reduces compilation time and improves timing preservation when making small design changes. You can use the Rapid Recompile option in place of or together with creating design partitions to preserve placement and routing results from a previous compilation.
- You can use non-rectangular LogicLock regions to create more compact and efficient floorplans.
- Avalon Verification IP components in SOPC Builder allow you to simulate the behavior of IP created for SOPC Builder systems and to monitor Avalon interface traffic. You can also perform Avalon Memory Map or Avalon Streaming Protocol assertion checking.
- The Quartus II software version 9.1 provides VHDL 2008 initial support.
- The IP library includes improved DDR2, DDR3, QDR II+, and RLDRAM II memory controllers.
- The Pin Advisor has been enhanced to include information on how to use the Quartus II software to generate more accurate and less pessimistic Simultaneous Switching Noise (SSN) results.

- The Quartus II software version 9.1 supports the following new megafunctions:
  - altotp megafunction
  - altfp\_matrix\_inv megafunction

The Quartus II software version 9.1 adds support for the following devices:

- Initial information support for these Cyclone IV GX devices: EP4CGX15, EP4CGX22, EP4CGX30
- Advance support for these Cyclone III LS devices: EP3CLS70, EP3CLS100
- Advance support for these HardCopy IV GX devices: HC4GX15, HC4GX25, HC4GX35
- Advance support for these Stratix IV devices: EP4SE360, EP4SE820, EP4S40G5, EP4S100G3, EP4S100G4, EP4S100G5, EP4SGX70HF35, EP4SGX110HF35, EP4SGX290KF43, EP4SGX290NF45, EP4SGX360KF43, EP4SGX360NF45, EP4SGX530KF43
- Full support for these Arria II GX devices: EP2AGX45, EP2AGX65, EP2AGX125ES
- Full support for these Cyclone III LS devices: EP3CLS150, EP3CLS200
- Full support for these HardCopy III devices: HC325, HC335
- Full support for these Stratix IV devices: EP4SE530ES, EP4SGX180, EP4SGX230, EP4SGX530ES, EP4S40G2, EP4S100G2

## EDA Interface Information

The Quartus II software version 9.1 supports the following EDA tools:

<b>Synthesis Tools</b>	<b>Version</b>	<b>NativeLink Support</b>
Synopsys Synplify & Synplify Pro	C-2009.06	✓
Mentor Graphics Precision RTL Synthesis	2009a	✓
Mentor Graphics LeonardoSpectrum	2009a	✓
Synopsys Design Compiler	2004.12-SP4	
Mentor Graphics DK Design Suite	5.0 SP5	✓
<b>Simulation Tools</b>	<b>Version</b>	<b>NativeLink Support</b>
Mentor Graphics ModelSim	6.5b	✓
Mentor Graphics ModelSim-Altera	6.5b	✓
Mentor Graphics ModelSim-Altera Starter Edition	6.5b	✓
Cadence NC-Sim	8.2 (Linux only)	
Synopsys VCS / VCS MX	Y-2009.06-SP1	✓
Aldec Active-HDL	8.1-SP2 (Windows only)	✓
Aldec Riviera-PRO	2009.06	✓
<b>Formal Verification Tools (Equivalence Checking)</b>	<b>Version</b>	<b>NativeLink Support</b>
Cadence Encounter Conformal	8.1	
<b>Chip Level Static Timing Analysis</b>	<b>Version</b>	<b>NativeLink Support</b>
Synopsys PrimeTime	Z-2007.06	✓
<b>Board Level Static Timing Analysis</b>	<b>Version</b>	<b>NativeLink Support</b>
Mentor Graphics TAU	3.7	
<b>Board Level Symbol/Pin-out Management</b>	<b>Version</b>	<b>NativeLink Support</b>
Mentor Graphics I/O Designer	7.3	

## Changes to Software Behavior

This section documents instances in which the behavior and default settings of this release of the Quartus II software have been changed from earlier releases of the software.

Items listed in the following table represent cases in which the behavior of the current release of the Quartus II software is different from a previous version.

Description	Workaround
ACEX, APEX, FLEX, and HardCopy Stratix device families are not provided with the Quartus II software version 9.1.	Use the Quartus II software version 9.0 SP2 or earlier to support those devices. The Quartus II software version 9.0 and the associated service packs will remain available on the Altera website ( <a href="http://www.altera.com">http://www.altera.com</a> ).
The Simulator and the Waveform Editor will not be provided in future versions of the Quartus II software beginning with version 10.0	Use the Quartus II software version 9.1 or earlier or use a third-party EDA simulator and waveform editor.
For Arria II GX, Cyclone III, Cyclone IV, HardCopy III, HardCopy IV, Stratix III, and Stratix IV devices, Analysis and Synthesis performs timing-driven synthesis by default.	To turn off timing-driven synthesis, Turn off <b>Timing-Driven Synthesis</b> on the <b>Analysis and Synthesis</b> page of the <b>Settings</b> dialog box.
<p>Changes to the default assignment settings in the Quartus II software include the following:</p> <ul style="list-style-type: none"> <li>■ The default value of PARALLEL_SYNTHESIS has changed to <b>On</b>.</li> <li>■ For Arria II GX, Cyclone III, Cyclone IV GX, HardCopy III, HardCopy IV, Stratix III, and Stratix IV devices, the default value of SYNTH_TIMING_DRIVEN_SYNTHESIS has changed to <b>On</b>.</li> </ul>	
<p>Changes to TimeQuest Timing Analyzer behavior in the Quartus II software version 9.1 include the following:</p> <ul style="list-style-type: none"> <li>■ <b>set_max_skew</b> now includes utsu, uth, utco, from_clock, to_clock, and clock_uncertainty.</li> <li>■ In designs that target Stratix III devices, if ENA_REGISTER_MODE of the ena port is set to DOUBLE_REGISTER, the internal register-to-register timing of the enable signal is guaranteed by design and is excluded from timing analysis.</li> <li>■ Stratix III I4 timing models have been updated in the Quartus II software versions 9.0 SP2 and 9.1. Only timing delays in Low Power mode LABs and Low Power mode MLABs in I4 industrial speed grade devices are affected. This change in the timing models may affect your static timing analysis and fitting result. Existing designs that target Stratix III I4 devices might exhibit some degradation in performance after timing analysis with the TimeQuest Timing Analyzer in the Quartus II software version 9.1. However, a full recompilation of the design removes any degradation in performance. Other speed grade devices (I3 and I4L at 1.1V; I4L at 0.9V; and all commercial speed grades) are not affected.</li> </ul>	<p>If your design works correctly in your hardware system, Altera recommends that you take no action. Otherwise, Altera recommends that you fully recompile the design.</p>
Mentor Graphics ModelSim-Altera Edition no longer includes the alt_vtl library used to simulate MAX+PLUS II designs.	Use the alt_vtl library from the Mentor Graphics ModelSim-Altera Edition version 6.4a.

Description	Workaround
In designs that target Stratix IV devices, altgx megafunction instances created with the <b>Use external termination</b> option turned on in the Quartus II software version 9.0 and earlier did not disable internal termination. The Quartus II software version 9.1 disables internal termination when the <b>Use external termination</b> option is turned on.	This change in software behavior decreases the resistance in designs that use external termination and may change measured signal characteristics compared to those measured in previous versions of the Quartus II software. This change in software behavior does not affect designs that use internal termination.
Starting in the Quartus II software version 9.1, an altgx megafunction generates only a 1-bit rateswitch port for PCIe Gen 2 x4/x8 configurations. In previous versions of the Quartus II software, an altgx megafunction generated 4- or 8-bit rateswitch ports, of which only bit 0 was used.	

## Known Issues & Workarounds

### General Quartus II Software Issues

Issue	Workaround
<p>The Quartus II software version 9.1 does not correctly synthesize variable part select with two-dimensional arrays. For example, the following Verilog statements are not synthesized correctly:</p> <pre>logic s[3:0] ; logic [0:w-1][3:0]m ; s = m[i+1];</pre>	<p>Do not use variable part select with two-dimensional arrays. Use multiple constant part selects such as <code>m[2+:1]</code>, and then choose from them.</p>
<p>The Quartus II software version 9.1 does not correctly synthesize <code>disable</code> statements when the <code>disable</code> statement refers to a labeled statement. For example, the following Verilog statements are not synthesized correctly:</p> <pre>lbl: out1 ,=r1^r2; disable lbl;</pre>	<p>Rewrite your code so that the statement is surrounded by a begin-end block and name the block after the begin keyword. For example, the following is synthesized correctly:</p> <pre>begin: lbl     out1 &lt;=r1^r2;     disable lbl; end;</pre>
<p>Running Partition Merge after importing a design with empty partitions created with a previous version of the Quartus II software results in the following error:</p> <pre>Error: Missing required database file.</pre>	<p>Run Analysis and Synthesis before running Partition Merge.</p>
<p>For the <code>altfb_matrix_mult</code> megafunction, the maximum column and row sizes for input matrices is limited to 64.</p>	
<p>If you attempt to add the <code>altfb_matrix_mult</code> megafunction to your project with the MegaWizard Plug-In Manager, the MegaWizard Plug-In Manager fails to add the <code>altfpc_lib</code> library to your project.</p>	<p>Manually include the <b>altfpc_lib.v</b> or <b>altfpc_lib.vhd</b> file in the project.</p>
<p>If you attempt to add the <code>altfb_matrix_inv</code> megafunction to your project with the MegaWizard Plug-In Manager, the MegaWizard Plug-In Manager fails to add the <code>altfpc_lib</code> library to your project.</p>	<p>Manually include the <b>altfpc_lib.v</b> or <b>altfpc_lib.vhd</b> file in the project.</p>

Issue	Workaround
<p>The altfp_convert megafunction fixed-point-to-floating-point and floating-point-to-fixed-point features are supported only from a command prompt.</p>	<p>To create an altfp_convert megafunction that converts a single precision value to a Q16.16 fixed point value for a design that targets a Stratix III device, type the following at a command prompt:</p> <pre>clearbox cbx_altfp_convert CBX_AUTO_BLACKBOX=ALL OPERATION=FLOAT2FIXED WIDTH_EXP_INPUT=8 WIDTH_MAN_INPUT=23 WIDTH_INT=16 WIDTH_RESULT=32 DEVICE_FAMILY=STRATIXIII clock dataa result cbx_file=float2fixed.v</pre> <p>To create an altfp_convert megafunction that converts a Q16.16 fixed point value to a single precision value, type the following at a command prompt:</p> <pre>clearbox cbx_altfp_convert CBX_AUTO_BLACKBOX=ALL OPERATION=FIXED2FLOAT WIDTH_EXP_OUTPUT=8 WIDTH_MAN_OUTPUT=23 WIDTH_INT=16 WIDTH_DATA=32 DEVICE_FAMILY=STRATIXIII clock dataa result cbx_file=fixed2float.v</pre>
<p>At a resolution of 1024x768, the MegaWizard Plug-in Manager cannot display settings for the altremote_update, altpll, and altgx megafunctions.</p>	<p>Change your screen resolution to a lesser value.</p>
<p>When a RAM is inferred under all the following conditions, the synthesized circuit is not guaranteed to be correct:</p> <ul style="list-style-type: none"> <li>■ The read from and write to the memory occur in the same always block or process.</li> <li>■ The always block or process that reads/writes to the memory array is combinational.</li> <li>■ The write assignment happens before the read.</li> </ul> <p>The RAM is single-port.</p>	<p>To solve this problem, either disable RAM inference or rewrite the HDL description of the RAM. RAM inference can be disabled by setting the <b>ramstyle</b> attribute to "logic" or by setting the <b>auto_ram_recognition</b> variable to <b>Off</b>. Alternatively, a different HDL description can be used for the RAM (refer to the "Inferring Memory Functions from HDL Code" chapter in the <i>Quartus II Handbook</i>).</p>
<p>When you compile a project and then try to open the Assignment Editor, the Quartus II software displays an internal error if the selected devices in the <b>Migration Devices</b> dialog box include EP4SGX290KF40C3, EP4SGX360KF40C3, and EP4SGX530KH40C3.</p>	<p>In the <b>Device</b> page in the <b>Settings</b> dialog box, click <b>Migration Devices</b>. In the <b>Migration Devices</b> dialog box, click <b>OK</b> to close the dialog box. In the <b>Device</b> page, click <b>OK</b> to close the page.</p>
<p>In projects targeting Stratix IV GT and Arria GX devices, transceivers with altgx instances created in the Quartus II software version 9.0 SP1 might display an internal error in versions of the Quartus II software later than 9.0 SP1:</p> <pre>Internal Error: Sub-system: FHSSI, File: /quartus/fitter/fhssi/fhssi_cell_group.c pp, Line: 1463 aux_cell != NULL</pre>	<p>Regenerate the altgx instances.</p>

## Platform-Specific Issues

### Windows Platforms Only

Issue	Workaround
<p>If you attempt to install the Quartus II software version 9.1 to a disk drive that uses a FAT32 file system, installation fails and Windows generates an error similar to the following:</p> <pre>File Error The following error occurred on the file &lt;file name&gt;. The directory or file cannot be created (0x52)</pre>	<p>Refer to the solution available at <a href="http://www.altera.com/support/kdb/solutions/rd11122009_735.html">http://www.altera.com/support/kdb/solutions/rd11122009_735.html</a>.</p>
<p>For Windows Vista 64-bit, when you install the update for the Quartus II software version 9.0 SP1, the software requires you to terminate the jtagserver process before you update.</p>	<p>Reboot before installing the Quartus II software version 9.0 SP1, without opening the 9.0 software between rebooting and installing.</p>

### Linux Platforms Only

Issue	Workaround
<p>The Quartus II Web Edition software version 9.1 for Linux is a beta release. This beta version allows you to experience the software before it is officially released, but it may have limited-feature functionality.</p>	<p>For a complete listing of features available with the Quartus II Web Edition software version 9.1 for Linux, refer to the <a href="#">Quartus II Web Edition Software download site</a>.</p>
<p>The Toolbar dialog box does not close.</p>	<p>Close the Customize dialog box before attempting to close the Toolbar dialog box</p>
<p>The Quartus GUI cannot be resized.</p>	<p>Contact Altera Technical Support by creating a Service Request at <a href="http://www.altera.com/mysupport">http://www.altera.com/mysupport</a> and provide them the reference number <b>rd11102009_744</b>.</p>

## Device Family Issues

### Arria II GX

Issue	Workaround
<p>Compilation of a design targeting an Arria II GX device that uses LVDS without Dynamic Phase Alignment (DPA) and a data rate higher than 840Mbit/s generates a report panel entitled "Transmitter/Receiver Package Skew Compensation" to guide you to compensate for the skew on your board trace. In the "Estimated TCCS/Sampling Window Reduction" column (the last column of the report panel), the delay reduction reported may be inconsistent with the value reported in "Recommended Trace Delay Addition."</p>	<p>Use the Recommended Trace Delay Addition value to compensate for the skew and ignore the Estimated TCCS/Sampling Window Reduction values.</p>
<p>For designs that use Arria II GX transceivers, generation of HSPICE Simulation Deck files with the EDA Netlist Writer is not supported.</p>	<p>To generate HSPICE Simulation Deck files, create a revision of your design and remove the transceiver pins from the revision.</p>

## Cyclone IV GX

In the New Project wizard, selecting a (not installed) device generates an internal error in the Quartus II software.	Select an installed device.
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## Stratix II

Issue	Workaround
<p>If your design contains encrypted IP, exporting version-compatible database files or archiving HardCopy handoff files may result in an error similar to the following:</p> <p>Error: Can't generate HDBX file for the project because the encrypted source file cannot be located: "&lt;file name&gt;"</p> <p>Error: Can't generate ATMX file for the project because the encrypted source file cannot be located: "&lt;file name&gt;"</p>	Contact Altera Technical Support by creating a Service Request at <a href="http://www.altera.com/mysupport">http://www.altera.com/mysupport</a> and provide them the reference number <b>rd11092009_176</b> .

## Stratix II GX

Issue	Workaround
<p>In reconfigurable alt2gxb instances, the PLL logical number and PLL location number must match in order to work properly in hardware. If the logical number and location number do not match, the Quartus II software generates a message similar to the following:</p> <p>Error: Can't place GXB CMU PLL</p>	Ensure that the PLL logical number and PLL location number match.

## Stratix IV

Issue	Workaround
See Stratix IV GX	

## Stratix IV GX

Issue	Workaround
With the altgx megafunction, if your design uses dynamic protocol reconfiguration from x4 bonding in basic mode to XAUI or PCIE x4 protocols, simulation fails.	
The altgx_reconfig megafunction cannot support both TX data rate division and channel/PLL reconfiguration simultaneously.	

Issue	Workaround
<p>If you attempt to instantiate an altgx megafunction with the following settings:</p> <ul style="list-style-type: none"> <li>■ <b>Which protocol will you be using?</b> set to <b>Basic (PMA Direct)</b></li> <li>■ <b>Which subprotocol will you be using?</b> set to <b>XN</b></li> <li>■ <b>What is the number of channels?</b> set to a value greater than 4</li> <li>■ <b>Enable Channel and Transmitter PLL reconfiguration</b> set to <b>On</b></li> <li>■ <b>Use additional CMU/ATX Transmitter PLLs from outside the Transceiver block</b> set to <b>On</b></li> <li>■ you select a total of two PLLs, and</li> <li>■ you select PLL3 as the PLL logical reference index of the main PLL</li> </ul> <p>the Quartus II software generates an internal error.</p>	<p>Create the altgx instance with one channel, and duplicate the one-channel instance in your design to create multiple channels.</p>
<p>If you enable serial loopback between two PMA Direct mode altgx transceivers placed in different channels or quads, communication between the transceivers may fail.</p>	<p>Enable serial loopback only between input and output pins on the same channel or quad.</p>
<p>altgx x8 bonding (PCIe and Basic) with reconfiguration is not working appropriately in the Quartus II software version 9.1.</p>	
<p>altgx receivers in Basic (PMA Direct) mode may encounter a hardware hold failure in the transfer to core logic if default timing constraints are used, even after passing timing analysis with the preliminary timing model.</p>	<p>To ensure that the core registers latch the receiver's data with the same clock edge that the RX PMA launched the data with, add the following line to your SDC:</p> <pre>set_multicycle_path -setup -from [get_registers *alt4gxb* wire_receive_pma*_recoverdata out*] 0</pre>

## Stratix IV GT

Issue	Workaround
<p>During fitting, timing analysis, or power analysis, incorrect voltage settings of the VCC, VCCA, or VCCD power rails can generate the following error message:</p> <pre>Error: The supply voltage value &lt;voltage&gt; applied to the &lt;power supply&gt; power rail is illegal for the currently selected device.</pre>	<p>Select supply voltage values with the <b>Voltage</b> tab of the <b>Settings</b> dialog box.</p>

## HardCopy

Issue	Workaround
<p>For designs that target HardCopy IV devices, if <b>Target Device</b> is set to <b>Auto device selected by the Fitter</b> and, in the Quartus Settings File (.qsf) or with Tcl assignments, you have specified package or speed grade restrictions such that no valid HardCopy IV devices can be selected by the Fitter, the Quartus II software may generate an internal error during synthesis similar to the following:</p> <pre>Internal Error: Sub-system: SUTIL, File: /quartus/synth/sutil/sutil_device.cpp, Line: 1242 is_legal_device()</pre>	<p>Assign a device to your project with the <b>Device</b> page of the Settings dialog box.</p>
<p>For designs that target HardCopy III or HardCopy IV devices, if, on the <b>Dual-Purpose Pins</b> tab of the <b>Device and Pin Options</b> dialog box, <b>Data[7 .. 1]</b> is set to <b>As output driving ground</b>, compilation generates an internal error similar to the following:</p> <pre>Unknown power supply for configuration pins</pre>	<p>Do not set <b>Data[7 .. 1]</b> to <b>As output driving ground</b>.</p>
<p>In the altdq_dqs MegaWizard, if the RLDRAMII mode is set to x18 or x36 and both the Simulation Model and Generate netlist options are turned on, the following message is generated:</p> <pre>Failed to generate the synthesis netlist file</pre>	<p>Use the megafunction-generated variation file as input to third party synthesis tools.</p>
<p>During compilation of a design that targets a HardCopy IV device, the Quartus II software might generate errors similar to the following:</p> <pre>Critical Warning: Atom "*" atx_pll0" has data field INT_CHARGE_PUMP_CURRENT_BITS value 200 in revision "test_hciv" versus 144 in revision "test"  Critical Warning: Atom "*" atx_pll0" has data field INT_CHARGE_PUMP_CURRENT_BITS value 160 in revision "test_hciv" versus 144 in revision "test"  Critical Warning: Object "Inclk0 signal type" has property field "* altpll:altpll_component altpll_i4f2:au to_generated pll1 " as value "Global Clock" in revision "sbtb_stratix_bridge_top" versus "--" in revision "sbtb_stratix_bridge_top_hc"</pre>	<p>You may safely ignore these messages.</p>

## SOPC Builder Issues

Issue	Workaround
The Vectored Interrupt controller does not support VHDL simulation models.	
The output port reset value of a parallel input/output (PIO) module may be invalid if the <b>Enable individual bit set/clear output register</b> option is turned on for the output register and the multi-bit output port reset value is not zero.	On the <b>Basic Settings</b> page of the MegaWizard interface for the PIO core, turn off <b>Enable individual bit set/clear output register</b> .
<p>When adding components to your system, SOPC Builder might generate messages similar to the following:</p> <pre>Warning: set_module_property on deprecated property class_name, please use name instead  Warning: set_module_property on deprecated property preview_elaboration_callback, please use elaboration_callback instead  Warning: set_module_property on deprecated property preview_validation_callback, please use validation_callback instead</pre>	You may safely ignore these messages.
<p>In the System Console, if you set DC gain to 4, the <b>transceiver_reconfig_analog_get_rx_dcgain</b> and <b>transceiver_reconfig_analog_set_rx_dcgain</b> Tcl commands generate the following error:</p> <pre>Invalid DC Gain value</pre>	Select a DC gain value between 0 and 3.
In designs that target Arria II GX or Stratix IV devices, if you set <b>DC gain</b> to <b>2</b> with the altgx MegaWizard, the effective <b>DC gain</b> of the receiver is incorrectly set to <b>1</b> .	After you configure your altgx megafunction instance, use the altgx_reconfig megafunction to set the <b>DC gain</b> to <b>2</b> .
In the System Console, if you call <b>design_load</b> twice on the same project, you lose plugin services.	Call <b>design_load</b> only once per design, per System Console session. If you need to reload the design, start a new System Console.

## EDA Integration Issues

Issue	Workaround
<p>Attempting to simulate the uniphy megafunction's generic memory model in the sample design provided with the Cadence NC-sim software version 8.2 fails with an error similar to the following:</p> <pre>Queue uses an element data type that is not currently supported.</pre>	<p>Use a vendor or third-party generic memory model.</p>
<p>On Linux computers, attempting to run the Mentor Graphics ModelSim-Altera or Mentor Graphics ModelSim-Altera Starter Edition <b>vsim</b> command from the <code>&lt;path to ModelSim&gt;/bin</code> directory generates an error similar to the following:</p> <pre>Error: cannot find /apps/altera/quartusII/9.1.linux.cb/mod elsim_ase/bin/linux/vsim</pre>	<p>Run the <b>vsim</b> command from the <code>&lt;path to ModelSim&gt;/linuxoem</code> directory.</p>

## Memory Interface Issues

Issue	Workaround
<p>If a uniphy instance is generated in slave mode, the timing constraints are incorrect. In slave mode, the PLL is not instantiated inside the PHY, but is assumed to be external to the PHY.</p>	<p>Manually edit the following twofiles:</p> <ul style="list-style-type: none"> <li>■ <code>&lt;core&gt;/constraints/&lt;core&gt;_parameters.tcl</code>. In this file, PLL output ports are identified by their names. If the PLL is external to the PHY, replace the names of the PLL output ports with the names of the PLL ports you intend to use.</li> <li>■ <code>&lt;core&gt;/constraints/&lt;core&gt;.sdc</code>. In this file, PLL output ports are referenced by prepending the uniphy hierarchy. If the PLL is external to the PHY, remove “<code>{ inst }</code>” from each PLL port reference.</li> </ul>

Issue	Workaround
<p>In the RLDRAMII GUI of the uniphy megafunction, the tQKH parameter is defined as a “percentage of <i>half</i> of a clock period.” However, in the generated timing constraints, the tQKH parameter is used as a “percentage of a <i>full</i> clock period.” As a result, the read hold margin, as defined in the timing constraints, is too optimistic.</p>	<p>Manually edit the following two files:</p> <ul style="list-style-type: none"> <li>■ <code>&lt;core&gt;_report_timing.tcl</code></li> <li>■ <code>&lt;core&gt;.sdc</code></li> </ul> <p>to apply the tCKH corrective factor to the equations where tQKH is used.</p> <p>For example, change</p> <pre>[ expr \$tQKH * \$tCK ]</pre> <p>to</p> <pre>[ expr \$tQKH * \$tCK * 0.45 ]</pre> <p>where '0.45' is an example value of the tCKH parameter. (the tCKH parameter for your memory device can be obtained from the RLDRAMII datasheet).</p>
<p>During timing analysis, a warning regarding the PLL bandwidth setting may appear when there are cascading PLLs driving the altmemphy megafunction:</p> <pre>"Critical Warning: ALTMEMPHY PLL, &lt;PLL name&gt;, when fed by another PLL, must have bandwidth mode set to High instead of Auto"</pre>	<p>Set the bandwidth setting to <b>High</b> for the PLL using the altpll megafunction.</p>

## Simulation Model Changes

### altera\_mf Models

Model	Changes
altqpram	<ul style="list-style-type: none"> <li>■ This simulation model pertains to the APEX family only. Because the APEX family is not provided with the Quartus II software version 9.1, the altqpram model is no longer available.</li> </ul>
altcam	<ul style="list-style-type: none"> <li>■ This simulation model pertains to the APEX family only. Because the APEX family is not provided with the Quartus II software version 9.1, the altcam model is no longer available.</li> </ul>

Note: APEX, FLEX, and HardCopy Stratix device families are no longer supported by the Quartus II software version 9.1 simulation models.

## Latest Known Quartus II Software Issues

For more information about known software issues, look for information on the **Quartus II Software Support** page at the following URL:

<http://www.altera.com/support/software/sof-quartus.html>

You can find known issue information for previous versions of the Quartus II software on the Knowledge Database page at the following URL:

<http://www.altera.com/support/kdb/kdb-index.jsp>

## Software Issues Resolved

The following Customer Service Requests were fixed or otherwise resolved in this version of the Quartus II software:

Customer Service Request Numbers Resolved in this Release						
10115823	10175143	10251515	10470752	10495254	10517143	10525686
10526733	10531827	10535870	10538785	10544917	10584069	10585183
10588198	10589908	10595431	10602636	10612535	10612711	10614051
10614525	10614864	10618978	10619100	10620219	10620546	10626220
10633906	10634022	10634328	10634382	10635461	10639276	10640261
10640543	10641639	10641717	10642504	10643608	10643636	10644598
10645647	10646127	10646634	10646649	10651464	10652589	10652751
10653316	10653551	10654269	10654385	10654807	10654822	10655978
10656044	10656628	10656926	10657088	10657121	10658239	10659055
10659845	10660268	10660528	10661227	10661692	10661856	10662408
10662463	10662776	10663778	10664616	10665605	10666740	10667598
10667881	10667922	10668661	10668981	10669110	10669198	10669318
10669468	10669591	10670099	10670339	10670392	10670933	10671265
10671666	10671959	10672357	10672835	10673076	10673620	10673992
10674241	10674273	10674344	10674506	10674794	10674897	10675598
10675728	10676281	10676912	10677394	10677584	10677947	10678098
10678293	10678304	10678327	10678545	10678757	10679010	10679142
10679203	10679243	10679266	10679348	10679651	10679664	10679676
10679733	10679762	10679777	10679940	10680257	10680622	10680883
10680890	10680947	10680983	10681172	10681188	10681349	10681396
10681414	10681424	10681529	10681621	10681824	10682595	10682639
10683347	10683456	10683560	10683859	10683910	10683932	10684013
10684127	10684210	10684370	10684502	10684704	10684745	10684802
10684831	10684896	10685063	10685298	10685349	10685480	10685540
10685596	10685649	10685722	10685726	10685834	10685860	10686026
10686076	10686218	10686357	10686406	10686426	10686769	10686797
10686815	10687386	10687430	10687544	10687691	10687753	10687770
10687798	10687847	10687880	10688026	10688206	10688219	10688442
10688473	10688478	10688499	10688613	10688680	10688728	10688731
10689011	10689192	10689301	10689334	10689421	10689452	10689546
10689643	10689723	10689904	10690032	10690049	10690097	10690163
10690353	10690368	10690458	10690488	10690543	10690568	10690596
10690641	10690804	10690921	10691058	10691138	10691159	10691454
10691526	10691650	10691720	10691764	10692139	10692194	10692304
10692377	10692494	10692729	10692757	10692779	10692865	10693083
10693164	10693218	10693249	10693451	10693598	10693625	10693684
10693891	10694020	10694022	10694050	10694115	10694202	10694206

<b>Customer Service Request Numbers Resolved in this Release</b>						
10694208	10694262	10694263	10694282	10694479	10694633	10694718
10694885	10695053	10695062	10695069	10695077	10695097	10695141
10695174	10695359	10695580	10695587	10695591	10695744	10695762
10695850	10696023	10696140	10696144	10696197	10696246	10696419
10696753	10696845	10696939	10696947	10697055	10697857	10697969
10698048	10698203	10698204	10698260	10698350	10698373	10698476
10698480	10698516	10698527	10698562	10698616	10698785	10698840
10698848	10698865	10698927	10698936	10698947	10698976	10698986
10699075	10699285	10699299	10699527	10699544	10699574	10699603
10700015	10700027	10700055	10700127	10700133	10700162	10700187
10700338	10700345	10700485	10700581	10700650	10700842	10701000
10701002	10701008	10701049	10701083	10701132	10701196	10701289
10701301	10701419	10701660	10702011	10702048	10702205	10702342
10702357	10702367	10702378	10702421	10702432	10702435	10702463
10702506	10702607	10702608	10702619	10702621	10702726	10702871
10702898	10703015	10703029	10703091	10703117	10703132	10703136
10703359	10703545	10703632	10703779	10703836	10703840	10703873
10704078	10704092	10704188	10704249	10704277	10704324	10704395
10704481	10704527	10704539	10704560	10704701	10704774	10704822
10704827	10705013	10705051	10705052	10705153	10705201	10705369
10705402	10705522	10705533	10705594	10705598	10705662	10705834
10705847	10705899	10706001	10706033	10706036	10706062	10706156
10706191	10706274	10706309	10706384	10706388	10706422	10706603
10706788	10706834	10706839	10706843	10706995	10707005	10707032
10707076	10707147	10707214	10707291	10707320	10707388	10707478
10707483	10707634	10707677	10707693	10707742	10707762	10707777
10707793	10707795	10707799	10707840	10707861	10707911	10708115
10708117	10708134	10708268	10708311	10708359	10708454	10708491
10708503	10708530	10708791	10708839	10708881	10708894	10708904
10708996	10709068	10709257	10709368	10709396	10709409	10709412
10709579	10709614	10709687	10709699	10709707	10709843	10709880
10709884	10709919	10710073	10710080	10710097	10710153	10710243
10710251	10710270	10710283	10710324	10710393	10710491	10710518
10710661	10710720	10710731	10710757	10710950	10710965	10711011
10711023	10711036	10711088	10711095	10711232	10711298	10711353
10711374	10711435	10711484	10711487	10711518	10711519	10711666
10711737	10712014	10712113	10712357	10712427	10712432	10712437
10712459	10712481	10712512	10712536	10712543	10712605	10712612
10712617	10712664	10712824	10712968	10713061	10713087	10713092
10713139	10713156	10713158	10713177	10713186	10713201	10713430

<b>Customer Service Request Numbers Resolved in this Release</b>						
10713468	10713524	10713613	10713614	10713735	10713750	10713798
10713839	10713850	10713906	10714027	10714035	10714039	10714044
10714144	10714268	10714282	10714320	10714393	10714400	10714509
10714511	10714594	10714613	10714669	10714676	10714721	10714727
10714850	10714857	10714882	10714947	10715008	10715027	10715090
10715163	10715174	10715175	10715176	10715178	10715186	10715192
10715198	10715245	10715399	10715405	10715419	10715490	10715502
10715554	10715619	10715716	10715866	10715867	10715997	10716009
10716096	10716119	10716121	10716124	10716127	10716198	10716281
10716323	10716330	10716374	10716383	10716490	10716630	10716649
10716663	10716695	10716704	10716851	10716880	10716909	10716941
10716992	10717034	10717107	10717242	10717428	10717479	10717625
10717693	10717695	10717760	10717879	10717936	10717953	10718026
10718082	10718100	10718129	10718160	10718214	10718316	10718342
10718410	10718415	10718434	10718571	10718787	10718880	10718907
10718960	10719087	10719131	10719358	10719371	10719391	10719578
10719587	10719634	10719702	10719770	10719800	10719818	10719851
10720007	10720009	10720061	10720090	10720149	10720170	10720332
10720514	10720755	10720800	10720841	10720847	10720963	10720995
10721018	10721039	10721123	10721245	10721264	10721286	10721314
10721539	10721566	10721568	10721594	10721636	10721689	10721748
10722000	10722024	10722033	10722043	10722250	10722315	10722408
10722431	10722438	10722457	10722665	10722813	10722978	10722987
10722998	10723044	10723108	10723243	10723277	10723360	10723402
10723558	10723573	10723591	10723595	10723631	10723720	10723740
10723841	10723860	10724027	10724133	10724172	10724179	10724181
10724212	10724329	10724334	10724395	10724411	10724437	10724441
10724528	10724547	10724647	10724950	10724991	10725128	10725236
10725449	10725460	10725547	10725678	10725726	10725858	10725918
10726253	10726366	10726369	10726433	10726456	10726595	10726606
10727098	10727182	10727240	10727241	10727245	10727599	10727875
10727959	10728235	10728394	10729151			

## Revision History

<b>Revision</b>	<b>Description</b>
1.0	Initial Release



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