



These release notes for the Altera® RapidIO MegaCore® function version 7.1 contain the following information:

- [New Features & Enhancements](#)
- [Errata Fixed in This Release](#)
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For system requirements and installation instructions, refer to *Quartus II Installation & Licensing for Windows* or *Quartus II Installation & Licensing for UNIX & Linux Workstations* on the Altera website.

New Features & Enhancements

The following new feature is included in this release:

- Added support for Arria™ GX device family
- Added SOPC Builder interface
- Avalon™-ST conversion of the pass-through port
- Improved error detection and recovery

Errata Fixed in This Release

The following errata were fixed in this release:

- Incorrect I/O Logical Layer Avalon-MM Slave Write Request Packets
- The Value Written to a Physical Layer Register Can Be Overwritten
- An Empty Demo Testbench Is Generated for Variations with an Atlantic Pass-Through Port But No Logical Layer Module
- Incorrect Revision ID Label in RapidIO MegaWizard
- RapidIO MegaWizard Interface Options for the Stratix II GX Transceiver Have No Effect

For existing up-to-date errata, refer to the *RapidIO MegaCore Function v7.1 Errata Sheet* on the Altera website.

Contact Altera

Although every effort has been made to ensure that this version of the RapidIO MegaCore Function works correctly, if problems occur, use the following contact information to communicate issues to the appropriate Altera representative.

For technical support or other information about Altera products, go to the Altera website at www.altera.com. You can also contact Altera through your local sales representative or any of the sources listed in [Table 1](#).

Information Type	Contact (1)
Technical support	www.altera.com/mysupport/
Technical training	www.altera.com/training/
Technical training services	custrain@altera.com
Product literature	www.altera.com/literature
Product literature services	literature@altera.com
FTP site	ftp.altera.com

Note:

(1) You can also contact your local Altera sales office or sales representative.

Revision History [Table 2](#) shows the revision history for the RapidIO MegaCore Function.

Version	Date	Revision
7.1	May 2007	<ul style="list-style-type: none"> ● Preliminary support for Arria™ GX devices ● Added SOPC Builder interface ● Avalon-ST conversion of the Pass-Through port ● Improved error detection and recovery
7.0	December 2006	<ul style="list-style-type: none"> ● Support for Cyclone III devices
6.1	December 2006	<ul style="list-style-type: none"> ● Support for Doorbell Message packets ● Support for Stratix® III devices ● For a list of errata fixed in this release, refer to the section "Errata Fixed in This Release" on page 1
3.1.1	August 2006	<p>Errata fixed in this release:</p> <ul style="list-style-type: none"> ● Timeout and Interrupt Occur When Transport Layer Processes an Odd Number of Consecutive 64-bit Packets ● Input-Output Avalon Master Returns Incorrect Read Data ● Invalid Read Data From RXSYM Register if RXCTRL Register Bit Zero Not Set ● Read Response Can Be Lost ● Control Symbol Transmit Queue Not Cleared Properly When MegaCore Function Is Reset

Table 2. RapidIO MegaCore Function Revision History (Part 2 of 2)

Version	Date	Revision
3.1.0	April 2006	Errata fixed in this release: <ul style="list-style-type: none"> ● SWRITE request packets are not supported ● NWRITE_R request packets are not supported ● The MegaCore function fails to signal maintenance read request errors ● The RapidIO I/O write short packet is formatted improperly ● Word ordering is incorrect inside RapidIO packets ● An incorrect CRC is generated for short serial RapidIO packets of six bytes ● IP Toolbench fails when generating a MegaCore function variation if the I/O Logical Layer or I/O Maintenance Logical Layer is enabled but the transport layer is not
3.0.1	January 2006	<ul style="list-style-type: none"> ● Improved support for the Transport and Logical layers ● Improved read (NREAD) and write (NWRITE) request processing
3.0.0	October 2005	<ul style="list-style-type: none"> ● Transport and Logical layers, with an Avalon® interface ● Optional XGMII interface for serial physical layer implementation in Cyclone® II, Stratix II, or HardCopy® II devices with an external transceiver
2.2.2	April 2005	Maintenance release.



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