

MAX CPLD Series Package & I/O Matrix



- Device available in commercial temperature. Contact Altera for industrial temperature.
- Device available in commercial and industrial temperatures.
- Device available in commercial and industrial, and qualified to extended temperatures.
- 36 Number indicates available user I/O pins.
- Vertical migration (Same V_{CC}, GND, ISP, and input pins).

		MAX [®] II CPLDs 3.3V, 2.5V, 1.8V				MAX 3000A CPLDs 3.3V					MAX 7000B CPLDs 2.5V					MAX 7000AE CPLDs 3.3V					MAX 7000S CPLDs 5.0V						
		EPM240/G/Z	EPM570/G/Z	EPM1270/G	EPM2210/G	EPN3032A	EPN3064A	EPN3128A	EPN3256A	EPN3512A	EPN7032B	EPN7064B	EPN7128B	EPN7256B	EPN7512B	EPN7032AE	EPN7064AE	EPN7128AE	EPN7256AE	EPN7512AE	EPN7032S	EPN7064S	EPN7128S	EPN7160S	EPN7192S	EPN7256S	
Density & Speed	Macrocells ¹	192	440	980	1,700	32	64	128	256	512	32	64	128	256	512	32	64	128	256	512	32	64	128	160	256	512	
	Logic Elements (LEs)	240	570	1,270	2,210	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	
	Pin-to-Pin Delay (ns) ²	4.7 4.7 7.5	5.4 5.4 9.0	6.2 6.2	7.0 7.0	4.5	4.5	5.0	7.5	7.5	3.5	3.5	4.0	5.0	5.5	4.5	4.5	5.0	5.5	7.5	5.0	5.0	6.0	6.0	7.5	7.5	
PLCC (L) ³	44-Pin					34	34				36					36	36				36	36					
	84-Pin																	68				68	68	64			
TQFP (T) ⁴	44-Pin					34	34				36	36				36	36				36	36					
	100-Pin	80	76				66	80				68	84	84			68	84	84			68	84	84			
	144-Pin		116	116				96	116				100	120	120			100	120	120							
PQFP (Q or R) ⁵	100-Pin																										
	160-Pin																							84			
	208-Pin								158	172				164	176				164	176						164	
BGA (B) ⁶	256-Pin													212					212								
FBGA (F) ⁷	100-Pin	80	76									68	84				68	84	84								
	256-Pin		160	212	204			98	161	208			100	164	212			100	164	212							
	324-Pin				272																						
UBGA (U) ⁸	49-Pin										36	41															
	169-Pin													141	141												
MBGA (M) ^{9, 10}	68-Pin	54																									
	100-Pin	80	76																								
	144-Pin		116																								
	256-Pin		160	212																							

- 1 Typical equivalent macrocells for MAX II devices
- 2 MAX IIZ data is preliminary
- 3 Plastic J-lead chip carrier
- 4 Thin quad flat pack
- 5 Plastic quad flat pack
- 6 Ball-grid array (1.27 mm)
- 7 FineLine BGA (1.0 mm)
- 8 Ultra FineLine BGA (0.8 mm)
- 9 Micro FineLine BGA (0.5 mm)
- 10 MAX IIZ devices are available only in commercial temperatures

Package Statistics	PLCC		TQFP			PQFP			BGA	FBGA			UBGA		MBGA			
Number of Pins	44	84	44	100	144	100	160	208	256	100	256	324	49	169	68	100	144	256
Nominal Length x Width (mm)	18 x 18	30 x 30	12 x 12	16 x 16	22 x 22	17 x 23	31 x 31	31 x 31	27 x 27	11 x 11	17 x 17	19 x 19	7 x 7	11 x 11	5 x 5	6 x 6	7 x 7	11 x 11
Maximum Surface Area (mm) ¹	312	921	149	262	493	399	986	952	740	125	296	369	52	125	27	38	52	125
Maximum Height (mm)	4.57	4.57	1.2	1.2	1.6	3.4	4.1	4.1	2.7	1.7	3.50 ¹	3.50 ¹	1.55	2.2	1.2	1.2	1.2	1.2
Nominal Lead Pitch (mm)	1.27	1.27	0.8	0.5	0.5	0.65	0.65	0.5	1.27	1	1	1	0.8	0.8	0.5	0.5	0.5	0.5
Maximum Lead Width (mm)	0.53	0.53	0.45	0.27	0.27	0.4	0.4	0.27	0.9	0.7	0.7	0.7	0.6	0.6	0.35	0.35	0.35	0.35

¹ Altera's maximum height specification is 2.6 mm. The 3.5 maximum height specification shown reflects the JEDEC specifications.

MAX CPLD Series Features



	MAX II CPLDs 3.3V, 2.5V, 1.8V				MAX 3000A CPLDs 3.3V					MAX 7000B CPLDs 2.5V					MAX 7000AE CPLDs 3.3V					MAX 7000S CPLDs 5.0V										
	EPM240/G/Z	EPM570/G/Z	EPM1270/G	EPM2210/G	EPM3032A	EPM3064A	EPM3128A	EPM3256A	EPM3512A	EPM3032B	EPM7064B	EPM7128B	EPM7256B	EPM7512B	EPM7032AE	EPM7064AE	EPM7128AE	EPM7256AE	EPM7512AE	EPM7032S	EPM7064S	EPM7128S	EPM7160S	EPM7192S	EPM7256S					
Features	User Flash Memory (Kbit)				8					-					-					-										
	Boundary Scan JTAG				✓					✓					✓					-										
	JTAG ISP				✓					✓					✓					✓										
	Fast Input Registers				✓					-					✓					✓										
	Programmable Register Power-Up				✓					-					✓					-										
	Programmable Ground Pins				✓					-					✓					-										
	Open-Drain Outputs				✓					✓					✓					✓										
	Programmable Pull-Up Resistors				✓					-					-					-										
	Bus Hold				✓					-					-					-										
	JTAG Translator				✓					-					-					-										
	Real-Time ISP				✓					-					-					-										
	0.5-mm BGA Packages ¹				✓					-					-					-										
Core Voltage & I/O Options	Core Voltage (V)				1.8					3.3					2.5					3.3					5.0					
	MultiVolt Core (V)				3.3, 2.5, 1.8 ²					-					-					-					-					
	MultiVolt I/O (V)				3.3, 2.5, 1.8, 1.5					5.0, 3.3, 2.5					3.3, 2.5, 1.8					5.0, 3.3, 2.5					-					
	I/O Power Banks				2 2 4 4					1					2					1					1					
	Maximum I/O Pins				80 160 212 272					34 66 98 161 208					36 68 100 164 212					36 68 100 164 212					36 68 100 104 124 164					
	Maximum Output Enables				80 160 212 272					6 6 6 6 10					6 6 6 6 10					6 6 6 6 10					6					
	Transistor-to-Transistor Logic (TTL) (5.0-V Tolerance)				-					-					-					✓					✓					
	LVTTTL/LVCMOS				-					-					-					-					-					
	32-Bit, 66-MHz PCI Compliant				-					-					-					-					-					
	GTL+ / SSTL-2, SSTL-3, All Class I & Class II				-					-					-					-					-					
	Schmitt Triggers				-					-					-					-					-					
	Programmable Slew Rate				-					-					-					-					-					
	Programmable Drive Strength				-					-					-					-					-					

¹ Package not available for EPM2210/G device

² MAX IIG and MAX IIZ devices require 1.8V core voltage supply

³ An external series resistor must be used for 5.0V tolerance