Version 14.0

ALTERA PRODUCT CATALOG

ALTERA®

MEASURABLE ADVANTAGE™

CONTENTS

Altera Solutions Portfolio

Altera delivers the broadest portfolio of programmable logic devices—FPGAs, SoCs, and CPLDs in combination with software tools, intellectual property (IP), embedded processors, customer support, and technical training. Altera's product leadership, excellent value, and superior quality of service give you a measurable advantage. Bring your great ideas to life faster, better, and more cost effectively.

FPGAs

Altera FPGAs give you the flexibility to innovate, differentiate, and stay ahead in the market. We have three classes of FPGAs to meet your market needs, from the industry's highest density and performance to the most cost effective.

High-End FPGAs

- Highest bandwidth, highest density FPGAs
- Integrated transceiver variants
- Design entire systems on a chip

Midrange FPGAs

- Balanced cost, power, and performance FPGAs
- Integrated transceiver and processor variants
- Comprehensive design protection

Lowest Cost and Power FPGAs

- Lowest system cost and power FPGAs
- Integrated transceiver and processor variants
- Fastest time to market

SoCs

SoCs consolidate two discrete devices into one, reducing system power, cost, and board size while increasing performance. SoCs integrate an ARM-based hard processor system (HPS) consisting of a dual-core ARM® processor, peripherals, and memory controllers with the FPGA fabric using a high-bandwidth interconnect backbone.

Power

Power your FPGA with Enpirion power management products. Our integrated products provide an industry-leading combination of small footprint, low noise performance, and high efficiency to complete your design faster.

Non-Volatile FPGA

For customers seeking a cost-effective, low-power, single-chip solution for control plane or datapath applications, MAX 10 FPGAs provide a highly integrated system solution.

CPLDs

For glue logic and any control functions, our non-volatile MAX series offers the market's lowest cost CPLDs—a single-chip solution, great for interface bridging, level shifting, I/O expansion, and management of analog I/Os.

Productivity-Enhancing Design Software, Embedded Processing, IP, Development Kits, and Training

With Altera, you get a complete design environment and a wide choice of design tools—all built to work together easily so your designs are up and running fast. You can try one of our training classes to get a jump-start on your designs. Choose Altera and see how we enhance your productivity and make a difference to your bottom line.

Arria 10 GX FPGA Features

www.altera.com/selector

The following features, packages, and I/O matrices give you an overview of our devices. To get more details about these devices or other older devices that are available, check out our online selector guide at www.altera.com/selector.

Arria® 10 GX FPGAs: Up to 96 full-duplex transceivers with data rates up to 17.4 Gbps, 16 Gbps backplane, and up to 1,150K equivalent logic elements (LEs).

		Maximum Resource Count for Arria 10 GX FPGAs[1]								
		10AX016	10AX022	10AX027	10AX032	10AX048	10AX057	10AX066	10AX090	10AX115
Resources	Adaptive logic modules (ALMs)	61,510	83,730	101,620	118,730	181,790	217,080	250,540	339,620	427,200
	LEs (K)	160	220	270	320	480	570	660	900	1,150
	Registers	246,040	334,920	406,480	474,920	727,160	868,320	1,002,160	1,358,480	1,708,800
	M20K memory blocks	440	588	750	891	1,438	1,800	2,133	2,423	2,713
	M20K memory (Mb)	9	11	15	17	28	35	42	47	53
	MLAB memory (Mb)	1	1.8	2.4	2.8	4.3	5.0	5.7	9.2	12.7
	Variable-precision digital signal processing (DSP) blocks	156	192	800	985	1,368	1,612	1,855	1,518	1,518
	18 x 19 multipliers	312	382	1,660	1,970	2,736	3,046	3,356	3,036	3,036
Architectural Features	Global clock networks	32								
	Regional clock networks	8	8	8	8	8	8	16	16	16
	Design security	Bitstream encryption with authentication								
I/O Features	I/O voltage levels supported (V)	1.2, 1.25, 1.35, 1.8, 2.5, 3.0[2]								
	I/O standards supported	**3 V I/Os Only:** 3 V LVTTL, 2.5 V CMOS **DDR and LVDS I/Os:** POD12, POD10, Differential POD12, Differential POD10, LVDS, RSDS, mini-LVDS, LVPECL **All I/Os:** 1.8 V CMOS, 1.5 V CMOS, 1.2 V CMOS, SSTL-18 (I and II), SSTL-15 (I and II), SSTL-135, SSTL-125, SSTL-12, HSTL-18 (I and II), HSTL-15 (I and II), HSTL-12 (I and II), HSUL-12, Differential SSTL-18 (I and II), Differential SSTL-15 (I and II), Differential SSTL-135, Differential SSTL-125, Differential SSTL-12, Differential HSTL-18 (I and II), Differential HSTL-15 (I and II), Differential HSTL-12 (I and II), Differential HSUL-12								
	LVDS channels, 1.6 Gbps (receive/transmit)	120	120	168	168	222	324	324	384	384
	Embedded dynamic phase alignment (DPA) circuitry	✓								
	On-chip termination (OCT)	Series, parallel, and differential								
	Transceiver count	12	12	24	24	36	48	48	96	96
	PCI Express® (PCIe®) hard IP blocks (Gen3)	1	1	2	2	2	2	2	4	4
	Memory devices supported	DDR4, DDR3, DDR2, QDR IV, QDR II+, QDR II+ Xtreme, LPDDR3, LPDDR2, RLDRAM 3, RLDRAM II, LLDRAM II, HMC								

[1] All data is correct at the time of printing, and may be subject to change without prior notice. For the latest information, please visit **www.altera.com**.

[2] 3.0 V compliant, requires a 3 V power supply.

Arria 10 GT FPGA Features

Arria 10 GT FPGAs: Up to 96 full-duplex optimized transceivers with data rates up to 28.1 Gbps, and up to 1,150K equivalent LEs.

		Maximum Resource Count for Arria 10 GT FPGAs[1]	
		10AT090	**10AT115**
Resources	ALMs	339,620	427,200
	LEs (K)	900	1,150
	Registers	1,358,480	1,708,800
	M20K memory blocks	2,423	2,713
	M20K memory (Mb)	47	53
	MLAB memory (Mb)	9.2	12.7
	Variable-precision DSP blocks	1,518	1,518
	18 x 19 multipliers	3,036	3,036
Architectural Features	Global clock networks	32	
	Regional clock networks	16	16
	Design security	Bitstream encryption with authentication	
I/O Features	I/O voltage levels supported (V)	1.2, 1.25, 1.35, 1.8, 2.5, 3.0[2]	
	I/O standards supported	**3 V I/Os Only:** 3 V LVTTL, 2.5 V CMOS **DDR and LVDS I/Os:** POD12, POD10, Differential POD12, Differential POD10, LVDS, RSDS, mini-LVDS, LVPECL **All I/Os:** 1.8 V CMOS, 1.5 V CMOS, 1.2 V CMOS, SSTL-18 (I and II), SSTL-15 (I and II), SSTL-135, SSTL-125, SSTL-12, HSTL-18 (I and II), HSTL-15 (I and II), HSTL-12 (I and II), HSUL-12, Differential SSTL-18 (I and II), Differential SSTL-15 (I and II), Differential SSTL-135, Differential SSTL-125, Differential SSTL-12, Differential HSTL-18 (I and II), Differential HSTL-15 (I and II), Differential HSTL-12 (I and II), Differential HSUL-12	
	LVDS channels, 1.6 Gbps (receive/transmit)	312	312
	Embedded DPA circuitry	✓	
	OCT	Series, parallel, and differential	
	Transceiver count	96	96
	PCIe hard IP blocks (Gen3)	4	4
	Memory devices supported	DDR4, DDR3, DDR2, QDR IV, QDR II+, QDR II+ Xtreme, LPDDR3, LPDDR2, RLDRAM 3, RLDRAM II, LLDRAM II, HMC	

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[2] 3.0 V compliant, requires a 3 V power supply.

Arria 10 SX SoC Features

The 20 nm Arria 10 SoCs deliver all the features and benefits of Arria 10 FPGAs plus a second-generation hard processor system with 87 percent higher processor performance (1.5 GHz dual-core ARM Cortex®-A9 MPCore™ processor) and enhancements, such as Secure Boot, three Ethernet Media Access Controller (EMAC) hard IP cores, and 64 bit DDR4 SDRAM support—all while maintaining full software compatibility with 28 nm SoCs.

		Maximum Resource Count for Arria 10 SX SoC[1]						
		10AS016	**10AS022**	**10AS027**	**10AS032**	**10AS048**	**10AS057**	**10AS066**
Resources	ALMs	61,510	83,730	101,620	118,730	181,790	217,080	250,540
	LEs (K)	160	220	270	320	480	570	660
	Registers	246,040	334,920	406,480	474,920	727,160	868,320	1,002,160
	M20K memory blocks	440	588	750	891	1,438	1,800	2,133
	M20K memory (Mb)	9	11	15	17	28	35	42
	MLAB memory (Mb)	1	1.8	2.4	2.8	4.3	5.0	5.7
	DSP blocks	156	192	800	985	1,368	1,612	1,855
	18 x 19 multipliers	312	382	1,660	1,970	2,736	3,046	3,356
Architectural Features	Global clock networks	32						
	Regional clock networks	8	8	8	8	8	8	16
I/O Features	I/O voltage levels supported (V)	1.2, 1.25, 1.35, 1.8, 2.5, 3.0[2]						
	I/O standards supported	**3 V I/Os Only:** 3 V LVTTL, 2.5 V CMOS **DDR and LVDS I/Os:** POD12, POD10, Differential POD12, Differential POD10, LVDS, RSDS, mini-LVDS, LVPECL **All I/Os:** 1.8 V CMOS, 1.5 V CMOS, 1.2 V CMOS, SSTL-18 (I and II), SSTL-15 (I and II), SSTL-135, SSTL-125, SSTL-12, HSTL-18 (I and II), HSTL-15 (I and II), HSTL-12 (I and II), HSUL-12, Differential SSTL-18 (I and II), Differential SSTL-15 (I and II), Differential SSTL-135, Differential SSTL-125, Differential SSTL-12, Differential HSTL-18 (I and II), Differential HSTL-15 (I and II), Differential HSTL-12 (I and II), Differential HSUL-12						
	LVDS channels, 1.6 Gbps (receive/transmit)	120	120	168	168	222	270	270
	Embedded DPA circuitry	✓						
	OCT	Series, parallel, and differential						
	Transceiver count	12	12	24	24	36	48	48
	PCIe hard IP blocks (Gen3)	1	1	2	2	2	2	2
	Memory devices supported	DDR4, DDR3, DDR2, QDR IV, QDR II+, QDR II+ Xtreme, LPDDR3, LPDDR2, RLDRAM 3, RLDRAM II, LLDRAM II, HMC						

[1] All data is correct at the time of printing, and may be subject to change without prior notice. For the latest information, please visit **www.altera.com**.

[2] 3.0 V compliant, requires a 3 V power supply.

Arria 10 SX SoC Features

		Maximum Resource Count for Arria 10 SX SoC[1]						
		10AS016	10AS022	10AS027	10AS032	10AS048	10AS057	10AS066
Hard Processor System	Central processing unit (CPU) core	Dual-core ARM Cortex-A9 MPCore processor						
	CPU cache and Co-processors	L1 instruction cache (32 KB) L1 data cache (32 KB) Layer 2 cache (512 KB) shared Floating-point unit (FPU) single and double precision ARM Neon™ media engine ARM CoreSight™ debug and trace technology Snoop control unit (SCU) Acceleration coherency port (ACP)						
	Scratch pad RAM	256 KB						
	HPS DDR memory	DDR4, DDR3, and LP DDR3 (Up to 64 bit with ECC)						
	Direct Memory Access (DMA) controller	8 channel						
	EMAC	3 x 10/100/1000 EMAC with integrated DMA						
	USB On-The-Go controller (OTG)	2 x USB OTG with integrated DMA						
	UART controller	2 x UART 16550 compatible						
	Serial Peripheral Interface (SPI) controller	4 x SPI						
	I^2C controller	5 x I^2C						
	Quad SPI flash controller	1 x SIO, DIO, QIO SPI flash supported						
	SD/SDIO/MMC controller	1 x eMMC 4.5 with DMA and CE-ATA support						
	NAND flash controller	1 x ONFI 1.0 or later 8 and 16 bit support						
	General-purpose timers	7X						
	Software-programmable general-purpose I/Os (GPIOs)	Maximum 54 GPIOs						
	Direct shared I/Os	48 I/O to connect HPS peripherals directly to I/O						
	Watchdog timers	4X						
	Security	Secure Boot, Advanced Encryption Standard (AES), and Secure Hash Algorithm						

[1] All data is correct at the time of printing, and may be subject to change without prior notice. For the latest information, please visit **www.altera.com**.

Arria 10 FPGA Series Package and I/O Matrices

	Arria 10 GX/GT FPGAs[1]					
	UBGA (U)	FBGA (F)				
	484 pin (U19) 19 x 19 (mm) 0.8-mm pitch	672 pin (F27) 27 x 27 (mm) 1.0-mm pitch	780 pin (F29) 29 x 29 (mm) 1.0-mm pitch	1,152 pin (F34) 35 x 35 (mm) 1.0-mm pitch	1,152 pin (F35) 35 x 35 (mm) 1.0-mm pitch	1,152 pin (F36) 35 x 35 (mm) 1.0-mm pitch
10AX016	192, 48, 72, 6	240, 48, 96, 12	288, 48, 120, 12			
10AX022	192, 48, 72, 6	240, 48, 96, 12	288, 48, 120, 12			
10AX027		240, 48, 96, 12	360, 48, 156, 12	384, 48, 168, 24	384, 48, 168, 24	
10AX032		240, 48, 96, 12	360, 48, 156, 12	384, 48, 168, 24	384, 48, 168, 24	
10AX048			360, 48, 156, 12	492, 48, 222, 24	396, 48, 174, 36	
10AX057				492, 48, 222, 24	396, 48, 174, 36	432, 48, 192, 36
10AX066				492, 48, 222, 24	396, 48, 174, 36	432, 48, 192, 36
10AX090				504, 0, 252, 24		432, 0, 216, 36
10AX115				504, 0, 252, 24		432, 0, 216, 36

	Arria 10 GX/GT FPGAs[1]					
	FBGA (F)					
	1,517 pin (F40) 40 x 40 (mm) 1.0-mm pitch	1,517 pin (F40) 40 x 40 (mm) 1.0-mm pitch	1,517 pin (F40) 40 x 40 (mm) 1.0-mm pitch	1,932 pin (F45) 45 x 45 (mm) 1.0-mm pitch	1,932 pin (F45) 45 x 45 (mm) 1.0-mm pitch	1,932 pin (F45) 45 x 45 (mm) 1.0-mm pitch
10AX027						
10AX032						
10AX048						
10AX057	696, 96, 324, 36	588, 48, 270, 48				
10AX066	696, 96, 324, 36	588, 48, 270, 48				
10AX090		600, 0, 300, 48	342, 0, 154, 66	768, 0, 384, 48	624, 0, 312, 72	480, 0, 240, 96
10AX115		600, 0, 300, 48	342, 0, 154, 66	768, 0, 384, 48	624, 0, 312, 72	480, 0, 240, 96
10AT090		600, 0, 300, 48			624, 0, 312, 72	480, 0, 240, 96
10AT115		600, 0, 300, 48			624, 0, 312, 72	480, 0, 240, 96

	Arria 10 SX SoCs[1]						
	UBGA (U)	FBGA (F)					
	484 pin (U19) 19 x 19 (mm) 0.8-mm pitch	672 pin (F27) 27 x 27 (mm) 1.0-mm pitch	780 pin (F29) 29 x 29 (mm) 1.0-mm pitch	1,152 pin (F34) 35 x 35 (mm) 1.0-mm pitch	1,152 pin (F35) 35 x 35 (mm) 1.0-mm pitch	1,517 pin (F40) 40 x 40 (mm) 1.0-mm pitch	1,517 pin (F40) 40 x 40 (mm) 1.0-mm pitch
10AS016	192, 48, 72, 6	240, 48, 96, 12	288, 48, 120, 12				
10AS022	192, 48, 72, 6	240, 48, 96, 12	288, 48, 120, 12				
10AS027		240, 48, 96, 12	360, 48, 156, 12	384, 48, 168, 24	384, 48, 168, 24		
10AS032		240, 48, 96, 12	360, 48, 156, 12	384, 48, 168, 24	384, 48, 168, 24		
10AS048			360, 48, 156, 12	492, 48, 222, 24	396, 48, 174, 36		
10AS057				492, 48, 222, 24	396, 48, 174, 36	696, 96, 324, 36	588, 48, 270, 48
10AS066				492, 48, 222, 24	396, 48, 174, 36	696, 96, 324, 36	588, 48, 270, 48

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624, 48, 192, 48 Numbers indicate GPIO count, 3.0 V I/O count, LVDS count, and transceiver count.

Vertical migration (same Vcc, Gnd, ISP, and input pins). User I/Os may be less than labeled for vertical migration.

Arria 10 series devices are offered in extended and industrial temperatures, and RoHS-compliant packages.

Stratix V GT FPGA Features

		Maximum Resource Count for Stratix V GT FPGAs (0.85 V)[1]	
		5SGTC5	5SGTC7
Resources	ALMs	160,400	234,720
	LEs (K)	425	622
	Registers	641,600	938,880
	M20K memory blocks	2,304	2,560
	M20K memory (Mb)	45	50
	MLAB memory (Mb)	4.9	7.16
	Variable-precision DSP blocks	256	256
	18 x 18 multipliers	512	512
Architectural Features	Global clock networks	16	
	Regional clock networks	92	
	Design security	✓	
I/O Features	I/O voltage levels supported (V)	1.2, 1.5, 1.8, 2.5, 3.3[2]	
	I/O standards supported	LVTTL, LVCMOS, PCI™, PCI-X™, LVDS, mini-LVDS, RSDS, LVPECL, Differential SSTL-15, Differential SSTL-18, Differential SSTL-2, Differential HSTL-12, Differential HSTL-5, Differential HSTL-18, SSTL-15 (I and II), SSTL-18 (I and II), SSTL-2 (I and II), 1.2 V HSTL (I and II), 1.5 V HSTL (I and II), 1.8 V HSTL (I and II)	
	LVDS channels, 1.4 Gbps (receive/transmit)	150	150
	Embedded DPA circuitry	✓	
	OCT	Series, parallel, and differential	
	Transceiver count (28.05 Gbps/14.1 Gbps)	4/32	4/32
	PCIe hard IP blocks (Gen3)	1	1
	Memory devices supported	DDR3, DDR2, QDR II, QDR II+, RLDRAM II, RLDRAM 3	

[1] All data is correct at the time of printing, and may be subject to change without prior notice. For the latest information, please visit **www.altera.com**.

[2] 3.3 V compliant, requires a 3 V power supply.

Stratix V GX FPGA Features

		Maximum Resource Count for Stratix V GX FPGAs (0.85 V)[1]									
		5SGXA3	**5SGXA4**	**5SGXA5**	**5SGXA7**	**5SGXA9**	**5SGXAB**	**5SGXB5**	**5SGXB6**	**5SGXB9**	**5SGXBB**
Resources	ALMs	128,300	158,500	185,000	234,720	317,000	359,200	185,000	225,400	317,000	359,200
	LEs (K)	340	420	490	622	840	952	490	597	840	952
	Registers	513,200	634,000	740,000	938,880	1,268,000	1,436,800	740,000	901,600	1,268,000	1,436,800
	M20K memory blocks	957	1,900	2,304	2,560	2,640	2,640	2,100	2,660	2,640	2,640
	M20K memory (Mb)	19	37	45	50	52	52	41	52	52	52
	MLAB memory (Mb)	3.92	4.84	5.65	7.16	9.67	10.96	5.65	6.88	9.67	10.96
	Variable-precision DSP blocks	256	256	256	256	352	352	399	399	352	352
	18 x 18 multipliers	512	512	512	512	704	704	798	798	704	704
Architectural Features	Global clock networks	16									
	Regional clock networks	92									
	Design security	✓									
I/O Features	I/O voltage levels supported (V)	1.2, 1.5, 1.8, 2.5, 3.3[2]									
	I/O standards supported	LVTTL, LVCMOS, PCI, PCI-X, LVDS, mini-LVDS, RSDS, LVPECL, Differential SSTL-15, Differential SSTL-18, Differential SSTL-2, Differential HSTL-12, Differential HSTL-5, Differential HSTL-18, SSTL-15 (I and II), SSTL-18 (I and II), SSTL-2 (I and II), 1.2 V HSTL (I and II), 1.5 V HSTL (I and II), 1.8 V HSTL (I and II)									
	LVDS channels, 1.4 Gbps (receive/transmit)	174	174	210	210	210	210	150	150	150	150
	Embedded DPA circuitry	✓									
	OCT	Series, parallel, and differential									
	Transceiver count (14.1 Gbps)	36	36	48	48	48	48	66	66	66	66
	PCIe hard IP blocks (Gen3)	2	2	4	4	4	4	4	4	4	4
	Memory devices supported	DDR3, DDR2, QDR II, QDR II+, RLDRAM II, RLDRAM 3									

[1] All data is correct at the time of printing, and may be subject to change without prior notice. For the latest information, please visit **www.altera.com**.

[2] 3.3 V compliant, requires a 3 V power supply.

Stratix V GS FPGA Features

		Maximum Resource Count for Stratix V GS FPGAs (0.85 V)[1]				
		5SGSD3	5SGSD4	5SGSD5	5SGSD6	5SGSD8
Resources	ALMs	89,000	135,840	172,600	220,000	262,400
	LEs (K)	236	360	457	583	695
	Registers	356,000	543,360	690,400	880,000	1,049,600
	M20K memory blocks	688	957	2,014	2,320	2,567
	M20K memory (Mb)	13	19	39	45	50
	MLAB memory (Mb)	2.72	4.15	5.27	6.71	8.01
	Variable-precision DSP blocks	600	1,044	1,590	1,775	1,963
	18 x 18 multipliers	1,200	2,088	3,180	3,550	3,926
Architectural Features	Global clock networks	16				
	Regional clock networks	92				
	Design security	✓				
I/O Features	I/O voltage levels supported (V)	1.2, 1.5, 1.8, 2.5, 3.3[2]				
	I/O standards supported	LVTTL, LVCMOS, PCI, PCI-X, LVDS, mini-LVDS, RSDS, LVPECL, Differential SSTL-15, Differential SSTL-18, Differential SSTL-2, Differential HSTL-12, Differential HSTL-5, Differential HSTL-18, SSTL-15 (I and II), SSTL-18 (I and II), SSTL-2 (I and II), 1.2 V HSTL (I and II), 1.5 V HSTL (I and II), 1.8 V HSTL (I and II)				
	LVDS channels, 1.4 Gbps (receive/transmit)	108	174	174	210	210
	Embedded DPA circuitry	✓				
	OCT	Series, parallel, and differential				
	Transceiver count (14.1 Gbps)	24	36	36	48	48
	PCIe hard IP blocks (Gen3)	1	1	1	2	2
	Memory devices supported	DDR3, DDR2, DDR, QDR II, QDR II+, RLDRAM II, RLDRAM 3				

[1] All data is correct at the time of printing, and may be subject to change without prior notice. For the latest information, please visit **www.altera.com**.
[2] 3.3 V compliant, requires a 3 V power supply.

Stratix V E FPGA Features

		Maximum Resource Count for Stratix V E FPGAs (0.85 V)[1]	
		5SEE9	5SEEB
Resources	ALMs	317,000	359,200
	LEs (K)	840	952
	Registers	1,268,000	1,436,800
	M20K memory blocks	2,640	2,640
	M20K memory (Mb)	52	52
	MLAB memory (Mb)	9.67	10.96
	Variable-precision DSP blocks	352	352
	18 x 18 multipliers	704	704
Architectural Features	Global clock networks	16	
	Regional clock networks	92	
	Design security	✓	
I/O Features	I/O voltage levels supported (V)	1.2, 1.5, 1.8, 2.5, 3.3[2]	
	I/O standards supported	LVTTL, LVCMOS, PCI, PCI-X, LVDS, mini-LVDS, RSDS, LVPECL, Differential SSTL-15, Differential SSTL-18, Differential SSTL-2, Differential HSTL-12, Differential HSTL-5, Differential HSTL-18, SSTL-15 (I and II), SSTL-18 (I and II), SSTL-2 (I and II), 1.2 V HSTL (I and II), 1.5 V HSTL (I and II), 1.8 V HSTL (I and II)	
	LVDS channels, 1.4 Gbps (receive/transmit)	210	210
	Embedded DPA circuitry	✓	
	OCT	Series, parallel, and differential	
	Memory devices supported	DDR3, DDR2, QDR II, QDR II+, RLDRAM II, RLDRAM 3	

[1] All data is correct at the time of printing, and may be subject to change without prior notice. For the latest information, please visit **www.altera.com**.

[2] 3.3 V compliant, requires a 3 V power supply.

Stratix V FPGA Series Package and I/O Matrices

	Stratix V GS, GX, GT, and E FPGAs (0.85 V)[1]						
	FBGA (F)						
	780 pin 29 x 29 (mm) 1.0-mm pitch	**1,152 pin** 35 x 35 (mm) 1.0-mm pitch	**1,152 pin** 35 x 35 (mm) 1.0-mm pitch	**1,517 pin** 40 x 40 (mm) 1.0-mm pitch	**1,517 pin** 40 x 40 (mm) 1.0-mm pitch	**1,760 pin** 42.5 x 42.5 (mm) 1.0-mm pitch	**1,932 pin** 45 x 45 (mm) 1.0-mm pitch
5SGSD3	360, 90, 12[2]	432, 108, 24					
5SGSD4	360, 90, 12[2]	432, 108, 24		696, 174, 36			
5SGSD5		552, 138, 24		696, 174, 36			
5SGSD6				696, 174, 36			840, 210, 48
5SGSD8				696, 174, 36			840, 210, 48
5SGXA3	360, 90, 12[2]	432, 108, 24	432, 108, 36	696, 174, 36			
5SGXA4		552, 138, 24	432, 108, 36	696, 174, 36			
5SGXA5		552, 138, 24	432, 108, 36	696, 174, 36	600, 150, 48		840, 210, 48
5SGXA7		552, 138, 24	432, 108, 36	696, 174, 36	600, 150, 48		840, 210, 48
5SGXA9				696, 174, 36[3]			840, 210, 48
5SGXAB				696, 174, 36[3]			840, 210, 48
5SGXB5				432, 108, 66		600, 150, 66	
5SGXB6				432, 108, 66		600, 150, 66	
5SGXB9						600, 150, 66[3]	
5SGXBB						600, 150, 66[3]	
5SGTC5					600, 150, 36[4]		
5SGTC7					600, 150, 36[4]		
5SEE9				696, 174, 0[3]			840, 210, 0
5SEEB				696, 174, 0[3]			840, 210, 0

[1] All data is correct at the time of printing, and may be subject to change without prior notice. For the latest information, please visit **www.altera.com**.

[2] Hybrid package (flip chip) FBGA: 33 x 33 (mm) 1.0-mm pitch.

[3] Hybrid package (flip chip) FBGA: 45 x 45 (mm) 1.0-mm pitch.

[4] GX–GT migration. Unused transceiver channels connected to power/ground.

264, 66, 24 Numbers indicate GPIO count, LVDS count, and transceiver count.

Vertical migration (same V_{CC}, GND, ISP, and input pins). User I/Os may be less than labelled for vertical migration.

Stratix series devices are offered in commercial and industrial temperatures and RoHS-compliant packages. Stratix IV GT devices are only offered in industrial temperatures (0˚C to 100˚C).

Arria V GX FPGA Features

		Maximum Resource Count for Arria V GX FPGAs (1.1 V, 1.15 V)[1]							
		5AGXA1	5AGXA3	5AGXA5	5AGXA7	5AGXB1	5AGXB3	5AGXB5	5AGXB7
Resources	ALMs	28,302	58,900	71,698	91,680	113,208	136,880	158,491	190,240
	LEs (K)	75	156	190	242	300	362	420	504
	Registers	113,208	235,600	286,792	366,720	452,832	547,520	633,964	760,960
	M10K memory blocks	800	1,051	1,180	1,366	1,510	1,726	2,054	2,414
	M10K memory (Kb)	8,000	10,510	11,800	13,660	15,100	17,260	20,540	24,140
	MLAB memory (Kb)	463	961	1,173	1,448	1,852	2,098	2,532	2,906
	Variable-precision DSP blocks	240	396	600	800	920	1,045	1,092	1,156
	18 x 18 multipliers	480	792	1,200	1,600	1,840	2,090	2,184	2,312
Architectural Features	Global clock networks	16							
	PLLs[2]	10	10	12	12	12	12	16	16
	Design security	✓							
I/O Features	I/O voltage levels supported (V)	1.2, 1.5, 1.8, 2.5, 3.0, 3.3							
	I/O standards supported	LVTTL, LVCMOS, PCI, PCI-X, LVDS, mini-LVDS, RSDS, LVPECL, Differential SSTL-15, Differential SSTL-18, Differential SSTL-2, Differential HSTL-12, Differential HSTL-15, Differential HSTL-18, SSTL-15 (I and II), SSTL-18 (I and II), SSTL-2 (I and II), 1.2 V HSTL (I and II), 1.5 V HSTL (I and II), 1.8 V HSTL (I and II)							
	LVDS transmitter (TX)	70	70	120	120	160	160	160	160
	LVDS receiver (RX)	80	80	136	136	176	176	176	176
	Embedded DPA circuitry	✓							
	OCT	Series and differential							
	Programmable drive strength	✓							
	Transceiver count (6.5536 Gbps)	9	9	24	24	24	24	36	36
	PCIe hard IP blocks (Gen2 x4)	1	1	2	2	2	2	2	2
	Hard memory controllers[3]	2	2	4	4	4	4	4	4
External Memory Interfaces	Memory devices supported	DDR3, DDR2, DDR II+[4], QDR II, QDR II+, RLDRAM II, LPDDR[4], LPDDR2[4]							

[1] All data is correct at the time of printing, and may be subject to change without prior notice. For the latest information, please visit **www.altera.com**.

[2] The phase-locked loop (PLL) count includes general-purpose fractional PLLs and transceiver fractional PLLs.

[3] With 16 and 32 bit error correction code (ECC) support.

[4] These memory interfaces are not available as Altera IP.

Arria V GT FPGA Features

		Maximum Resource Count for Arria V GT FPGAs (1.1 V, 1.15 V)[1]			
		5AGTC3	5AGTC7	5AGTD3	5AGTD7
Resources	ALMs	58,900	91,680	136,880	190,240
	LEs (K)	156	242	362	504
	Registers	235,600	366,720	547,520	760,960
	M10K memory blocks	1,051	1,366	1,726	2,414
	M10K memory (Kb)	10,510	13,660	17,260	24,140
	MLAB memory (Kb)	961	1,448	2,098	2,906
	Variable-precision DSP blocks	396	800	1,045	1,156
	18 x 18 multipliers	792	1,600	2,090	2,312
Architectural Features	Global clock networks	16			
	PLLs[2]	10	12	12	16
	Design security	✓			
I/O Features	I/O voltage levels supported (V)	1.2, 1.5, 1.8, 2.5, 3.0, 3.3			
	I/O standards supported	LVTTL, LVCMOS, PCI, PCI-X, LVDS, mini-LVDS, RSDS, LVPECL, Differential SSTL-15, Differential SSTL-18, Differential SSTL-2, Differential HSTL-12, Differential HSTL-15, Differential HSTL-18, SSTL-15 (I and II), SSTL-18 (I and II), SSTL-2 (I and II), 1.2 V HSTL (I and II), 1.5 V HSTL (I and II), 1.8 V HSTL (I and II)			
	LVDS transmitter (TX)	70	120	160	160
	LVDS receiver (RX)	80	136	176	176
	Embedded DPA circuitry	✓			
	OCT	Series and differential			
	Programmable drive strength	✓			
	Transceiver count (10.3125 Gbps/6.5536 Gbps)[3]	4/3	12/6	12/6	20/6
	PCIe hard IP blocks (Gen2 x4)	1	2	2	2
	Hard memory controllers[4]	2	4	4	4
External Memory Interfaces	Memory devices supported	DDR3, DDR2, DDR II+[5], QDR II, QDR II+, RLDRAM II, LPDDR[5], LPDDR2[5]			

[1] All data is correct at the time of printing, and may be subject to change without prior notice. For the latest information, please visit **www.altera.com**.

[2] The PLL count includes general-purpose fractional PLLs and transceiver fractional PLLs.

[3] One pair of 10 Gbps transceiver channels can be configured as three 6 Gbps transceiver channels.

[4] With 16 and 32 bit ECC support.

[5] These memory interfaces are not available as Altera IP.

Arria V GZ FPGA Features

		Maximum Resource Count for Arria V GZ FPGAs (0.85 V)[1]			
		5AGZE1	5AGZE3	5AGZE5	5AGZE7
Resources	ALMs	83,020	135,840	150,960	169,800
	LEs (K)	220	360	400	450
	Registers	332,080	543,360	603,840	679,200
	M20K memory blocks	585	957	1,440	1,700
	M20K memory (Kb)	11,700	19,140	28,800	34,000
	MLAB memory (Kb)	2,594	4,245	4,718	5,306
	Variable-precision DSP blocks	800	1,044	1,092	1,139
	18 x 18 multipliers	1,600	2,088	2,184	2,278
Architectural Features	Global clock networks	16			
	PLLs[2]	20	20	24	24
	Design security	✓			
I/O Features	I/O voltage levels supported (V)	1.2, 1.5, 1.8, 2.5, 3.0, 3.3[3]			
	I/O standards supported	LVTTL, LVCMOS, PCI, PCI-X, LVDS, mini-LVDS, RSDS, LVPECL, Differential SSTL-15, Differential SSTL-18, Differential SSTL-2, Differential HSTL-12, Differential HSTL-15, Differential HSTL-18, SSTL-15 (I and II), SSTL-18 (I and II), SSTL-2 (I and II), 1.2 V HSTL (I and II), 1.5 V HSTL (I and II), 1.8 V HSTL (I and II)			
	LVDS transmitter (TX)	99	99	166	166
	LVDS receiver (RX)	108	108	168	168
	Embedded DPA circuitry	✓			
	OCT	Series and differential			
	Programmable drive strength	✓			
	Transceiver count (12.5 Gbps)	24	24	36	36
	PCIe hard IP blocks (Gen2 x8, Gen3)	1	1	1	1
External Memory Interfaces	Memory devices supported	DDR3, DDR2, QDR II, QDR II+, RLDRAM II, RLDRAM 3			

[1] All data is correct at the time of printing, and may be subject to change without prior notice. For the latest information, please visit **www.altera.com.**

[2] The PLL count includes general-purpose fractional PLLs and transceiver fractional PLLs.

[3] 3.3 V compliant, requires a 3 V power supply.

Arria V SX SoC Features

		Maximum Resource Count for Arria V SX SoCs (1.1 V)[1]	
		5ASXB3	5ASXB5
Resources	ALMs	132,075	174,340
	LEs (K)	350	462
	Registers	528,300	697,360
	M10K memory blocks	1,729	2,282
	M10K memory (Kb)	17,288	22,820
	MLAB memory (Kb)	2,014	2,658
	Variable-precision DSP blocks	809	1,090
	18 x 18 multipliers	1,618	2,180
Architectural Features	Processor cores (ARM Cortex-A9)	Dual	Dual
	Maximum CPU Clock Frequency	1.05 GHz	1.05 GHz
	Global clock networks	16	
	PLLs[2] (FPGA)	14	14
	PLLs[2] (HPS)	3	3
	Design security	✓	
I/O Features	I/O voltage levels supported (V)	1.2, 1.5, 1.8, 2.5, 3.0, 3.3	
	I/O standards supported	LVTTL, LVCMOS, PCI, PCI-X, LVDS, mini-LVDS, RSDS, LVPECL, Differential SSTL-15, Differential SSTL-18, Differential SSTL-2, Differential HSTL-12, Differential HSTL-15, Differential HSTL-18, SSTL-15 (I and II), SSTL-18 (I and II), SSTL-2 (I and II), 1.2 V HSTL (I and II), 1.5 V HSTL (I and II), 1.8 V HSTL (I and II)	
	LVDS transmitter (TX)	136	136
	LVDS receiver (RX)	120	120
	Embedded DPA circuitry	✓	
	OCT	Series and differential	
	Programmable drive strength	✓	
	Transceiver count (6.5536 Gbps)	30	30
	PCIe hard IP blocks (Gen2 x4)	2	2
	GPIOs (FPGA)	540	540
	GPIOs (HPS)	208	208
	Hard memory controllers[3] (FPGA)	3	3
	Hard memory controllers[3] (HPS)	1	1
External Memory Interfaces	Memory devices supported	DDR3, DDR2, DDR, QDR II, QDR II+, RLDRAM II, LPDDR2[4], SDR	

[1] All data is correct at the time of printing, and may be subject to change without prior notice. For the latest information, please visit **www.altera.com.**

[2] The PLL count includes general-purpose fractional PLLs and transceiver fractional PLLs.

[3] With 16 and 32 bit ECC support.

[4] These memory interfaces are not available as Altera IP.

Arria V ST SoC Features

		Maximum Resource Count for Arria V ST SoCs (1.1 V)[1]	
		5ASTD3	5ASTD5
Resources	ALMs	132,075	174,340
	LEs (K)	350	462
	Registers	528,300	697,360
	M10K memory blocks	1,729	2,282
	M10K memory (Kb)	17,288	22,820
	MLAB memory (Kb)	2,014	2,658
	Variable-precision DSP blocks	809	1,090
	18 x 18 multipliers	1,618	2,180
Architectural Features	Processor cores (ARM Cortex-A9)	Dual	Dual
	Maximum CPU Clock Frequency	1.05 GHz	1.05 GHz
	Global clock networks	16	
	PLLs[2] (FPGA)	14	14
	PLLs[2] (HPS)	3	3
	Design security	✓	
I/O Features	I/O voltage levels supported (V)	1.2, 1.5, 1.8, 2.5, 3.0, 3.3	
	I/O standards supported	LVTTL, LVCMOS, PCI, PCI-X, LVDS, mini-LVDS, RSDS, LVPECL, Differential SSTL-15, Differential SSTL-18, Differential SSTL-2, Differential HSTL-12, Differential HSTL-15, Differential HSTL-18, SSTL-15 (I and II), SSTL-18 (I and II), SSTL-2 (I and II), 1.2 V HSTL (I and II), 1.5 V HSTL (I and II), 1.8 V HSTL (I and II)	
	LVDS transmitter (TX)	136	136
	LVDS receiver (RX)	120	120
	Embedded DPA circuitry	✓	
	OCT	Series and differential	
	Programmable drive strength	✓	
	Transceiver count (10.3125 Gbps/6.5536 Gbps)	16/30	16/30
	PCIe hard IP blocks (Gen2 x4)	2	2
	GPIOs (FPGA)	540	540
	GPIOs (HPS)	208	208
	Hard memory controllers[3] (FPGA)	3	3
	Hard memory controllers[3] (HPS)	1	1
External Memory Interfaces	Memory devices supported	DDR3, DDR2, DDR, QDR II, QDR II+, RLDRAM II, LPDDR2[4], SDR	

[1] All data is correct at the time of printing, and may be subject to change without prior notice. For the latest information, please visit **www.altera.com.**

[2] The PLL count includes general-purpose fractional PLLs and transceiver fractional PLLs.

[3] With 16 and 32 bit ECC support.

[4] These memory interfaces are not available as Altera IP.

Arria V FPGA Series Package and I/O Matrices

	Arria V GX,GT, and GZ FPGAs (0.85 V)[1]					
	FBGA (F)	Hybrid FBGA (H)	FBGA (F)			
	672 pin 27 x 27 (mm) 1.0-mm pitch	**780 pin** 29 x 29 (mm) 1.0-mm pitch	**896 pin** 31 x 31 (mm) 1.0-mm pitch		**1,152 pin** 35 x 35 (mm) 1.0-mm pitch	**1,517 pin** 40 x 40 (mm) 1.0-mm pitch
5AGXA1	336 9,0		416 9,0	320 9,0		
5AGXA3	336 9,0		416 9,0	320 9,0		
5AGXA5	336 9,0		384 18,0	320 9,0	544 24,0	
5AGXA7	336 9,0		384 18,0	320 9,0	544 24,0	
5AGXB1			384 18,0	320 9,0	544 24,0	704 24,0
5AGXB3			384 18,0	320 9,0	544 24,0	704 24,0
5AGXB5					544 24,0	704 36,0
5AGXB7					544 24,0	704 36,0
5AGTC3	336 3,4		416 3,4	320 3,4		
5AGTC7			384 6,8	320 3,4	544 6,12	
5AGTD3			384 6,8	320 3,4	544 6,12	704 6,12
5AGTD7					544 6,12	704 6,20
5AGZE1		342 12			414 24	
5AGZE3		342 12			414 24	
5AGZE5					534 24	674 36
5AGZE7					534 24	674 36

[1] All data is correct at the time of printing, and may be subject to change without prior notice. For the latest information, please visit **www.altera.com.**

636 / 8,0 — For Arria V GX and GT devices, values on top indicate available user I/O pins; for Arria V GX and GT, values at the bottom indicate the 6.5536 Gbps and 10.3125 Gbps transceiver count. One pair of 10 Gbps transceiver channels can be configured as three 6 Gbps transceiver channels. For Arria V GZ device, values on top indicate available user I/O pins; values at the bottom indicate the 12.5 Gbps transceiver count.

Vertical migration (same V_{CC}, GND, ISP, and input pins). I/O pins can be migrated across device variants indicated with vertical migration lines of the same color. For vertical migration, the number of user I/Os may be less than the number stated in the table.

Vertical migration is possible only if you use up to 320 I/O pins, up to nine 6.5536 Gbps transceiver count (for Arria V GX devices), and up to four 10.3125 Gbps transceiver count (for Arria V GT devices).

Arria V FPGA Series Package and I/O Matrices

	Arria V SX and ST SoCs (1.1 V)[1]		
	FBGA (F)		
	896 pin 31 x 31 (mm) 1.0-mm pitch	**1,152 pin** 35 x 35 (mm) 1.0-mm pitch	**1,517 pin** 40 x 40 (mm) 1.0-mm pitch
5ASXB3	250, 208 12+0	385, 208 18+0	540, 208 30+0
5ASXB5	250, 208 12+0	385, 208 18+0	540, 208 30+0
5ASTD3	250, 208 12+6	385, 208 18+8	540, 208 30+16
5ASTD5	250, 208 12+6	385, 208 18+8	540, 208 30+16

[1] All data is correct at the time of printing, and may be subject to change without prior notice. For the latest information, please visit **www.altera.com.**

636, 216 / 8+0 Values on top indicate available FPGA user I/O pins and HPS I/O pins; values at the bottom indicate the 6.5536 Gbps plus 10.3125 Gbps transceiver count.

Vertical migration (same V_{CC}, GND, ISP, and input pins). For vertical migration, the number of user I/Os may be less than the number stated in the table.

Cyclone V E FPGA Features

		Maximum Resource Count for Cyclone® V E FPGAs (1.1 V)[1]				
		5CEA2	5CEA4	5CEA5	5CEA7	5CEA9
Resources	ALMs	9,434	18,480	29,080	56,480	113,560
	LEs (K)	25	49	77	149.5	301
	Registers	37,736	73,920	116,320	225,920	454,240
	M10K memory blocks	176	308	446	686	1,220
	M10K memory (Kb)	1,760	3,080	4,460	6,860	12,200
	MLAB memory (Kb)	196	303	424	836	1,717
	Variable-precision DSP blocks	25	66	150	156	342
	18 x 18 multipliers	50	132	300	312	684
Architectural Features	Global clock networks	16				
	PLLs	4	4	6	6	6
	Design security	✓				
I/O Features	I/O voltage levels supported (V)	1.1, 1.2, 1.5, 1.8, 2.5, 3.3				
	I/O standards supported	LVTTL, LVCMOS, PCI, PCI-X, LVDS, mini-LVDS, RSDS, LVPECL, Differential SSTL-15, Differential SSTL-18, Differential SSTL-2, Differential HSTL-12, Differential HSTL-15, Differential HSTL-18, SSTL-15 (I and II), SSTL-18 (I and II), SSTL-2 (I and II), 1.2 V HSTL (I and II), 1.5 V HSTL (I and II), 1.8 V HSTL (I and II), HiSpi, SLVS, Sub-LVDS				
	LVDS channels, 875 Mbps receive, 840 Mbps transmit	56	56	60	120	120
	Embedded DPA circuitry	–				
	OCT	Series and differential				
	Programmable drive strength	✓				
	PCIe hard IP blocks	–				
	Hard memory controllers[2]	1	1	2	2	2
External Memory Interfaces	Memory devices supported	DDR3, DDR2, LPDDR2				

[1] All data is correct at the time of printing, and may be subject to change without prior notice. For the latest information, please visit **www.altera.com.**

[2] With 16 and 32 bit ECC support.

Cyclone V GX FPGA Features

		Maximum Resource Count for Cyclone V GX FPGAs (1.1 V)[1]				
		5CGXC3	5CGXC4	5CGXC5	5CGXC7	5CGXC9
Resources	ALMs	13,460	18,868	29,080	56,480	113,560
	LEs (K)	35.5	50	77	149.5	301
	Registers	53,840	75,472	116,320	225,920	454,240
	M10K memory blocks	135	250	446	686	1,220
	M10K memory (Kb)	1,350	2,500	4,460	6,860	12,200
	MLAB memory (Kb)	291	295	424	836	1,717
	Variable-precision DSP blocks	57	70	150	156	342
	18 x 18 multipliers	114	140	300	312	684
Architectural Features	Global clock networks	16				
	PLLs[2]	4	6	6	7	8
	Design security	✓				
I/O Features	I/O voltage levels supported (V)	1.1, 1.2, 1.5, 1.8, 2.5, 3.3				
	I/O standards supported	LVTTL, LVCMOS, PCI, PCI-X, LVDS, mini-LVDS, RSDS, LVPECL, Differential SSTL-15, Differential SSTL-18, Differential SSTL-2, Differential HSTL-12, Differential HSTL-15, Differential HSTL-18, SSTL-15 (I and II), SSTL-18 (I and II), SSTL-2 (I and II), 1.2 V HSTL (I and II), 1.5 V HSTL (I and II), 1.8 V HSTL (I and II), HiSpi, SLVS, Sub-LVDS				
	LVDS channels, 875 Mbps receive, 840 Mbps transmit	52	84	84	120	140
	Embedded DPA circuitry	–				
	OCT	Series and differential				
	Programmable drive strength	✓				
	Transceiver count (3.125 Gbps)	3	6	6	9	12
	PCIe hard IP blocks (Gen1 x4)	1	2	2	2	2
	Hard memory controllers[3]	1	2	2	2	2
External Memory Interfaces	Memory devices supported	DDR3, DDR2, LPDDR2				

[1] All data is correct at the time of printing, and may be subject to change without prior notice. For the latest information, please visit **www.altera.com.**

[2] The PLL count includes general-purpose fractional PLLs and transceiver fractional PLLs.

[3] With 16 and 32 bit ECC support.

Cyclone V GT FPGA Features

		Maximum Resource Count for Cyclone V GT FPGAs (1.1 V)[1]		
		5CGTD5	5CGTD7	5CGTD9
Resources	ALMs	29,080	56,480	113,560
	LEs (K)	77	149.5	301
	Registers	116,320	225,920	454,240
	M10K memory blocks	446	686	1,220
	M10K memory (Kb)	4,460	6,860	12,200
	MLAB memory (Kb)	424	836	1,717
	Variable-precision DSP blocks	150	156	342
	18 x 18 multipliers	300	312	684
Architectural Features	Global clock networks	16		
	PLLs[2]	6	7	8
	Design security	✓		
I/O Features	I/O voltage levels supported (V)	1.1, 1.2, 1.5, 1.8, 2.5, 3.3		
	I/O standards supported	LLVTTL, LVCMOS, PCI, PCI-X, LVDS, mini-LVDS, RSDS, LVPECL, Differential SSTL-15, Differential SSTL-18, Differential SSTL-2, Differential HSTL-12, Differential HSTL-15, Differential HSTL-18, SSTL-15 (I and II), SSTL-18 (I and II), SSTL-2 (I and II), 1.2 V HSTL (I and II), 1.5 V HSTL (I and II), 1.8 V HSTL (I and II), HiSpi, SLVS, Sub-LVDS		
	LVDS channels, 875 Mbps receive, 840 Mbps transmit	84	120	140
	Embedded DPA circuitry	–		
	OCT	Series and differential		
	Programmable drive strength	✓		
	Transceiver count (6.144 Gbps)[4]	6	9	12
	PCIe hard IP blocks (Gen2 x1, x2, and x4, Gen1 x4)	2	2	2
	Hard memory controllers[3]	2	2	2
External Memory Interfaces	Memory devices supported	DDR3, DDR2, LPDDR2		

[1] All data is correct at the time of printing, and may be subject to change without prior notice. For the latest information, please visit **www.altera.com.**

[2] The PLL count includes general-purpose fractional PLLs and transceiver fractional PLLs.

[3] With 16 and 32 bit ECC support.

[4] Automotive Grade GT comes with 5 Gbps transceiver.

Cyclone V SE SoC Features

		Maximum Resource Count for Cyclone V SE SoCs (1.1 V)[1]			
		5CSEA2	5CSEA4	5CSEA5	5CSEA6
Resources	ALMs	9,434	15,094	32,075	41,509
	LEs (K)	25	40	85	110
	Registers	37,736	60,376	128,300	166,036
	M10K memory blocks	140	270	397	557
	M10K memory (Kb)	1,400	2,700	3,970	5,570
	MLAB memory (Kb)	138	231	480	621
	Variable-precision DSP blocks	36	84	87	112
	18 x 18 multipliers	72	168	174	224
Architectural Features	Processor cores (ARM Cortex-A9)	Single or dual	Single or dual	Single or dual	Single or dual
	Maximum CPU Clock Frequency	925 MHz	925 MHz	925 MHz	925 MHz
	Global clock networks	16			
	PLLs[2] (FPGA)	5	5	6	6
	PLLs[2] (HPS)	3	3	3	3
	Design security	✓			
I/O Features	I/O voltage levels supported (V)	1.1, 1.2, 1.5, 1.8, 2.5, 3.3			
	I/O standards supported	LVTTL, LVCMOS, PCI, PCI-X, LVDS, mini-LVDS, RSDS, LVPECL, Differential SSTL-15, Differential SSTL-18, Differential SSTL-2, Differential HSTL-12, Differential HSTL-15, Differential HSTL-18, SSTL-15 (I and II), SSTL-18 (I and II), SSTL-2 (I and II), 1.2 V HSTL (I and II), 1.5 V HSTL (I and II), 1.8 V HSTL (I and II), HiSpi, SLVS, Sub-LVDS			
	LVDS channels, 875 Mbps receive, 840 Mbps transmit	37, 32	37, 32	72, 72	72, 72
	Embedded DPA circuitry	–			
	OCT	Series and differential			
	Programmable drive strength	✓			
	PCIe hard IP blocks	–			
	GPIOs (FPGA)	145	145	288	288
	GPIOs (HPS)	181	181	181	181
	Hard memory controllers[3] (FPGA)	1	1	1	1
	Hard memory controllers[3] (HPS)	1	1	1	1
External Memory Interfaces	Memory devices supported	DDR3, DDR2, LPDDR2			

[1] All data is correct at the time of printing, and may be subject to change without prior notice. For the latest information, please visit **www.altera.com.**

[2] The PLL count includes general-purpose fractional PLLs and transceiver fractional PLLs.

[3] With 16 and 32 bit ECC support.

Cyclone V SX SoC Features

		Maximum Resource Count for Cyclone V SX SoCs (1.1 V)[1]			
		5CSXC2	5CSXC4	5CSXC5	5CSXC6
Resources	ALMs	9,434	15,094	32,075	41,509
	LEs (K)	25	40	85	110
	Registers	37,736	60,376	128,300	166,036
	M10K memory blocks	140	270	397	557
	M10K memory (Kb)	1,400	2,700	3,970	5,570
	MLAB memory (Kb)	138	231	480	621
	Variable-precision DSP blocks	36	84	87	112
	18 x 18 multipliers	72	168	174	224
Architectural Features	Processor cores (ARM Cortex-A9)	Dual	Dual	Dual	Dual
	Maximum CPU Clock Frequency	925 MHz	925 MHz	925 MHz	925 MHz
	Global clock networks	16			
	PLLs[2] (FPGA)	5	5	6	6
	PLLs[2] (HPS)	3	3	3	3
	Design security	✓			
I/O Features	I/O voltage levels supported (V)	1.1, 1.2, 1.5, 1.8, 2.5, 3.3			
	I/O standards supported	LVTTL, LVCMOS, PCI, PCI-X, LVDS, mini-LVDS, RSDS, LVPECL, Differential SSTL-15, Differential SSTL-18, Differential SSTL-2, Differential HSTL-12, Differential HSTL-15, Differential HSTL-18, SSTL-15 (I and II), SSTL-18 (I and II), SSTL-2 (I and II), 1.2 V HSTL (I and II), 1.5 V HSTL (I and II), 1.8 V HSTL (I and II), HiSpi, SLVS, Sub-LVDS			
	LVDS channels, 875 Mbps receive, 840 Mbps transmit	37, 32	37, 32	72, 72	72, 72
	Embedded DPA circuitry	–			
	OCT	Series and differential			
	Programmable drive strength	✓			
	Transceiver count (3.125 Gbps)	6	6	9	9
	PCIe hard IP blocks (Gen1 x4)	2	2	2	2
	GPIOs (FPGA)	145	145	288	288
	GPIOs (HPS)	181	181	181	181
	Hard memory controllers[3] (FPGA)	1	1	1	1
	Hard memory controllers[3] (HPS)	1	1	1	1
External Memory Interfaces	Memory devices supported	DDR3, DDR2, LPDDR2			

[1] All data is correct at the time of printing, and may be subject to change without prior notice. For the latest information, please visit **www.altera.com.**

[2] The PLL count includes general-purpose fractional PLLs and transceiver fractional PLLs.

[3] With 16 and 32 bit ECC support.

Cyclone V ST SoC Features

		Maximum Resource Count for Cyclone V ST SoCs (1.1 V)[1]	
		5CSTD5	5CSTD6
Resources	ALMs	32,075	41,509
	LEs (K)	85	110
	Registers	128,300	166,036
	M10K memory blocks	397	557
	M10K memory (Kb)	3,970	5,570
	MLAB memory (Kb)	480	621
	Variable-precision DSP blocks	87	112
	18 x 18 multipliers	174	224
Architectural Features	Processor cores (ARM Cortex-A9)	Dual	Dual
	Maximum CPU Clock Frequency	925 MHz	925 MHz
	Global clock networks	16	
	PLLs[2] (FPGA)	6	6
	PLLs[2] (HPS)	3	3
	Design security	✓	
I/O Features	I/O voltage levels supported (V)	1.1, 1.2, 1.5, 1.8, 2.5, 3.3	
	I/O standards supported	LLVTTL, LVCMOS, PCI, PCI-X, LVDS, mini-LVDS, RSDS, LVPECL, Differential SSTL-15, Differential SSTL-18, Differential SSTL-2, Differential HSTL-12, Differential HSTL-15, Differential HSTL-18, SSTL-15 (I and II), SSTL-18 (I and II), SSTL-2 (I and II), 1.2 V HSTL (I and II), 1.5 V HSTL (I and II), 1.8 V HSTL (I and II), HiSpi, SLVS, Sub-LVDS	
	LVDS channels, 875 Mbps receive, 840 Mbps transmit	72	72
	Embedded DPA circuitry	–	
	OCT	Series and differential	
	Programmable drive strength	✓	
	Transceiver count (5 Gbps)	9	9
	PCIe hard IP blocks (Gen2 x1,x2, and x4, Gen1 x4)	2	2
	GPIOs (FPGA)	288	288
	GPIOs (HPS)	181	181
	Hard memory controllers[3] (FPGA)	1	1
	Hard memory controllers[3] (HPS)	1	1
External Memory Interfaces	Memory devices supported	DDR3, DDR2, LPDDR2	

[1] All data is correct at the time of printing, and may be subject to change without prior notice. For the latest information, please visit **www.altera.com.**

[2] The PLL count includes general-purpose fractional PLLs and transceiver fractional PLLs.

[3] With 16 and 32 bit ECC support.

Cyclone V FPGA Series Package and I/O Matrices

	Cyclone V E, GX, and GT FPGAs (1.1 V)[1]									
	MBGA (M)			UBGA (U)		FBGA (F)				
	301 pin 11 x 11 (mm) 0.5-mm pitch	**383 pin** 13 x 13 (mm) 0.5-mm pitch	**484 pin** 15 x 15 (mm) 0.5-mm pitch	**324 pin** 15 x 15 (mm) 0.8-mm pitch	**484 pin** 19 x 19 (mm) 0.8-mm pitch	**256 pin** 17 x 17 (mm) 1.0-mm pitch	**484 pin** 23 x 23 (mm) 1.0-mm pitch	**672 pin** 27 x 27 (mm) 1.0-mm pitch	**896 pin** 31 x 31 (mm) 1.0-mm pitch	**1,152 pin** 35 x 35 (mm) 1.0-mm pitch
5CEA2		223		176	224	128	224			
5CEA4		223		176	224	128	224			
5CEA5		175			224		240			
5CEA7			240		240		240	336	480	
5CEA9					240		224	336	480	
5CGXC3				144 3	208 3		208 3			
5CGXC4	129 4	175 6			224 6		240 6	336 6		
5CGXC5	129 4	175 6			224 6		240 6	336 6		
5CGXC7			240 3		240 6		240 6	336 9	480 9	
5CGXC9					240 5		224 6	336 9	480 12	560 12
5CGTD5	129 4	175 6			224 6		240 6	336 6		
5CGTD7			240 3		240 6		240 6	336 9	480 9	
5CGTD9					240 5		224 6	336 9	480 12	560 12

[1] All data is correct at the time of printing, and may be subject to change without prior notice. For the latest information, please visit **www.altera.com.**

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12 Values on top indicate available user I/O pins; values at the bottom indicate the 3.125 Gbps, 5 Gbps, or 6.144 Gbps transceiver count.

Vertical migration (same V_{CC}, GND, ISP, and input pins). For vertical migration, the number of user I/Os may be less than the number stated in the table.

This vertical migration can be achieved if you use only up to 175 GPIOs.

Cyclone V FPGA Series Package and I/O Matrices

	Cyclone V SE, SX, and ST SoCs (1.1 V)[1]		
	UBGA (U)		FBGA (F)
	484 pin 19 x 19 (mm) 0.8-mm pitch	**672 pin** 23 x 23 (mm) 0.8-mm pitch	**896 pin** 31 x 31 (mm) 1.0-mm pitch
5CSEA2	66, 151 0	145, 181 0	
5CSEA4	66, 151 0	145, 181 0	
5CSEA5	66, 151 0	145, 181 0	288, 181 0
5CSEA6	66, 151 0	145, 181 0	288, 181 0
5CSXC2		145, 181 6	
5CSXC4		145, 181 6	
5CSXC5		145, 181 9	288, 181 9
5CSXC6		145, 181 9	288, 181 9
5CSTD5			288, 181 9
5CSTD6			288, 181 9

[1] All data is correct at the time of printing, and may be subject to change without prior notice. For the latest information, please visit **www.altera.com.**

636, 161 / 12 Values on top indicate available FPGA user I/O pins and HPS I/O pins; values at the bottom indicate the 3.125 Gbps or 5 Gbps transceiver count.

Vertical migration (same V_{CC}, GND, ISP, and input pins). For vertical migration, the number of user I/Os may be less than the number stated in the table.

This vertical migration can be achieved if you use only up to 138 GPIOs.

Stratix IV GT FPGA Features

		Maximum Resource Count for Stratix IV GT FPGAs (0.95 V)[1]					
		EP4S40G2	**EP4S40G5**	**EP4S100G2**	**EP4S100G3**	**EP4S100G4**	**EP4S100G5**
Resources	ALMs	91,200	212,480	91,200	116,480	141,440	212,480
	LEs (K)	228	531	228	291	354	531
	Registers[2]	182,400	424,960	182,400	232,960	282,880	424,960
	M9K memory blocks	1,235	1,280	1,235	936	1,248	1,280
	M144K memory blocks	22	64	22	36	48	64
	MLAB memory (Kb)	2,850	6,640	2,850	3,640	4,420	6,640
	Embedded memory (Kb)	14,283	20,736	14,283	13,608	18,144	20,736
	18 x 18 multipliers	1,288	1,024	1,288	832	1,024	1,024
Architectural Features	Global clock networks	16					
	Regional clock networks	64	88	64	88	88	88
	Periphery clock networks	88	112	88	112	112	112
	PLLs	8	8	8	12	12	12
	Design security	✓					
	Others	Plug & Play Signal Integrity, Programmable Power Technology					
I/O Features	I/O voltage levels supported (V)	1.2, 1.5, 1.8, 2.5, 3.3[3]					
	I/O standards supported	LVTTL, LVCMOS, PCI, PCI-X, LVDS, mini-LVDS, RSDS, LVPECL, Differential SSTL-15, Differential SSTL-18, Differential SSTL-2, Differential HSTL-12, Differential HSTL-15, Differential HSTL-18, SSTL-15 (I and II), SSTL-18 (I and II), SSTL-2 (I and II), 1.2 V HSTL (I and II), 1.5 V HSTL (I and II), 1.8 V HSTL (I and II)					
	Emulated LVDS channels, 1,100 Mbps	192	256	192	256	256	256
	LVDS channels, 1,600 Mbps (receive/transmit)	46/46					
	Embedded DPA circuitry	✓					
	OCT	Series, parallel, and differential					
	Transceiver count[4] (11.3 Gbps/8.5 Gbps/6.5 Gbps)	12/12/12	12/12/12	24/0/12	24/8/16	24/8/16	32/0/16
	PCIe hard IP blocks	2	2	2	4	4	4
	Memory devices supported	DDR3, DDR2, DDR, QDR II, QDR II+, RLDRAM 2, SDR					

[1] Available in industrial temperatures only (0°C to 100°C).

[2] This is the base core logic register count. The ALM can support three registers when used in LUTREG mode, which increases total register count by an additional 50 percent.

[3] 3.3 V compliant, requires a 3 V power supply.

[4] The total transceiver count is the sum of 11.3 Gbps plus 8.5 Gbps plus 6.5 Gbps transceivers.

Stratix IV GX FPGA Features

		Maximum Resource Count for Stratix IV GX FPGAs (0.9 V)						
		EP4SGX70	EP4SGX110	EP4SGX180	EP4SGX230	EP4SGX290	EP4SGX360	EP4SGX530
Resources	ALMs	29,040	42,240	70,300	91,200	116,480	141,440	212,480
	LEs (K)	73	106	176	228	291	354	531
	Registers[1]	58,080	84,480	140,600	182,400	232,960	282,880	424,960
	M9K memory blocks	462	660	950	1,235	936	1,248	1,280
	M144K memory blocks	16	16	20	22	36	48	64
	MLAB memory (Kb)	908	1,320	2,197	2,850	3,640	4,420	6,640
	Embedded memory (Kb)	6,462	8,244	11,430	14,283	13,608	18,144	20,736
	18 x 18 multipliers	384	512	920	1,288	832	1,040[2]	1,024
Architectural Features	Global clock networks	16						
	Regional clock networks	64	64	64	64	88	88	88
	Periphery clock networks	56	56	88	88	88	88	112
	PLLs	4	4	8	8	12	12	12
	Design security	✓						
	Others	Plug & Play Signal Integrity, Programmable Power Technology						
I/O Features	I/O voltage levels supported (V)	1.2, 1.5, 1.8, 2.5, 3.3[4]						
	I/O standards supported	LVTTL, LVCMOS, PCI, PCI-X, LVDS, mini-LVDS, RSDS, LVPECL, Differential SSTL-15, Differential SSTL-18, Differential SSTL-2, Differential HSTL-12, Differential HSTL-15, Differential HSTL-18, SSTL-15 (I and II), SSTL-18 (I and II), SSTL-2 (I and II), 1.2 V HSTL (I and II), 1.5 V HSTL (I and II), 1.8 V HSTL (I and II)						
	Emulated LVDS channels, 1,100 Mbps	128	128	192	192	256	256	256
	LVDS channels, 1,600 Mbps (receive/transmit)	56/56	56/56	88/88	88/88	98/98	98/98	98/98
	Embedded DPA circuitry							
	OCT	Series, parallel, and differential						
	Transceiver count (8.5 Gbps/6.5 Gbps)[5]	16/8	16/8	24/12	24/12	32/16	32/16	32/16
	PCIe hard IP blocks	2	2	2	2	4	4	4
	Memory devices supported	DDR3, DDR2, DDR, QDR II, QDR II+, RLDRAM 2, SDR						

[1] This is the base core logic register count. The ALM can support three registers when used in LUTREG mode, which increases the total register count by an additional 50 percent.

[2] EP4SGX360N has 1,024 18x18 multipliers.

[3] For EP4SGX70D and EP4SGX110D/F devices.

[4] 3.3 V compliant, requires a 3 V power supply.

[5] The total transceiver count is the sum of 8.5 Gbps transceivers plus 6.5 Gbps transceivers.

Stratix IV E FPGA Features

		Maximum Resource Count for Stratix IV E FPGAs (0.9 V)			
		EP4SE230	**EP4SE360**	**EP4SE530**	**EP4SE820**
Resources	ALMs	91,200	141,440	212,480	325,220
	LEs (K)	228	354	531	813
	Registers[1]	182,400	282,880	424,960	650,440
	M9K memory blocks	1,235	1,248	1,280	1,610
	M144K memory blocks	22	48	64	60
	MLAB memory (Kb)	2,850	4,420	6,640	10,163
	Embedded memory (Kb)	14,283	18,144	20,736	23,130
	18 x 18 multipliers	1,288	1,040	1,024	960
Architectural Features	Global clock networks	16			
	Regional clock networks	64	88	88	88
	Periphery clock networks	88	88	112	132
	PLLs	4	12	12	12
	Design security	✓			
	Others	Programmable Power Technology			
I/O Features	I/O voltage levels supported (V)	1.2, 1.5, 1.8, 2.5, 3.3[2]			
	I/O standards supported	LVTTL, LVCMOS, PCI, PCI-X, LVDS, mini-LVDS, RSDS, LVPECL, Differential SSTL-15, Differential SSTL-18, Differential SSTL-2, Differential HSTL-12, Differential HSTL-15, Differential HSTL-18, SSTL-15 (I and II), SSTL-18 (I and II), SSTL-2 (I and II), 1.2 V HSTL (I and II), 1.5 V HSTL (I and II), 1.8 V HSTL (I and II)			
	Emulated LVDS channels, 1,100 Mbps	128	256	256	288
	LVDS channels, 1,600 Mbps (receive/transmit)	56/56	88/88	112/112	132/132
	Embedded DPA circuitry	✓			
	OCT	Series, parallel, and differential			
	Memory devices supported	DDR3, DDR2, DDR, QDR II, QDR II+, RLDRAM 2, SDR			

[1] This is the base core logic register count. The ALM can support three registers when used in LUTREG mode, which can increase the total register count by an additional 50 percent.
[2] 3.3 V compliant, requires a 3 V power supply.

Stratix IV FPGA Series Package and I/O Matrices

		FBGA (F)[1]					
		780 pin 29 x 29 (mm) 1.0-mm pitch	**1,152 pin** 35 x 35 (mm) 1.0-mm pitch	**1,152 pin** 35 x 35 (mm) 1.0-mm pitch	**1,517 pin** 40 x 40 (mm) 1.0-mm pitch	**1,760 pin** 42.5 x 42.5 (mm) 1.0-mm pitch	**1,932 pin** 45 x 45 (mm) 1.0-mm pitch
Stratix IV GT FPGAs (0.95V)	**EP4S40G2**				646 12+12+12		
	EP4S40G5				646[4] 12+12+12		
	EP4S100G2				646 24+0+12		
	EP4S100G3						769 24+8+16
	EP4S100G4						769 24+8+16
	EP4S100G5				646[4] 24+0+12		769 32+0+16
Stratix IV GX FPGAs (0.9 V)[2]	**EP4SGX70**	368 8+0		480 16+8			
	EP4SGX110	368 8+0	368 16+0	480 16+8			
	EP4SGX180	368 8+0	560 16+0	560 16+8	736 24+12		
	EP4SGX230	368 8+0	560 16+0	560 16+8	736 24+12		
	EP4SGX290	288[3] 16+0	560 16+0	560 16+8	736 24+12	864 24+12	904 32+16
	EP4SGX360	288[3] 16+0	560 16+0	560 16+8	736 24+12	864 24+12	904 32+16
	EP4SGX530			560[4] 16+8	736[4] 24+12	864 24+12	904 32+16
Stratix IV E FPGAs	**EP4SE820**		736[4]		960[4]	1,104	
	EP4SE530		736[4]		960[4]	960	
	EP4SE360	480[2]	736				
	EP4SE230	480					

[1] FineLine ball grid array.

[2] I/O count does not include dedicated clock inputs that can be used as data inputs.

[3] Hybrid package (flip chip) FBGA: 35 x 35 (mm) 1.0-mm pitch.

[4] Hybrid package (flip chip) FBGA: 42.5 x 42.5 (mm) 1.0-mm pitch.

636 (12+12+12) Values on top indicate available user I/O pins; values on bottom indicate the 11.3 Gbps plus 8.5 Gbps plus 6.5 Gbps transceiver count.

636 (8+0) Values on top indicate available user I/O pins; values at the bottom indicate the 8.5 Gbps plus 6.5 Gbps transceiver count.

288 Number indicates available user I/O pins.

Vertical migration (same V_{CC}, GND, ISP, and input pins). For vertical migration, the number of user I/Os may be less than the number stated in the table.

Stratix series devices are offered in commercial and industrial temperatures and RoHS-compliant packages. Stratix IV GT devices are only offered in industrial temperatures (0°C to 100°C).

Arria II GZ FPGA Features

		Maximum Resource Count for Arria II GZ FPGAs (0.9 V)		
		EP2AGZ225	EP2AGZ300	EP2AGZ350
Resources	ALMs	89,600	119,200	139,400
	LEs (K)	224	298	349
	Registers	179,200	238,400	278,800
	M9K memory blocks	1,235	1,248	1,248
	M144K memory blocks	0	24	36
	MLAB memory (Kb)	2,850	4,420	4,420
	Embedded memory (Kb)	11,115	14,688	16,416
	18 x 18 multipliers	800	920	1,040
Architectural Features	Global clock networks	16		
	Regional clock networks	64	88	88
	Periphery clock networks	88		
	PLLs	8	8	8
	Design security	✓		
I/O Features	I/O voltage levels supported (V)	1.2, 1.5, 1.8, 2.5, 3.0		
	I/O standards supported	LVTTL, LVCMOS, PCI, PCI-X, LVDS, mini-LVDS, RSDS, LVPECL, Differential SSTL-15, Differential SSTL-18, Differential SSTL-2, Differential HSTL-12, Differential HSTL-15 (I and II), Differential HSTL-18, SSTL-15 (I and II), SSTL-18 (I and II), 1.2 V HSTL (I and II), SSTL-2 (I and II), 1.5 V HSTL (I and II), 1.8 V HSTL (I and II)		
	Emulated LVDS channels, 1,152 Mbps	184	184	184
	LVDS channels, 1,250 Mbps (receive/transmit)	Up to 86		
	Embedded DPA circuitry	✓		
	OCT	Series and differential		
	Transceiver count (6.375 Gbps)	Up to 24		
	PCIe hard IP blocks (value as 1.1, 2.0, etc)	1		
External Memory Interfaces	Memory devices supported	DDR3, DDR2, DDR, QDR II, RLDRAM 2, SDR		

Arria II GX FPGA Features

		Maximum Resource Count for Arria II GX FPGAs (0.9 V)					
		EP2AGX45	**EP2AGX65**	**EP2AGX95**	**EP2AGX125**	**EP2AGX190**	**EP2AGX260**
Resources	ALMs	18,050	25,300	37,470	49,640	76,120	102,600
	LEs (K)	43	60	89	118	118	244
	Registers[1]	36,100	50,600	74,940	99,280	152,240	205,200
	M9K memory blocks	319	495	612	730	840	950
	MLAB memory (Kb)	564	791	1,171	1,551	2,379	3,206
	Embedded memory (Kb)	2,871	4,455	5,508	6,570	7,560	8,550
	18 x 18 multipliers	232	312	448	576	656	736
Architectural Features	Global clock networks	16					
	Regional clock networks	48					
	Periphery clock networks	50	50	59	59	84	84
	PLLs	4	4	6	6	6	6
	Design security	✓					
	Others	Plug & Play Signal Integrity					
I/O Features	I/O voltage levels supported (V)	1.2, 1.5, 1.8, 2.5, 3.0, 3.3					
	I/O standards supported	LVTTL, LVCMOS, PCI, PCI-X, LVDS, mini-LVDS, RSDS, LVPECL, BLVDS, Differential SSTL-18, Differential SSTL-15, Differential SSTL-2, Differential HSTL-18, Differential HSTL-12, Differential HSTL-15, SSTL-18 (I and II), SSTL-15 (I), SSTL-2 (I and II), 1.8 V HSTL (I and II), 1.5 V HSTL (I and II), 1.2 V HSTL (I and II)					
	Emulated LVDS channels, 945 Mbps	56	56	64	64	96	96
	LVDS channels, 1,250 Mbps (receive/transmit)	85/84	85/84	105/104	105/104	145/144	145/144
	Embedded DPA circuitry	✓					
	OCT	Series and differential					
	Transceiver count (6.375 Gbps)	8	8	12	12	16	16
	PCIe hard IP block (Gen1)	1					
External Memory Interfaces	Memory devices supported	DDR3, DDR2, DDR, QDR II					

[1] This is the base core logic register count. The ALM can support three registers when used in LUTREG mode, which increases total register count by an additional 50 percent.

Arria II GZ and GX FPGA Series Package and I/O Matrices

	Arria II GX FPGAs (0.9 V)			
	UBGA (U)[1]	FBGA (F)		
	358 pin 17 x 17 (mm) 0.8-mm pitch	**572 pin** 25 x 25 (mm) 1.0-mm pitch	**780 pin** 29 x 29 (mm) 1.0-mm pitch	**1,152 pin** 35 x 35 (mm) 1.0-mm pitch
EP2AGX45	156 4	252 8	364 8	
EP2AGX65	156 4	252 8	364 8	
EP2AGX95		260 8	372 12	452 12
EP2AGX125		260 8	372 12	452 12
EP2AGX190			372 12	612 16
EP2AGX260			372 12	612 16

[1]Ultra FineLine ball grid array.

726 / 24 Values on top indicate available user I/O pins; values at the bottom indicate the 6.375 Gbps transceiver count.

Vertical migration (same V_{CC}, GND, ISP, and input pins). For vertical migration, the number of user I/Os may be less than the number stated in the table.

	Arria II GZ FPGAs (0.9 V)		
	Hybrid FBGA (H)	FBGA (F)	
	780 pin 33 x 33 (mm) 1.0-mm pitch	**1,152 pin** 35 x 35 (mm) 1.0-mm pitch	**1,517 pin** 40 x 40 (mm) 1.0-mm pitch
EP2AGZ225		554 16	734 24
EP2AGZ300	281 16	554 16	734 24
EP2AGZ350	281 16	554 16	734 24

636 / 12 Values on top indicate available user I/O pins; values at the bottom indicate the 6.375 Gbps transceiver count.

Vertical migration (same V_{CC}, GND, ISP, and input pins). For vertical migration, the number of user I/Os may be less than the number stated in the table.

Cyclone IV GX FPGA Features

		Maximum Resource Count for Cyclone IV GX FPGAs (1.2 V)						
		EP4CGX15	EP4CGX22	EP4CGX30	EP4CGX50	EP4CGX75	EP4CGX110	EP4CGX150
Resources	LEs (K)	14	21	29	50	74	109	150
	M9K memory blocks	60	84	120	278	462	666	720
	Embedded memory (Kb)	540	756	1,080	2,502	4,158	5,490	6,480
	18 x 18 multipliers	0	40	80	140	198	280	360
Architectural Features	Global clock networks	20	20	20	30	30	30	30
	PLLs	3	4	4	8	8	8	8
I/O Features	I/O voltage levels supported (V)	1.2, 1.5, 1.8, 2.5, 3.3						
	I/O standards supported	LVTTL, LVCMOS, PCI, PCI-X, LVDS, mini-LVDS, RSDS, LVPECL, Differential SSTL-15, Differential SSTL-18, Differential SSTL-2, Differential HSTL-12, Differential HSTL-15, Differential HSTL-18, SSTL-15 (I and II), SSTL-18 (I and II), SSTL-2 (I and II), 1.2 V HSTL (I and II), 1.5 V HSTL (I and II), 1.8 V HSTL (I and II)						
	Emulated LVDS channels	9	40	40	73	73	139	139
	LVDS channels, 840 Mbps (receive/transmit)	7/7	14/14	14/14	49/49	49/49	59/59	59/59
	Transceiver count[1] (2.5 Gbps/3.125 Gbps)	2/0	2, 0 / 4, 0	4, 0 / 0, 4[2]	0, 8	0, 8	0, 8	0, 8
	PCIe hard IP blocks (Gen1)	1						
External Memory Interfaces	Memory devices supported	DDR2, DDR, SDR						

[1] Transceiver performance varies by product line and package offering.
[2] EP4CGX30 supports 3.125 Gbps only in F484 package option.

Cyclone IV E FPGA Features

		Maximum Resource Count for Cyclone IV E FPGAs								
		EP4CE6	**EP4CE10**	**EP4CE15**	**EP4CE22**	**EP4CE30**	**EP4CE40**	**EP4CE55**	**EP4CE75**	**EP4CE115**
Resources	LEs (K)	6	10	15	22	29	40	56	75	114
	M9K memory blocks	30	46	56	66	66	126	260	305	432
	Embedded memory (Kb)	270	414	504	594	594	1,134	2,340	2,745	3,888
	18 x 18 multipliers	15	23	56	66	66	116	154	200	266
Architectural Features	Global clock networks	10	10	20	20	20	20	20	20	20
	PLLs	2	2	4	4	4	4	4	4	4
I/O Features	I/O voltage levels supported (V)	1.2, 1.5, 1.8, 2.5, 3.3								
	I/O standards supported	LVTTL, LVCMOS, PCI, PCI-X, LVDS, mini-LVDS, RSDS, LVPECL, Differential SSTL-15, Differential SSTL-18, Differential SSTL-2, Differential HSTL-12, Differential HSTL-15, Differential HSTL-18, SSTL-15 (I and II), SSTL-18 (I and II), SSTL-2 (I and II), 1.2 V HSTL (I and II), 1.5 V HSTL (I and II), 1.8 V HSTL (I and II)								
	LVDS channels	66	66	137	52	224	224	160	178	230
External Memory Interfaces	Memory devices supported	DDR2, DDR, SDR								

Cyclone IV GX and E FPGA Series Package and I/O Matrices

	Cyclone IV GX FPGAs (1.2 V)					
	QFN (N)[1]	FBGA (F)				
	148 pin 11 x 11 (mm) 0.5-mm pitch	**169 v pin** 14 x 14 (mm) 1.0-mm pitch	**324 pin** 19 x 19 (mm) 1.0-mm pitch	**484 pin** 23 x 23 (mm) 1.0-mm pitch	**672 pin** 27 x 27 (mm) 1.0-mm pitch	**896 pin** 31 x 31 (mm) 1.0-mm pitch
EP4CGX15	72 2	72 2				
EP4CGX22		72 2	150 4			
EP4CGX30		72 2	150 4	290 4		
EP4CGX50				290 4	310 8	
EP4CGX75				290 4	310 8	
EP4CGX110				270 4	393 8	475 8
EP4CGX150				270 4	393 8	475 8

[1] Quad flat pack no lead.

636 / 12 — Values on top indicate available user I/O pins; values at the bottom indicate the 2.5 Gbps or 3.125 Gbps transceiver count.

Vertical migration (same V_{CC}, GND, ISP, and input pins). For vertical migration, the number of user I/Os may be less than the number stated in the table.

	Cyclone IV E FPGAs (1.0 V and 1.2 V)							
	EQFP (E)[1]	FBGA (F)				MBGA (M)	UBGA (U)	
	144 pin 22 x 22 (mm) 0.5-mm pitch	**256 pin** 17 x 17 (mm) 1.0-mm pitch	**324 pin** 19 x 19 (mm) 1.0-mm pitch	**484 pin** 23 x 23 (mm) 1.0-mm pitch	**780 pin** 29 x 29 (mm) 1.0-mm pitch	**164 pin** 8 x 8 (mm) 0.5-mm pitch	**256 pin** 14 x 14 (mm) 0.8-mm pitch	**484 pin** 19 x 19 (mm) 0.8-mm pitch
EP4CE6	91	179					179	
EP4CE10	91	179					179	
EP4CE15	81	165		343		74	165	
EP4CE22	79	153					153	
EP4CE30			193	328	532			
EP4CE40			193	328	532			328
EP4CE55				324	374			324
EP4CE75				292	426			292
EP4CE115				280	528			

[1] Enhanced thin quad flat pack.

636 — Number indicates available user I/O pins.

Vertical migration (same V_{CC}, GND, ISP, and input pins). For vertical migration, the number of user I/Os may be less than the number stated in the table.

Cyclone III FPGA Features

		Maximum Resource Count for Cyclone III FPGAs (1.2 V)							
		EP3C5	**EP3C10**	**EP3C16**	**EP3C25**	**EP3C40**	**EP3C55**	**EP3C80**	**EP3C120**
Resources	LEs (K)	5	10	15	25	40	56	81	119
	M9K memory blocks	46	46	56	66	126	260	305	432
	Embedded memory (Kb)	414	414	504	594	1,134	2,340	2,745	3,888
	18 x 18 multipliers	23	23	56	66	126	156	244	288
Architectural Features	Global clock networks	10	10	20	20	20	20	20	20
	PLLs	2	2	4	4	4	4	4	4
	Design security	–							
I/O Features	I/O voltage levels supported (V)	1.2, 1.5, 1.8, 2.5, 3.3							
	I/O standards supported	LVDS, LVPECL, Differential SSTL-18, Differential SSTL-2, Differential HSTL, SSTL-18 (I and II), SSTL-2 (I and II), 1.5 V HSTL (I and II), 1.8 V HSTL (I and II), PCI, PCI-X 1.0, LVTTL, LVCMOS							
	Emulated LVDS channels, 840 Mbps	66	66	136	79	223	159	177	229
	OCT	Series and differential							
External Memory Interfaces	Memory device supported	DDR2, DDR, SDR							

Cyclone III LS FPGA Features

		Maximum Resource Count for Cyclone III LS FPGAs (1.2 V)			
		EP3CLS70	**EP3CLS100**	**EP3CLS150**	**EP3CLS200**
Resources	LEs (K)	70	100	151	198
	M9K memory blocks	333	483	666	891
	Embedded memory (Kb)	2,997	4,347	5,994	8,019
	18 x 18 multipliers	200	276	320	396
Architectural Features	Global clock networks	20			
	PLLs	4			
	Design security	✓			
I/O Features	I/O voltage levels supported (V)	1.2, 1.5, 1.8, 2.5, 3.3			
	I/O standards supported	LVDS, LVPECL, Differential SSTL-18, Differential SSTL-2, Differential HSTL, SSTL-18 (I and II), SSTL-2 (I and II), 1.5 V HSTL (I and II), 1.8 V HSTL (I and II), PCI, PCI-X 1.0, LVTTL, LVCMOS			
	LVDS channels, 840 Mbps	169			
	OCT	Series and differential			
External Memory Interfaces	Memory device supported	DDR2, DDR, SDR			

Cyclone III Series Package and I/O Matrices

	Cyclone III FPGAs (1.2 V)								
	EQFP (E)	MBGA (M)[1]	PQFP (Q)[2]	FBGA (F)				UBGA (U)	
	144 pin 22 x 22 (mm) 0.5-mm pitch	**164 pin** 8 x 8 (mm) 0.5-mm pitch	**240 pin** 34.6 x 34.6 (mm) 0.5-mm pitch	**256 pin** 17 x 17 (mm) 1.0-mm pitch	**324 pin** 19 x 19 (mm) 1.0-mm pitch	**484 pin** 23 x 23 (mm) 1.0-mm pitch	**780 pin** 29 x 29 (mm) 1.0-mm pitch	**256 pin** 14 x 14 (mm) 0.8-mm pitch	**484 pin** 19 x 19 (mm) 0.8-mm pitch
EP3C5	94	106		182				182	
EP3C10	94	106		182				182	
EP3C16	84	92	160	168		346		168	346
EP3C25	82		148	156	215			156	
EP3C40			128		196	331	535		331
EP3C55						327	377		327
EP3C80						295	429		295
EP3C120						283	531		
EP3CLS70						294	429		294
EP3CLS100						294	429		294
EP3CLS150						226	429		
EP3CLS200						226	429		

[1] Micro FineLine BGA.
[2] Plastic quad flat pack.

636 Number indicates available user I/O pins.

Vertical migration (same V_{CC}, GND, ISP, and input pins). For vertical migration, the number of user I/Os may be less than the number stated in the table.

MAX 10 FPGA Features

Altera's new MAX 10 FPGAs revolutionize non-volatile integration by delivering advanced processing capabilities in a low-cost, instant-on, small form factor programmable logic device.

The MAX 10 FPGAs are built on TSMC's 55 nm flash technology enabling instant-on configuration so you can quickly control power-up or initialization of other components in the system. The devices also include full-featured FPGA capabilities, such as DSP , analog functionality, Nios II embedded processor support, and memory controllers.

By integrating new features within a robust set of FPGA capabilities, the MAX 10 FPGAs are optimized for a wide range of high-volume, cost-sensitive applications, including:

Automotive

- Built on TSMC's 55 nm high-volume flash process tailored for the automotive industry's rigorous safety and quality requirements
- Integrated flash provides instant-on behavior for applications requiring fast boot times such as rear-view cameras in Advanced Driver Assistance Systems (ADAS) and infotainment displays
- FPGA-class signal processing acceleration for electric vehicle (EV) applications, such as motor control, battery management, and power conversion

Industrial

- Reduced footprint, increased design security and reliability, while lowering system cost
- Accurate environmental condition sensing and efficient real-time controls for motor control, I/O modules, and Internet of Things (IoT) applications
- Single chip support for multiple Industrial Ethernet protocols and machine-to-machine (M2M) communication

Communications

- Analog functionality for sensing board environment allows integration of power-up sequencing and system-monitoring circuitry into a single device
- High I/O count and software-based system management using the Nios II soft processor enable board management integration in an advanced, reliable single-chip system controller

MAX V CPLD Features

		MAX V CPLDs (1.8 V)						
		5M40Z	5M80Z	5M160Z	5M240Z	5M570Z	5M1270Z	5M2210Z
Density and Speed	LEs	40	80	160	240	570	1270	2210
	Equivalent macrocells[1]	32	64	128	192	440	980	1700
	Pin-to-pin delay (ns)	7.5	7.5	7.5	7.5	9.0	6.2	7.0
	User flash memory (Kb)	8						
	Total on-chip memory (bits)[2]	Yes	Yes	Yes	Yes	Yes	Yes	Yes
Architectural Features	Internal oscillator	✓						
	Digital PLL[3]	✓						
	Fast power on reset	✓						
	Boundary scan JTAG	✓						
	JTAG ISP	✓						
	Fast input registers	✓						
	Programmable register power up	✓						
	JTAG translator	✓						
	Real-time ISP	✓						
I/O Features	Multivolt I/Os (V)	1.2, 1.5, 1.8, 2.5, 3.3					1.2, 1.5, 1.8, 2.5, 3.3, 5.0[4]	
	I/O power banks	2	2	2	2	2	4	4
	Maximum output enables	54	54	79	114	159	271	271
	LVTTL/LVCMOS	✓						
	LVDS outputs	Yes	Yes	Yes	Yes	Yes	Yes	Yes
	32 bit, 66 MHz PCI compliant	-	-	-	-	-	✓[4]	✓[4]
	Schmitt triggers	✓						
	Programmable slew rate	✓						
	Programmable pull-up resistors	✓						
	Programmable ground pins	✓						
	Open-drain outputs	✓						
	Bus hold	✓						

[1] Typical equivalent macrocells.

[2] Unused LEs can be converted to memory. The total number of available LE RAM bits depends on the memory mode, depth, and width configurations of the instantiated memory.

[3] Optional IP core. Contact your Altera sales representative for availability.

[4] An external resistor must be used for 5 V tolerance.

MAX II CPLD Features

		MAX II CPLDs (3.3 V, 2.5 V, 1.8 V)			
		EPM240/Z	EPM570/Z	EPM1270	EPM2210
Density and Speed	Equivalent macrocells[1]	192	440	980	1,700
	Pin-to-pin delay (ns)	4.7, 7.5	5.4, 9.0	6.2	7.0
Architectural Features	User flash memory (Kb)	8			
	Boundary scan JTAG	✓			
	JTAG ISP	✓			
	Fast input registers	✓			
	Programmable register power up	✓			
	JTAG translator	✓			
	Real-time ISP	✓			
I/O Features	Multivolt I/Os (V)	1.5, 1.8, 2.5, 3.3	1.5, 1.8, 2.5, 3.3	1.5, 1.8, 2.5, 3.3, 5.0[2]	1.5, 1.8, 2.5, 3.3, 5.0[2]
	I/O power banks	2	2	4	4
	Maximum output enables	80	160	212	272
	LVTTL/LVCMOS	✓			
	32 bit, 66 MHz PCI compliant	-	-	✓[2]	✓[2]
	Schmitt triggers	✓			
	Programmable slew rate	✓			
	Programmable pull-up resistors	✓			
	Programmable ground pins	✓			
	Open-drain outputs	✓			
	Bus hold	✓			

[1] Typical equivalent macrocells.

[2] An external resistor must be used for 5 V tolerance.

MAX V and MAX II CPLD Series Package and I/O Matrices

	MAX V CPLDs (1.8 V)[1]							
	EQFP (E)[2]	TQFP (T)[3]		MBGA (M)[4]			FBGA (F)	
	64 pin 7 x 7 (mm) 0.4-mm pitch	100 pin 14 x 14 (mm) 0.5-mm pitch	144 pin 20 x 20 (mm) 0.5-mm pitch	64 pin 4.5 x 4.5 (mm) 0.5-mm pitch	68 pin 5 x 5 (mm) 0.5-mm pitch	100 pin 6 x 6 (mm) 0.5-mm pitch	256 pin 17 x 17 (mm) 1.0-mm pitch	324 pin 19 x 19 (mm) 1.0-mm pitch
5M40Z	54			30				
5M80Z	54	79		30	52			
5M160Z	54	79			52	79		
5M240Z		79	114		52	79		
5M570Z		74	114			74	159	
5M1270Z			114				211	271
5M2210Z							203	271

	MAX II CPLDs (3.3 V, 2.5 V, 1.8 V)[1]								
	TQFP (T)		FBGA (F)			MBGA (M)			
	100 pin 16 x 16 (mm) 0.5-mm pitch	144 pin 22 x 22 (mm) 0.5-mm pitch	100 pin 11 x 11 (mm) 1.0-mm pitch	256 pin 17 x 17 (mm) 1.0-mm pitch	324 pin 19 x 19 (mm) 1.0-mm pitch	68 pin 5 x 5 (mm) 0.5-mm pitch	100 pin 6 x 6 (mm) 0.5-mm pitch	144 pin 7 x 7 (mm) 0.5-mm pitch	256 pin 11 x 11 (mm) 0.5-mm pitch
EPM240Z						54	80		
EPM570Z							76	116	160
EPM240	80		80				80		
EPM570	76	116	76	160			76		160
EPM1270		116		212					212
EPM2210				204	272				

[1]For temperature grades of specific packages (commercial, industrial, or extended temperatures), refer to Altera's online selector guide.
[2]Enhanced quad flat pack.
[3]Thin quad flat pack.
[4]Micro FineLine BGA (0.5 mm).

636 Number indicates available user I/O pins.

Vertical migration (same V_{CC}, GND, ISP, and input pins). For vertical migration, the number of user I/Os may be less than the number stated in the table.

Enpirion Power DC-DC Converters

Altera develops FPGAs and CPLDs using advanced process technologies that provide fast performance and high logic density. To meet demanding power requirements, Altera's Enpirion products deliver the industry's first family of power system-on-chip (PowerSoC) DC-DC converters featuring integrated inductors. They provide an industry-leading combination of high efficiency, small footprint, and low-noise performance.

Powering Your Innovation — PowerSoC

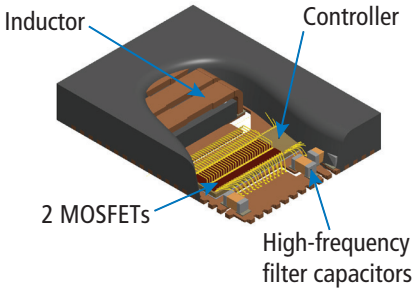
Key Intellectual Property

High-frequency power conversion

Magnetics engineering

Power packaging and construction

Integrated Power Management Systems



Engineered Turnkey Solutions

Fully simulated, characterized, and validated

System-level qualified

Eliminates inductor and capacitor selection

Enpirion Power DC-DC Converters

Benefits of PowerSoC

Addressing today's and tomorrow's system power design challenges:

Highest Power Density and Smallest Footprint

Greatly minimizes the amount of PCB space and height profile required for point-of-load regulation compared to alternative discrete switching regulators and modules.

High Efficiency and Thermal Performance

Optimized with up to 96 percent efficiency. High-efficiency devices are industrial graded, with most products not requiring load de-rating or air flow at 85°C ambient temperature.

Lowest Component Count and Higher Reliability

PowerSoCs are specified, simulated, characterized, validated, and manufacturing-tested as a complete power system. Fewer components and tightly controlled IC manufacturing processes permit an unsurpassed 45,000-year mean time between failures (MTBF) reliability.

Ease of Design and Fastest Time to Market

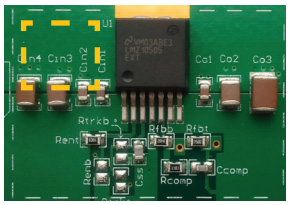
PowerSoCs with integrated inductor and compensation enable turnkey designs. Development requires fewer design steps with significantly less exposure to design iteration versus discrete switching regulators.

Fully Validated Power Solutions

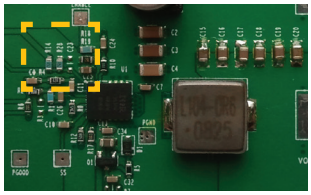
Fully validated PCB layout and design files enable customers nearly 100 percent first-pass success.

PowerSoC Comparison

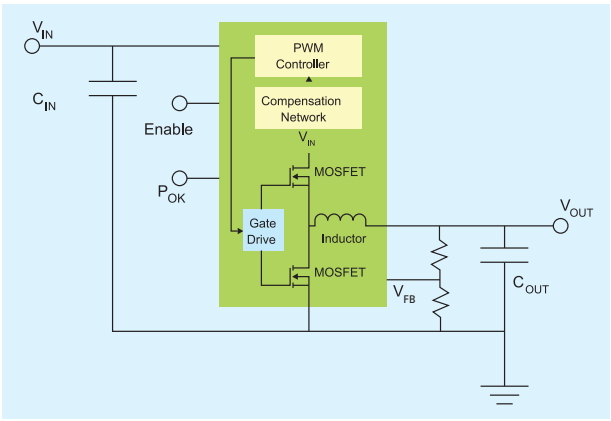
PowerSoC – 25% to 50% smaller footprint than alternative solutions:

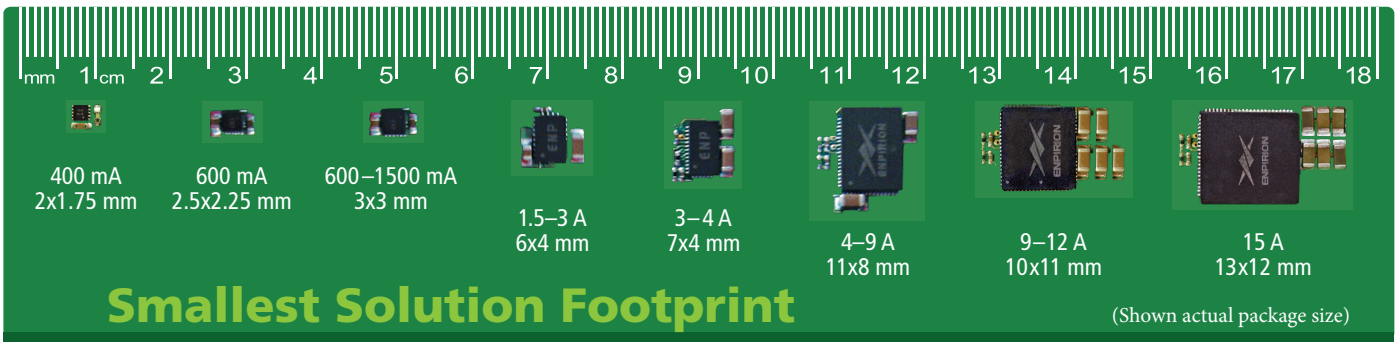


Competitors' Modules



Competitors' Discrete Regulators

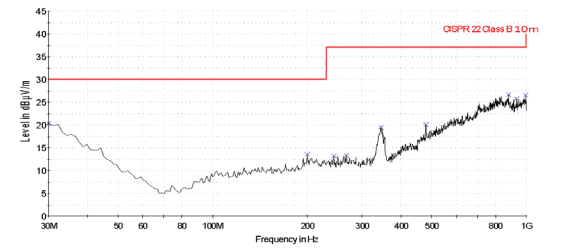




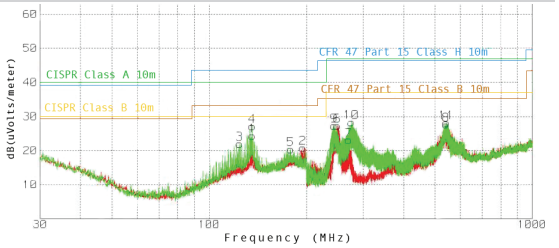
Enpirion Power DC-DC Converters

Low Radiated Noise

Enpirion

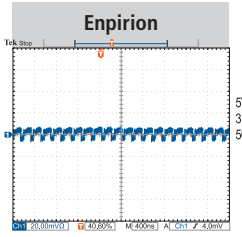


Competitor



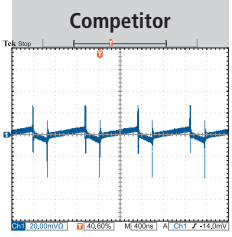
Low Ripple

Enpirion



5V Input
3.3V Output
500 MHz Bandwidth

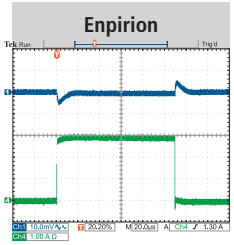
Competitor



5V Input
3.3V Output
500 MHz Bandwidth

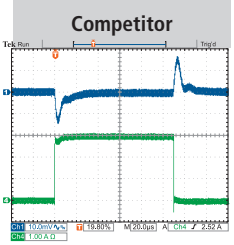
Fast Dynamic Response

Enpirion



5V Input
3.3V Output

Competitor



5V Input
3.3V Output

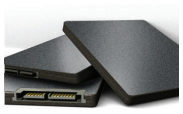
Applications

Market pressures are driving equipment manufacturers to add more features, functionality, and higher bandwidth while moving to smaller form factors and targeting improved energy efficiency. The newest 28 nm and 20 nm FPGAs, processors, and other SoCs address these challenges, in part, by implementing more granular and precise levels of power management. The result is an escalating number of power rails, complex power-up sequencing requirements, and tighter noise tolerances. Enpirion power solutions from Altera meet these power design challenges and are broadly used in many applications.

Computer

Server motherboards
NIC and HBA cards
RAID controllers
Micro servers

Enterprise Storage



Solid State Drives (SSD):
SATA, SAS, mSATA, PCIe
Storage systems

Networking and Telecommunications

Radio basestation (macro, pico, femto)
Backhaul (microwave, wireline)
Media gateway (ATCA/AMC)

Test and Measurement

Network analyzers
Automated test equipment (ATE)
Data acquisition
Scopes, analyzers, signal generators

Industrial and Embedded

Security systems/digital video recorder (DVR)
Industrial computing
Industrial communication modules

Optical Networking

Optical Modules:
SFP, XFP, CXP, CFP
Active optical cable
Reprogrammable add/drop multiplexer

Enpirion Power DC-DC Converters

Featured PowerSoC Products

Part Number	I_{OUT} (A)	V_{IN} (VDC)	V_{OUT} Range (VDC)[1]	Pkg (pins)	Pkg Size (mm) L	W	H	Solution Size (mm^2)	Ext. Components	XFB V Adjust	VID V Adjust	Power Good	Program Soft Start	Margining	Input Sync	Output Sync	Parallel Capability	Light Load Mode
5300 5 V Step-Down Converters																		
EP5348UI	0.4	2.5 – 5.5	0.60 – Note 1	uQFN14	2.0	1.75	0.9	21	6	•								
EP535[x]HUI[2]	0.6	2.4 – 5.5	1.80 – 3.3	uQFN16	2.5	2.25	1.1	14	2		3-pin							•
EP535[x]LUI[2]	0.6	2.4 – 5.5	0.60 – Note 1	uQFN16	2.5	2.25	1.1	14	2	•	3-pin							•
EP53A[x]HQI[2]	1.0	2.4 – 5.5	1.80 – 3.3	QFN16	3.0	3.0	1.1	21	3		3-pin							•
EP53A[x]LQI[2]	1.0	2.4 – 5.5	0.60 – Note 1	QFN16	3.0	3.0	1.1	21	3	•	3-pin							•
EP53F8QI	1.5	2.4 – 5.5	0.60 – Note 1	QFN16	3.0	3.0	1.1	40	8	•		•						
EN5319QI	1.5	2.4 – 5.5	0.60 – Note 1	QFN24	4.0	6.0	1.1	55	6	•		•						
EN5329QI	2.0	2.4 – 5.5	0.60 – Note 1	QFN24	4.0	6.0	1.1	55	6	•		•						
EN5339QI	3.0	2.4 – 5.5	0.60 – Note 1	QFN24	4.0	6.0	1.1	55	7	•		•						
EN5364QI	6.0	2.4 – 6.6	0.60 – Note 1	QFN68	8.0	11.0	1.85	160	6	•		•	•	•	•	•	•	
EN5367QI	6.0	2.5 – 5.5	0.60 – Note 1	QFN54	10.0	5.5	3.0	160	12	•		•	•		•			
EN5394QI	9.0	2.4 – 6.6	0.60 – Note 1	QFN68	8.0	11.0	1.85	190	7	•		•	•	•	•	•	•	
6300 Efficiency-Optimized Step-Down DC-DC Converters																		
EN6310QI	1.0	2.7 – 5.5	0.60 – 3.3	QFN30	4.0	5.0	1.85	65	10	•		•	•					
EN6337QI	3.0	2.5 – 6.6	0.60 – Note 1	QFN38	4.0	7.0	1.85	75	6	•		•	•		•			•
EN6347QI	4.0	2.5 – 6.6	0.60 – Note 1	QFN38	4.0	7.0	1.85	75	6	•		•	•		•			•
EN6360QI	8.0	2.5 – 6.6	0.60 – Note 1	QFN68	8.0	11.0	3.0	190	10	•		•	•		•	•	•	
EN63A0QI	12.0	2.5 – 6.6	0.60 – Note 1	QFN76	10.0	11.0	3.0	225	11	•		•	•		•	•	•	
2300 12 V Step-Down Converters																		
EN2342QI	4.0	4.5 – 14.0	0.75 – 5.0	QFN68	8.0	11.0	3.0	200	15	•		•	•		•	•		
EN2360QI	6.0	4.5 – 14.0	0.75 – 5.0	QFN68	8.0	11.0	3.0	200	13	•		•	•		•	•		
EN2390QI	9.0	4.5 – 14.0	0.75 – 3.3	QFN76	10.0	11.0	3.0	235	17	•		•	•		•	•	•	
EN23F0QI	15.0	4.5 – 14.0	0.75 – 3.3	QFN92	13.0	12.0	3.0	325	19	•		•	•		•	•	•	
EV1300 Source/Sink DDR VTT Converters																		
EV1320QI	2.0	1.0 – 1.8	0.50 – 0.9	QFN16	3.0	3.0	0.55	40	6			•	•				•	
EV1340QI	5.0	1.0 – 1.8	0.50 – 0.9	QFN54	5.5	10.0	3.0	125	14	•		•	•				•	
EV1380QI	8.0	1.16 – 1.8	0.60 – 0.9	QFN68	8.0	11.0	3.0	200	14	•		•	•				•	

Notes

1. Maximum $V_{OUT} = V_{IN} - V_{DROPOUT}$ where $V_{DROPOUT} = R_{DROPOUT}$ x Load Current. Reference device datasheet to calculate $V_{DROPOUT}$. Typical $V_{DROPOUT} = 0.4V$.
2. [x] = "8" for PWM only; "7" for Light Load mode

Definitions

- Qualified to industrial (I) ambient temperature range: -40°C to + 85°C
- VID = Output voltage programming using Voltage ID code pins
- Margining = The ability to force V_{OUT} out of regulation by a selectable percentage (via 2 pins)
- Input/Output Sync = ability to control frequency of the regulator(s) to reduce input/output voltage ripple
- Size estimate for single-sided PCB including all suggested external components

For a complete list of Enpirion power products, please visit www.altera.com/devices/power/power-index.html

Powering Your FPGA Innovation

Featured Products for FPGA Applications

Altera offers a range of verified power solutions that cover FPGA power requirements.

Max I_{LOAD} (A)	Solution	Description	V_{IN} Range (V)	V_{OUT} Range (V)[1]	Core Power[2]	Low Noise[3]
240	ED9603S0xQI and ET4040QI	6-phase digital controller with PMBus and 40A powertrain	4.5 – 14	0.6 – 5.0	•	
160	EC7401QI and ET4040QI	4-phase pulse-width modulation (PWM) controller and 40A powertrain	4.5 – 14	0.6 – 5.0	•	
40	ED8101P0xQI and ET4040QI	Single-phase digital controller with PMBus and 40A powertrain	4.5 – 14	0.6 – 5.0	•	
40	ED8106N0xQI and ET4040QI	Single-phase digital controller and 40A powertrain	4.5 – 14	0.6 – 5.0	•	
15	EN23F0QI	15A PowerSoC, parallel capability	4.5 – 14	0.75 – 3.3	•	•
12	EN63A0QI	High-efficiency 12A PowerSoC, parallel capability	2.5 – 6.6	0.6 – V_{IN} - $V_{DROPOUT}$	•	•
9	EN2390QI	9A PowerSoC, parallel capability	4.5 – 14	0.75 – 3.3	•	•
8	EN6360QI	High-efficiency 8A PowerSoC, parallel capability	2.5 – 6.6	0.6 – V_{IN} - $V_{DROPOUT}$	•	•
6	EN2360QI	6A PowerSoC, pin compatible with EN2342QI	4.5 – 14	0.75 – 5.0	•	•
6	EN5367QI	6A PowerSoC	2.5 – 5.5	0.6 – V_{IN} - $V_{DROPOUT}$		•
4	EN2342QI	4A PowerSoC, pin compatible with EN2362QI	4.5 – 14	0.75 – 5.0	•	•
4	EN6347QI	High-efficiency 4A PowerSoC	2.5 – 6.6	0.6 – V_{IN} - $V_{DROPOUT}$	•	•
3	EN6337QI	High-efficiency 3A PowerSoC	2.5 – 6.6	0.6 – V_{IN} - $V_{DROPOUT}$	•	•
3	EN5339QI	3A PowerSoC; pin compatible with EN5329/19QI	2.4 – 5.5	0.6 – V_{IN} - $V_{DROPOUT}$		•
2	ER2120QI	2A switching regulator with integrated MOSFETs	5.0 – 14	0.6 – 12	•	
2	EN5329QI	2A PowerSoC; pin compatible with EN5339/19QI	2.4 – 5.5	0.6 – V_{IN} - $V_{DROPOUT}$		•
1.5	EN5319QI	1.5A PowerSoC; pin compatible with EN5339/29QI	2.4 – 5.5	0.6 – V_{IN} - $V_{DROPOUT}$		•
1	ER3110DI	1A switching regulator with integrated MOSFETs	3.0 – 36	0.6 – 12	•	
1	EN6310QI	High-efficiency 1A PowerSoC	2.7 – 5.5	0.6 – 3.3	•	•
1	EP53A8xQI	Ultra small 1A PowerSoC	2.4 – 5.5	0.6 – V_{IN} - $V_{DROPOUT}$		•
1	EY1501DI	1A linear regulator	2.2 – 6	0.8 – 5	•	•
0.6	EP5358xQI	Ultra small 0.6A PowerSoC	2.4 – 5.5	0.6 – V_{IN} - $V_{DROPOUT}$		•
0.5	ER3105QI	0.5A switching regulator with integrated MOSFETs	3.0 – 36	0.6 – 34	•	
0.15	EY1603TI	150mA low IQ linear regulator	6.0 – 40	2.5 – 12	•	•
0.05	EY1602SI	50mA low IQ linear regulator	6.0 – 40	2.5 – 12	•	•

Special Function Products

Product	Description
ES1010QI	12V power distribution hot swap controller
ES1022QI	Sequencer with 4 delay adjustable sequenced outputs with input voltage monitoring
ES1020QI	Sequencer with 4 delay adjustable sequenced outputs with input voltage monitoring; supplies gate drive for external FETs
ES1021QI	Sequencer with 4 delay adjustable sequenced outputs with input voltage monitoring; supplies gate drive for external FETs; groups 4 channels into 2 groups each with their own enable

Notes

1. Reference device datasheet for $V_{DROPOUT}$ value
2. Meets accuracy, ripple, and transient requirements for FPGA core rails.
3. Low-output voltage ripple and meets CISPR 22 Class B emissions standard.

Configuration Devices

www.altera.com/literature/lit-config.jsp

The following is an overview of our configuration devices. To determine the right configuration device for your FPGA, check out our Configuration Handbook or the configuration chapter in the handbook of your selected FPGA.

Altera's serial configuration devices store the configuration file for our SRAM-based FPGAs. We designed our serial configuration devices to minimize board space while providing a dedicated FPGA configuration solution. Serial configuration devices are recommended for new designs. For information on additional configuration devices supporting older products, see our Configuration Handbook.

	EPCQ-L Serial Configuration Devices for Arria 10 FPGAs (1.8V)
	FBGA
	24 pin 6 x 8 (mm) 1.0 mm pitch
EPCQL256	256
EPCQL512	512
EPCQL1024	1,024

512 Number indicates memory size in Megabits (Mb)

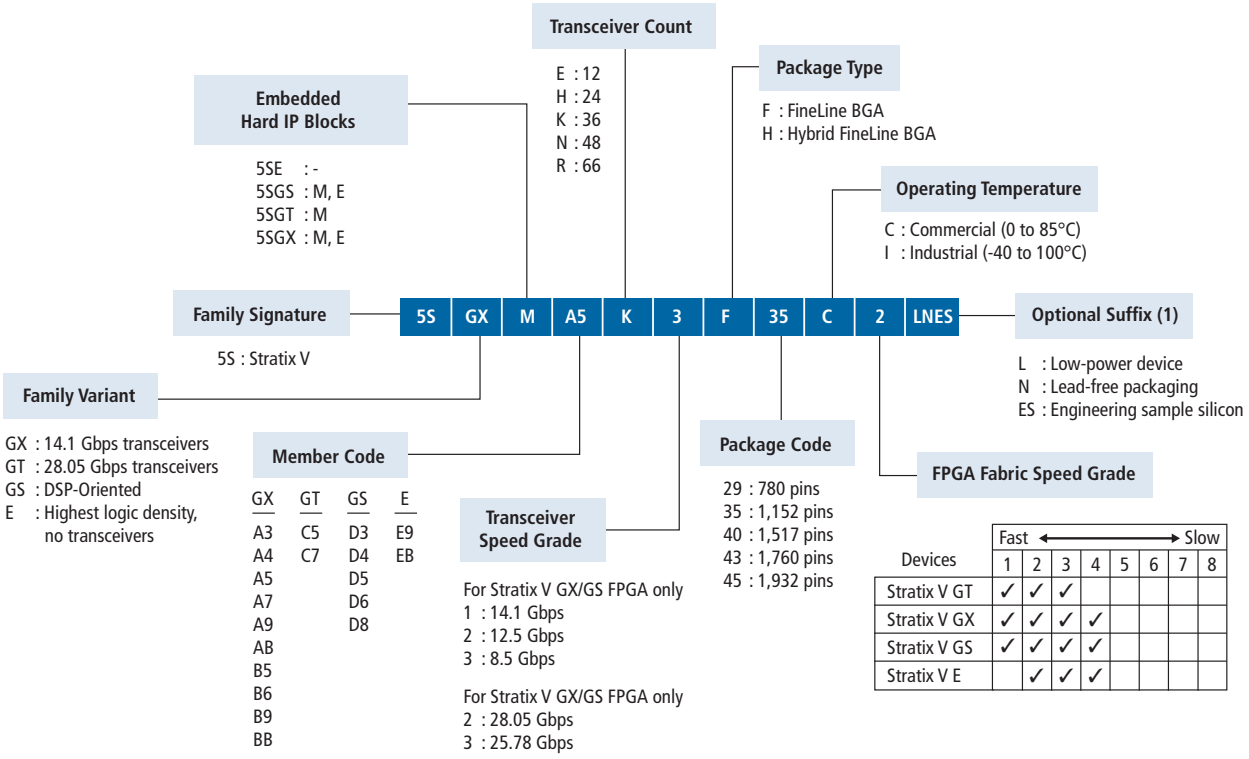
Vertical migration (same Vcc, GND, ISP, and input pins)

	EPCQ Serial Configuration Devices for 28 nm and Prior FPGAs (3.0V-3.3V)	
	SOIC	
	8 pin 4.9 x 6.0 (mm)	**16 pin** 10.3 x 10.3 (mm)
EPCQ16	16	
EPCQ32	32	
EPCQ64		64
EPCQ128		128
EPCQ256		256
EPCQ512		512

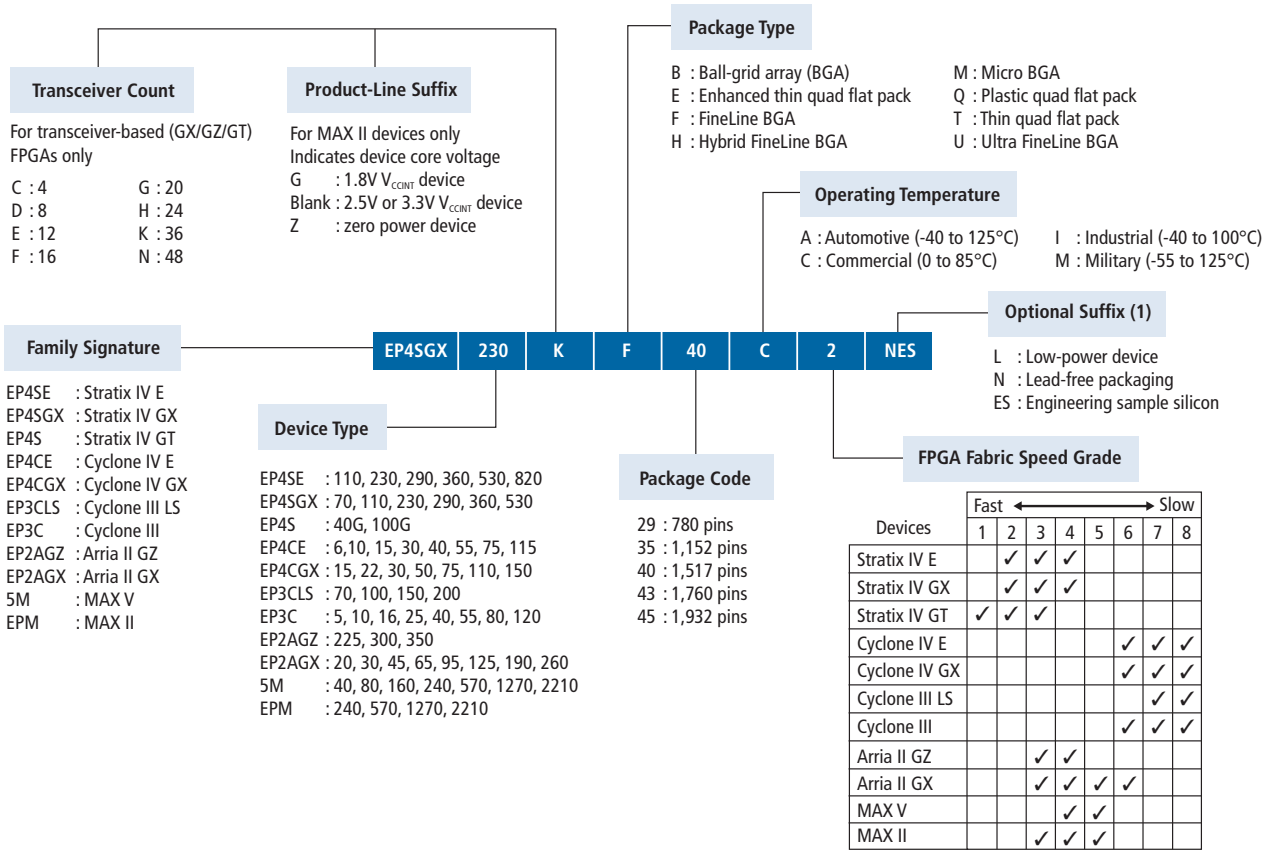
512 Number indicates memory size in Megabits (Mb)

Vertical migration (same Vcc, GND, ISP, and input pins)

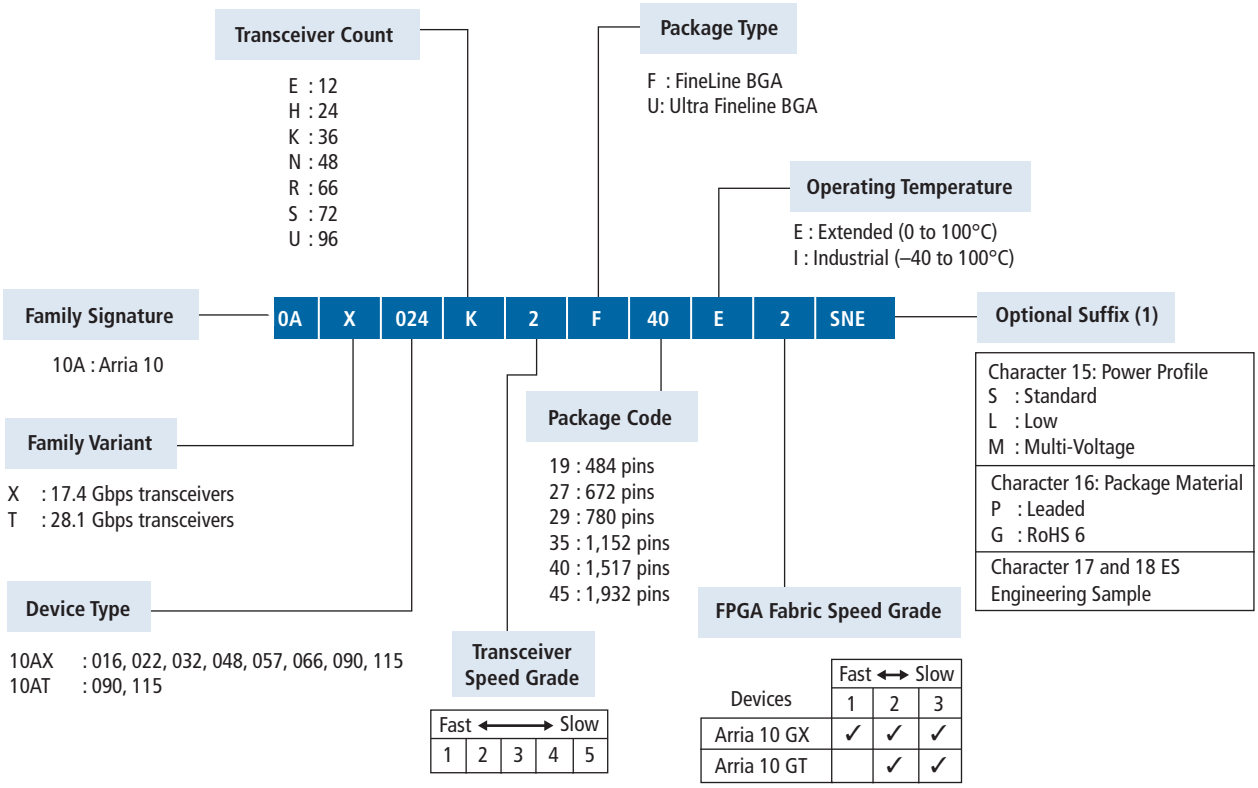
Ordering Information for Stratix V (GT, GX, GS, and E) Devices



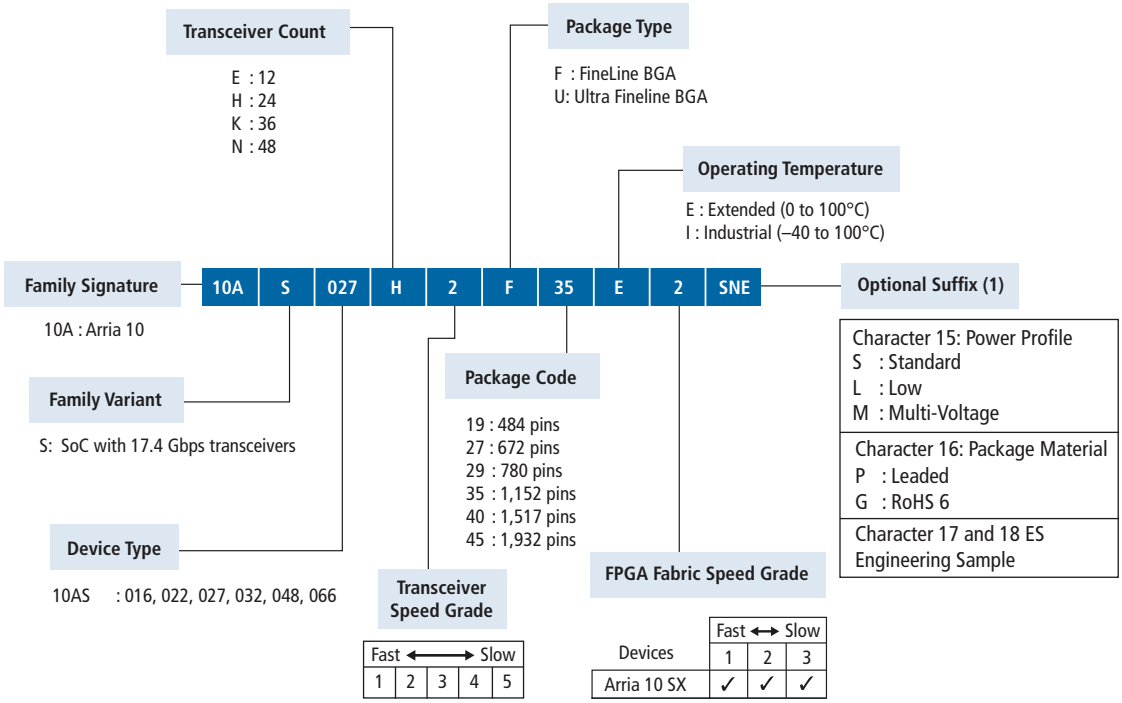
Ordering Information for Stratix IV (E, GX, GT), Cyclone IV (E,GX), Cyclone III, MAX V, and MAX II



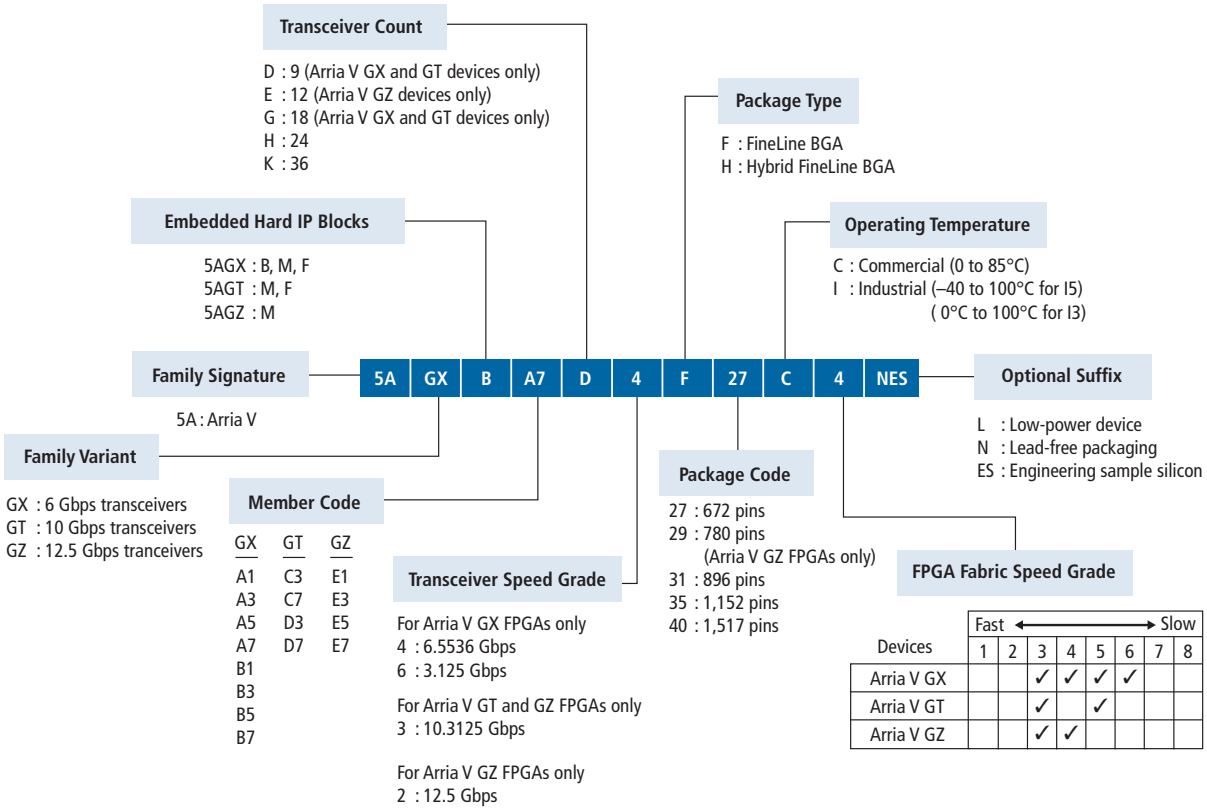
Ordering Information for Arria 10 (GX and GT) Devices



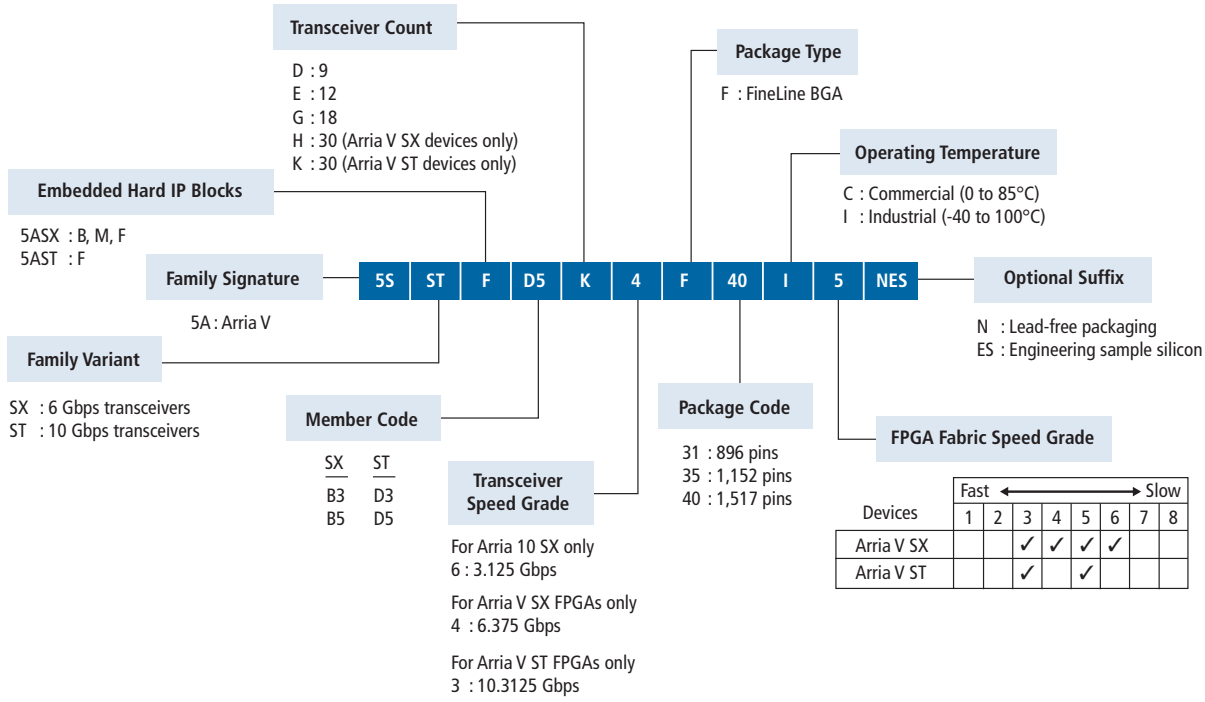
Ordering Information for Arria 10 (SX) SoCs



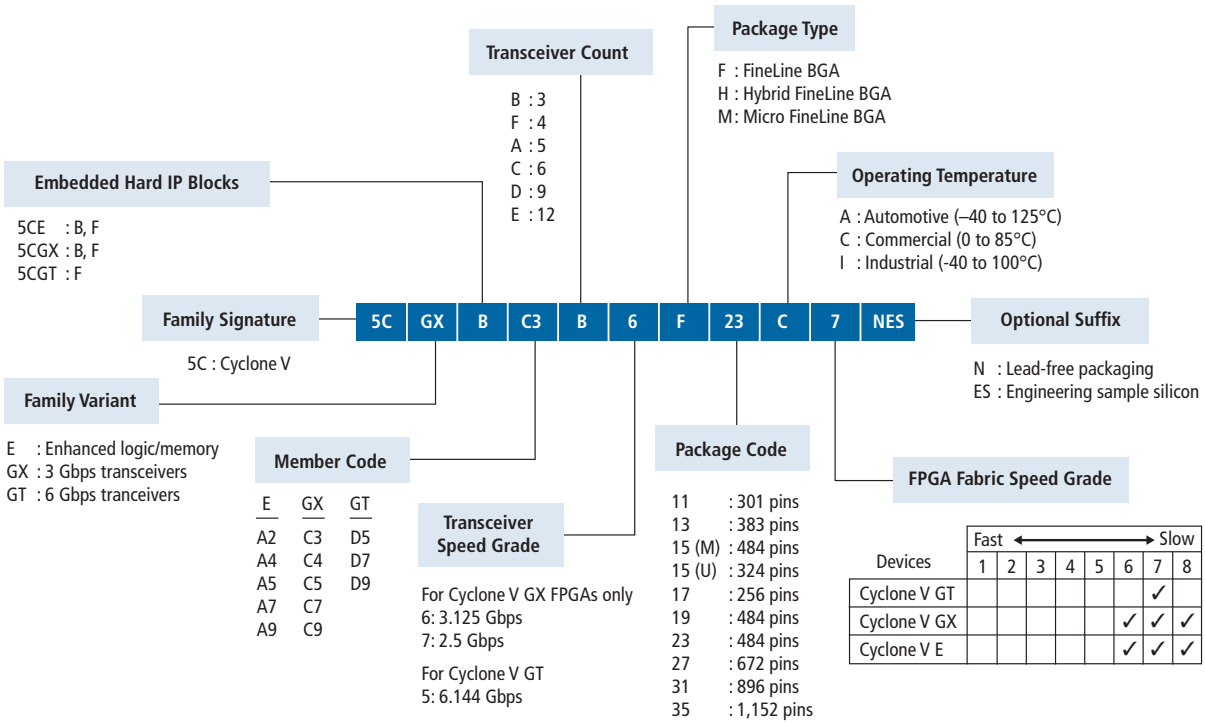
Ordering Information for Arria V (GT, GX, GZ) Devices



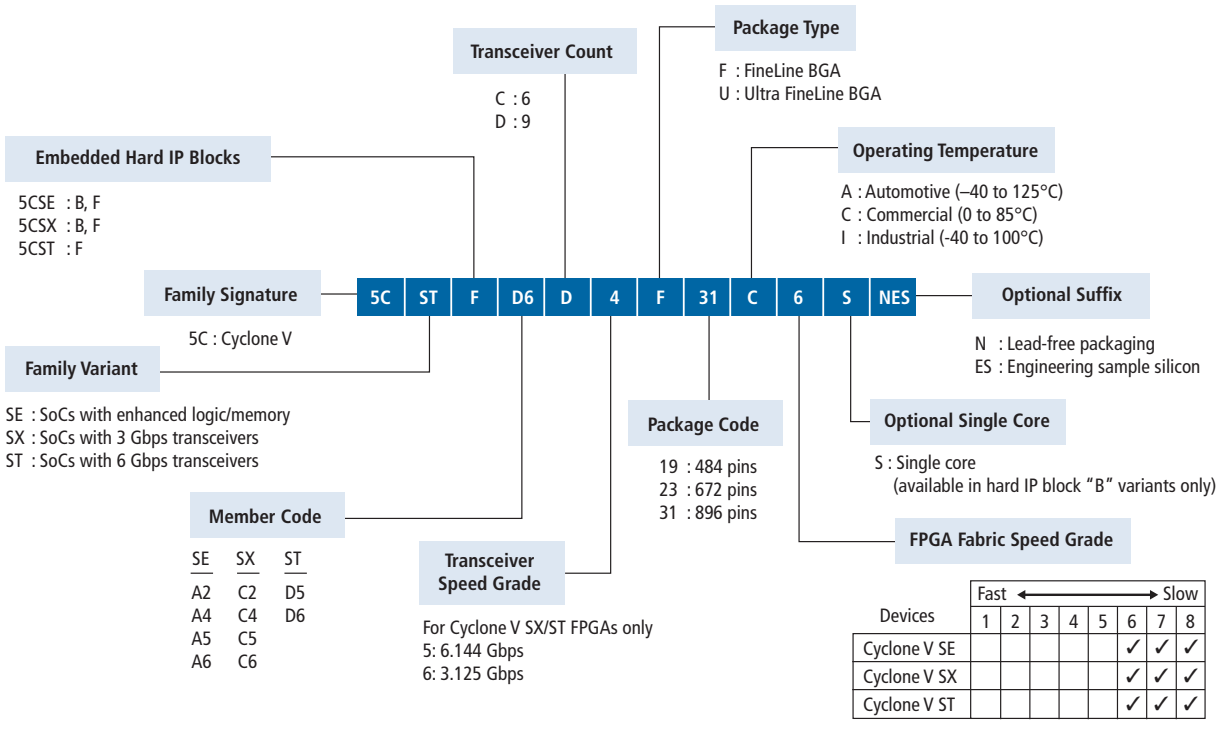
Ordering Information for Arria V (SX, ST) SoCs



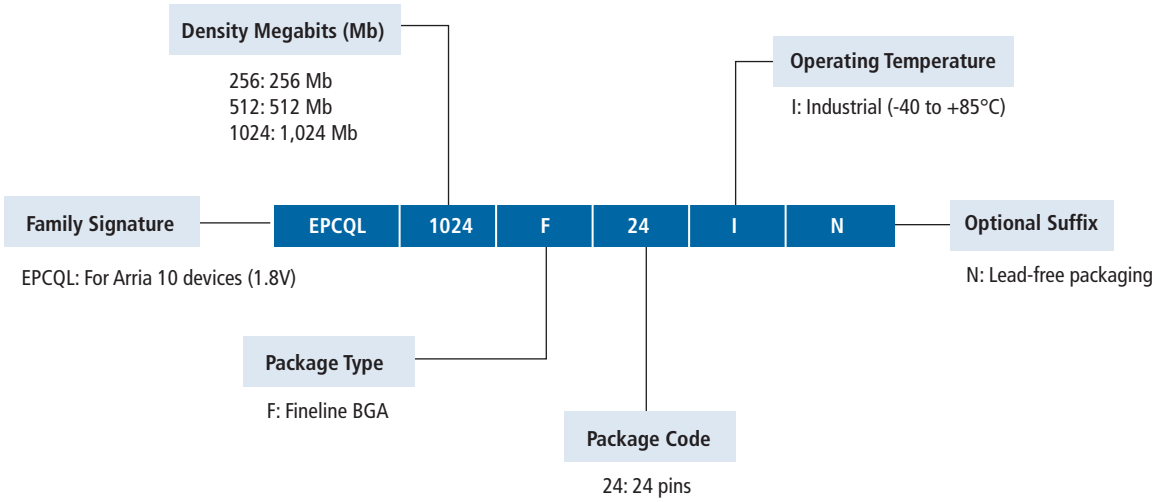
Ordering Information for Cyclone V (E, GX, GT) Devices

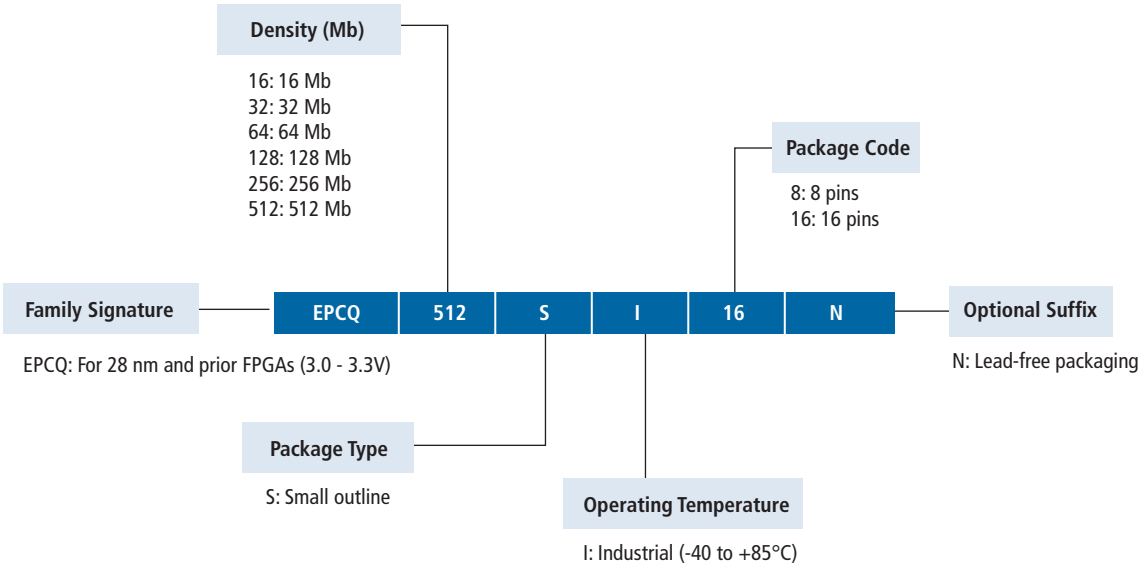


Ordering Information for Cyclone V (SE, SX, ST) SoCs



Ordering Information for Serial Configuration Devices





Quartus II Design Software

www.altera.com/products/software

Quartus II software is number one in performance and productivity for CPLD, FPGA, and SoC designs, providing the fastest path to convert your concept into reality. Quartus II software also supports many third-party tools for synthesis, static timing analysis, board-level simulation, signal integrity analysis, and formal verification.

	Quartus II Software Design Flow		
	Quartus II Software Key Features	Availability	
		Subscription Edition	Web Edition (Free)
Design Entry	Cyclone FPGA and MAX CPLD device support	✓	✓
	Arria and Stratix FPGA device support	✓	✓[1]
	Cyclone and Arria SoC support	✓	✓
	Multiprocessor support (faster compile time support)	✓	✓[2]
	IP base suite (includes licenses for 15 popular IP cores)	✓	Available for purchase
	Qsys (next-generation system–integration tool)	✓	✓
	Rapid Recompile (faster compile for small design changes)	✓	
	Incremental compile (performance preservation and team-based design)	✓	
Functional Simulation	ModelSim®-Altera Starter Edition software	✓	✓
	ModelSim-Altera Edition software	✓[3]	✓[3]
Synthesis	Quartus Integrated Synthesis (synthesis tool)	✓	✓
Placement and Routing	Fitter (placement and routing tool)	✓	✓
Timing and Power Verification	TimeQuest tool (static timing analysis)	✓	✓
	PowerPlay tool and optimization (power analysis)	✓	✓
In-System Debug	SignalTap™ II logic analyzer (embedded logic analyzer)[2]	✓	✓[2]
	Transceiver toolkit (transceiver interface and verification tool)	✓	
	JNEye link analysis tool	✓	
	Operating System (OS) Support	Availability	
		Subscription Edition	Web Edition (Free)
	Windows/Linux 64 bit support	✓	✓

[1] Only Arria II FPGA - EP2AGX45 device is supported
[2] Available with TalkBack feature enabled.
[3] Requires additional license.

Quartus II Design Software

	Quartus II Design Software Features Summary	
Design Flow Methodology	Incremental compilation[1]	Improves design timing closure and reduces design compilation times up to 70 percent. Supports team-based design.
	Pin planner	Eases the process of assigning and managing pin assignments for high-density and high-pin-count designs.
	Qsys (replaces SOPC Builder)	Automates system development by integrating IP functions and subsystems (collection of IP functions) using a hierarchical approach and a high-performance interconnect (based on a network-on-a-chip architecture).
	Off-the-shelf IP cores	Lets you construct your system-level design using IP cores from Altera and from Altera's third-party IP partners.
	Parallel development in ASICs[1]	Allows for FPGA prototypes to be designed in parallel using the same design software and IP.
	Scripting support	Supports command-line operation and Tcl scripting, as well as GUI design.
	Rapid Recompile[1]	Maximizes your productivity by reducing your compilation time by 50 percent on average (for a small design change after a full compile). Improves design timing preservation.
Performance and Timing Closure Methodology	Physical synthesis	Uses post placement and routing delay knowledge of a design to improve performance.
	Design space explorer (DSE)	Increases performance by automatically iterating through combinations of Quartus II software settings to find optimal results.
	Extensive cross-probing	Provides support for cross-probing between verification tools and design source files.
	Optimization advisors	Provides design-specific advice to improve performance, resource usage, and power consumption.
	Chip planner	Reduces verification time (while maintaining timing closure) by enabling small, post placement and routing design changes to be implemented in minutes.
Verification	TimeQuest timing analyzer	Provides native Synopsys® Design Constraint (SDC) support and allows you to create, manage, and analyze complex timing constraints and quickly perform advanced timing verification.
	SignalTap II embedded logic analyzer[2]	Supports the most channels, fastest clock speeds, largest sample depths, and most advanced triggering capabilities available in an embedded logic analyzer.
	System Console	Enables you to easily debug your FPGA in real time using read and write transactions. It also enables you to quickly create a GUI to help monitor and send data into your FPGA.
	PowerPlay technology	Enables you to accurately analyze and optimize both dynamic and static power consumption.
Third-Party Support	EDA partners	Offers EDA software support for synthesis, functional and timing simulation, static timing analysis, board-level simulation, signal integrity analysis, and formal verification. To see a complete list of partners, visit www.altera.com/products/software/partners/eda_partners/eda-index.html.

[1] Included in Subscription Edition only.
[2] Available with Talkback feature enabled in Web Edition.

Getting Started Steps

Step 1: Download free Web Edition

www.altera.com/download

Step 2: Get oriented with Quartus II software interactive tutorial

After installation, open the interactive tutorial on the welcome screen.

Step 3: Sign up for training

www.altera.com/training

Quartus II Design Software

Purchase Quartus II software and increase your productivity today.

Pricing	Description
$2,995 (SW-QUARTUS-SE-FIX) Renewal $2,495 (SWR-QUARTUS-SE-FIX)	Fixed-node license: subscription for one year—Windows only.
$3,995 (SW-QUARTUS-SE-FLT) Renewal $2,495 (SWR-QUARTUS-SE-FLT) Add seat $3,995 (SW-QUARTUS-SE-ADD)	Floating-node license: subscription for one year—Windows/Linux.

ModelSim-Altera Edition Software	
$945 (SW-MODELSIM-AE) Renewal $945 (SWR-MODELSIM-AE)	ModelSim-Altera Edition software is available as a $945 option for both Quartus II Subscription Edition and Web Edition software. It's 33 percent faster than Starter Edition with no line limitation.
ModelSim-Altera Starter Edition Software	
Free	Free for both Quartus II Subscription Edition and Web Edition software with a 10,000 executable line limitation, ModelSim-Altera Starter Edition software is recommended for simulating small FPGA designs.

Altera SDK for OpenCL

The Altera SDK for OpenCL* allows the easy implementation of applications onto FPGAs by abstracting away the complexities of FPGA design, allowing software programmers to write hardware-accelerated kernel functions in OpenCL C, an ANSI C-based language with additional OpenCL constructs to extract parallelism. The FPGA, as an accelerator, provides significant advantages over a CPU or GPU by allowing the creation of customized small scalar or large vector processing units or a deep hardware pipeline to create a completely custom accelerator at the lowest possible power.

Altera SDK for OpenCL Software Features Summary	
Offline compiler (aoc)	• GCC-based model compiler of OpenCL kernel code
Altera OpenCL Utility (aocl)	• Diagnostics for board installation • Flash or program FPGA image • Install board drivers (typically PCIe)
Altera SDK for OpenCL Licensing	• Purchase a one year perpetual license ($995) • Fixed and float available • 60-day evaluation license available on request • Requires licensed Quartus II software Subscription Edition or Development Kit Edition
Operating System	• Microsoft 64 bit Windows 7 • Red Hat Enterprise 64 bit Linux (RHEL) 6.x
Memory Requirements	• Computer equipped with at least 16 GB RAM

* Product is based on a published Khronos Specification, and has passed the Khronos Conformance Testing Process. Current conformance status can be found at www.khronos.org/conformance.

SoC Embedded Design Suite

The Altera SoC Embedded Design Suite (EDS) is a comprehensive tool suite for embedded software development on Altera SoCs. It comprises development tools, utility programs, run-time software, and design examples to jump-start firmware and application software development. The SoC EDS includes an exclusive offering of the ARM Development Studio™ 5 (DS-5™) Altera Edition Toolkit.

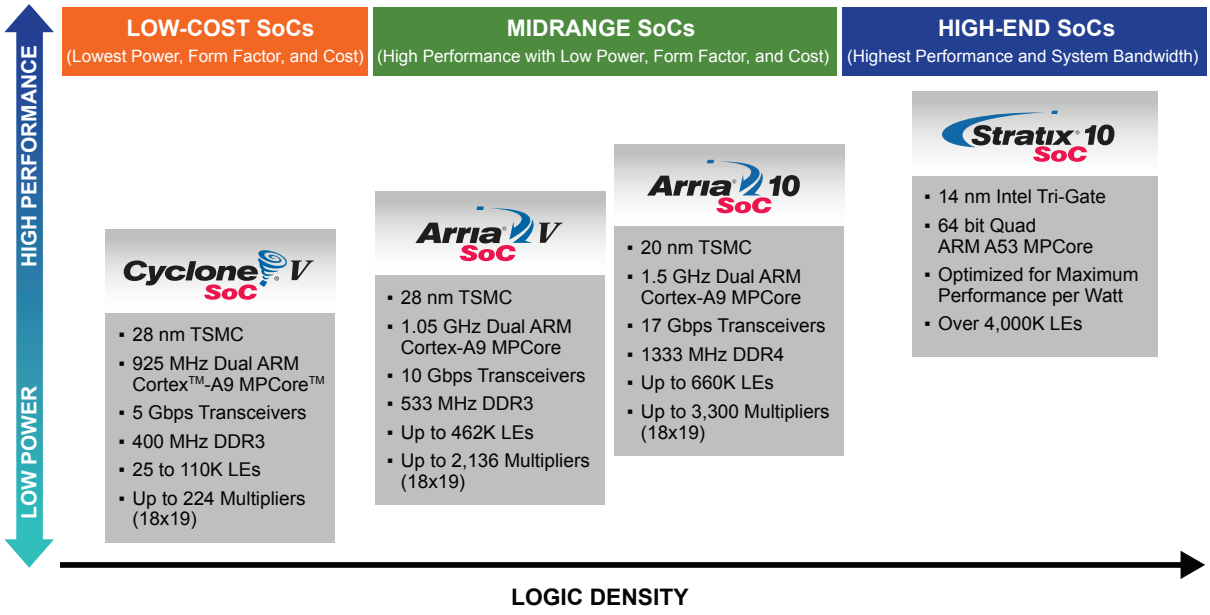
	SoC Embedded Design Suite		
	SoC EDS Key Features	Availability	
		Subscription Edition	Web Edition (Free)
Hardware/Software Handoff Tools	Preloader Generator	✓	✓
	Device Tree Generator	✓	✓
Compiler Tools	Linaro Compiler	✓	✓
	Sourcery EABI GNU Compiler	✓	✓
Run-time	SoC Linux		✓
	U-Boot		✓
Libraries	SoC Abstraction Layer (SoCAL)	✓	✓
	Hardware Manager	✓	✓
DS-5 Altera Edition Features	Linux application debugging over Ethernet	✓	✓
	Debugging over USB-Blaster™ II cable - Board bring-up - Device driver development - Operating system (OS) porting - Bare-metal programming	✓	
	FPGA-adaptive debugging - Auto peripheral register discovery - Cross-triggering between CPU and FPGA domains - ARM CoreSight trace support - Access to System Trace Module (STM) events	✓	
	Streamline Performance Analyzer support	✓	Limited
Getting Started Examples	Golden system reference designs for SoC development kits	✓	✓
Others	Other design examples: - DeviceWide Asymmetric Multi Processing (AMP) - Triple Speed Ethernet (TSE) with Modular Scatter Gather Direct Memory Access (mSGDMA) - PCIe Root Port (RP) with Message Signaled Interrupts (MSI)	✓	✓
	Quartus II Programmer	✓	✓
	SignalTap II Logic Analyzer	✓	✓
	Altera Boot Disk Utility	✓	✓
	OS Support	Availability	
		Subscription Edition	Web Edition (Free)
	Windows/Linux 32 bit support	✓	✓
	Windows/Linux 64 bit support	Compatible	Compatible

SoC Embedded Design Suite	Pricing
Subscription Edition (ESW-SOCEDS-DS5-FIX)	$995
Web Edition	Free

Altera's Customizable Processor Portfolio

www.altera.com/embedded

Altera's processor portfolio comprises SoCs, which feature single- or dual-core ARM Cortex-A9 MPCore hard processor systems as well as soft processors that can be used in any FPGA or SoC.



Summary of Processors

Category	Processor	Vendor	Description
Hard processors for SoC			
Applications processing	Dual-core ARM Cortex-A9	Altera	Altera's 28 nm Cyclone V and Arria V SoC families and 20 nm Arria 10 SoCs offer integrated ARM-based HPS, comprising peripherals, memory, and interfaces, with an FPGA fabric.
Soft processors			
Power- and cost-optimized processing	Nios II economy core	Altera	With unique, real-time hardware features, such as custom instructions (ability to use FPGA hardware to accelerate a function), vectored interrupt controller, and tightly coupled memory, as well as support for industry-leading real-time operating systems (RTOS), the Nios II processor meets both your hard and soft real-time requirements.
Real-time processing	Nios II standard and fast core	Altera	With unique, real-time hardware features, such as custom instructions (ability to use FPGA hardware to accelerate a function), vectored interrupt controller, and tightly coupled memory, as well as support for industry-leading RTOS, the Nios II processor offers a versatile solution for real-time processing.
Applications processing	Nios II fast core	Altera	A simple configuration option enables the Nios II fast core to use a memory management unit to run embedded Linux. Both open source and commercially supported versions of Linux for Nios II processors are available.
Safety-critical processing	Nios II SC	H-Cell	Certify your design for DO-254 compliance by using the Nios II Safety Critical core along with the DO-254 compliance design services offered by H-Cell.

Altera's Customizable Processor Portfolio

Performance and Feature Set Summary of Key Processors Supported on Altera Devices						
Category	**Cost-and Power-Sensitive Processors**		**Real-Time Processor**		**Applications Processors**	
Features	**ARM Cortex-M1**	**Nios II Economy**	**Nios II Standard**	**Nios II Fast**	**28 nm[1] Dual-Core ARM Cortex-A9**	**20 nm[2] Dual-Core ARM Cortex-A9**
Maximum frequency (MHz)	200	340 (Stratix V)	300 (Stratix V)	310	925 MHz (Cyclone V SoC) 1.05 GHz (Arria V SoC)	1.5 GHz
Maximum performance (MIPS[3] at MHz) Stratix series	160 (at 200 MHz)	51 (at 340 MHz)	192 (at 300 MHz)	350 (at 310 MHz)	–	–
Maximum performance (MIPS[3] at MHz) Arria series	–	45 (at 300 MHz)	108 (at 170 MHz)	192 (at 170 MHz)	2,625 MIPS per core at 1.05 GHz	3,750 MIPS per core at 1.5 GHz
Maximum performance (MIPS[3] at MHz) Cyclone series	–	30 (at 200 MHz)	89 (at 145 MHz)	180 (at 160 MHz)	2,313 MIPS per core at 925 MHz	–
Maximum performance efficiency (MIPS[3] per MHz)	0.8	0.15	0.64	1.13	2.5	2.5
16/32 bit instruction set support	16 and 32	32	32	32	16 and 32	16 and 32
Level 1 instruction cache	–	–	Configurable	Configurable	32 KB	32 KB
Level 1 data cache	–	–	–	Configurable	32 KB	32 KB
Level 2 cache	–	–	–	–	512 KB	512 KB
Memory management unit	–	–	–	Configurable	✓	✓
Floating-point unit	–	–	FPCI[4]	FPCI[4]	Dual precision	Dual precision
Vectored interrupt controller	✓	–	✓	✓	–	–
Tightly coupled memory	Up to 64K	–	Configurable	Configurable	–	–
Custom instruction interface	–	Up to 256	Up to 256	Up to 256	–	–
Equivalent LEs	2,500	600	1,200	1,800 – 3,200	HPS	HPS

[1] Altera 28 nm SoCs comprise Cyclone V SoCs and Arria V SoCs
[2] Altera 20 nm SoCs comprise Arria 10 SoCs
[3] Dhrystone 2.1 benchmark
[4] Floating-point custom instructions

Altera's Customizable Processor Portfolio

Available OS Board Support Packages			
OS	**OS BSP Supplier**	**Nios II Processor**	**ARM-Based SoC**
eCos	eCosCentric	✓	✓
eCos (Zylin)	Zylin	✓	–
embOS	Segger	✓	–
EUROS	Euros	✓	–
Linux	Wind River	✓	✓
Linux	SLS	✓	–
Linux	Open Source	✓	✓
oSCAN	Vector	✓	–
ThreadX	Express Logic	✓	✓
µCLinux	Open Source*	✓	–
VxWorks	Wind River	–	✓
Toppers	Open Source	✓	–
OSE	Enea	–	✓
INTEGRITY	Green Hills Software	–	✓
µC/OS-II, µC/OS-III	Micriμm	✓	✓
QNX Neutrino	QNX	–	✓
Android	FUJISOFT	–	✓
Windows Embedded	iWave	–	✓
µITRON	eSol	–	✓

*Refer to **www.rocketboards.org**

Getting Started

Learn more about Altera's portfolio of customizable processors and how you can get started by visiting **www.altera.com/embedded.**

Nios II Processor

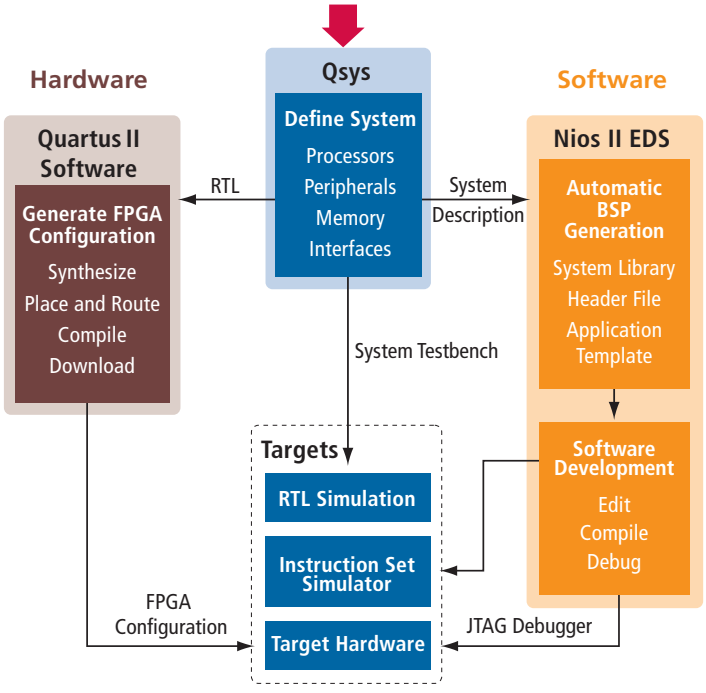
Altera's Nios II processor, the world's most versatile processor according to Gartner Research, is the most widely used soft processor in the FPGA industry. This soft processor delivers unprecedented flexibility for your cost-sensitive, real-time, safety-critical (DO-254), and applications processing needs. All Altera FPGA device families support the Nios II processor.

The Nios II processor in any one of Altera's FPGAs offers a custom SoC solution that has the flexibility of software and the performance of hardware. Through its innovative design, the Nios II processor leverages the logic resources of the device to provide unprecedented hard and soft real-time capabilities.

You can:

- Lower overall system cost, complexity, and power consumption by integrating the processor with the FPGA.
- Scale performance with multiple processors, custom instructions (hardware acceleration of a processor instruction) or co-processor modules (hardware accelerator next to the soft processor).
- Target any Stratix, Arria, or Cyclone series FPGA.
- Eliminate the risk of processor and ASSP device obsolescence.
- Take advantage of the free Nios II economy core, the free Nios II Embedded Design Suite (EDS), and the free NicheStack TCP/IP Network Stack - Nios II Edition software to get started today.

Nios II Processor Development Flow



Nios II Processor

Nios II EDS Contents
Nios II Software Build Tools (SBT) for Eclipse, for software development • Based on Eclipse IDE • New project wizards • Software templates • Source navigator and editor • Compiler for C and C++ (GNU)
Software Debugger/Profiler
Flash Programmer
Embedded Software • Hardware Abstraction Layer (HAL) • MicroC/OS-II RTOS • NicheStack TCP/IP Network Stack—Nios II Edition • Newlib ANSI-C standard library • Simple file system
Other Altera Command-Line Tools and Utilities
Design Examples

Hardware Development Tools

- Quartus II design software
- Qsys system integration tool
- SignalTap II embedded logic analyzer plug-in for Nios II processor
- System Console for low-level debug of Qsys systems

Licensing

Getting started with the Nios II processor is now easier than ever. Not only is the Nios II EDS free, but the Nios II economy core IP is also free.

As for the Nios II standard and fast core IP, licenses are available for stand-alone IP (IP-NIOS) or as part of the Embedded IP Suite (IPS-EMBEDDED). These royalty-free licenses never expire and allow you to target your processor design on any Altera FPGA. The Embedded IP Suite is a value bundle that contains licenses of the Nios II processor IP core, DDR1/2 Memory Controller IP core, Triple-Speed Ethernet MAC IP core, and the NicheStack TCP/IP Network Stack-Nios II Edition software.

Development Kits

Go to page 70 for information about embedded development kits.

Nios II EDS: What You Get for Free!

The Nios II Embedded Design Suite (EDS) provides all the tools and software you need to develop code for the Nios II processor.

With the Nios II EDS you can:

- **Develop software with Nios II Software Build Tools for Eclipse: Based on industry-standard Eclipse, the Nios II Software Build Tool (SBT) is an integrated development environment for editing, compiling, debugging software code, and flash programming.**
- **Manage board support packages (BSP): The Nios II EDS makes managing your BSP easier than ever. Nios II EDS will automatically add device drivers for Altera-provided IP to your BSP. The BSP Editor provides full control over your build options.**
- **Get free Network Stack software: The Nios II EDS includes NicheStack TCP/IP Network Stack-Nios II Edition—a commercial-grade network stack software—for free.**
- **Evaluate a RTOS: The Nios II EDS contains an evaluation version of the popular Micrium MicroS/OS-II RTOS. Product licenses are sold separately by Micrium.**

Join the Nios II Community!

Be part of thousands of Nios II developers by visiting Altera Wiki and Altera Forum. Altera Wiki has hundreds of design examples and design tips from Nios II developers all over the world. Join ongoing discussions on the Nios II section of Altera Forum to know more about Nios II Linux, hardware, and software development.

Visit the following websites:

www.alterawiki.com

www.alteraforum.com

www.rocketboards.org

Altera and Partner Functions

www.altera.com/selector

The following is a partial list of IP functions from Altera and its partners. To get the details, check out our online selector guide.

	Product Name	Vendor Name
DSP	**Error Detection/Correction**	
	Reed-Solomon Compiler Decoder	Altera
	Reed-Solomon Compiler Encoder	Altera
	Reed-Solomon Encoder/Decoder II[1]	Altera
	Viterbi Compiler, High-Speed Parallel Decoder	Altera
	Viterbi Compiler, Low-Speed/ Hybrid Serial Decoder	Altera
	DVB-RCS CTC Turbo Decoder	TurboConcept
	WiMAX CTC Decoder	TurboConcept
	3GPP/LTE CTC Decoder	TurboConcept
	Turbo Product Code Decoder	TurboConcept
	Filters and Transforms	
	Fast Fourier Transform (FFT)/ Inverse FFT (IFFT)	Altera
	Cascaded Integrator Comb (CIC) Compiler	Altera
	Finite Impulse Response (FIR) Compiler	Altera
	FIR Compiler II	Altera
	2D Forward/Inverse Discrete Cosine Transform	CAST, Inc.
	2D Inverse Discrete Cosine Transform (IDCT)	CAST, Inc.
	Forward Discrete Cosine Transform (DCT)	CAST, Inc.
	Modulation/Demodulation	
	Numerically Controlled Oscillator Compiler	Altera
	DVB-C/J.83 (QAM) Modulator	Commsonic
	DVB/H T/H Modulator	Commsonic
	DVB-S2 Modulator	Commsonic
	Video and Image Processing	
	Video and Image Processing Suite[1]	Altera
	JPEG Decoder and Encoder	Barco Silex
	JPEG 2000 Sub-Frame Latency Encoder and Decoder	Barco Silex
	Multi-Channel JPEG 2000 Encoder and Decoder Cores	Barco Silex

[1]Qsys-compliant licensed core.

	Product Name	Vendor Name
DSP (Continued)	JPEG CODEC	CAST, Inc.
	JPEG Encoders and Decoders	CAST, Inc.
	Lossless JPEG Encoder and Decoder	CAST, Inc.
	H.264 AVC High-Definition (HD) and Extended Definition (ED) Video Encoder	CAST, Inc.
	H.264 Encoders	Jointwave Group LLC
	Arithmetic	
	Floating-Point Addition/ Subtraction	Altera
	Floating-Point Multiplication	Altera
	Floating-Point Division	Altera
	Floating-Point Square Root	Altera
	Floating-Point Compare	Altera
	Floating-Point Arithmetic Unit	Digital Core Design
	Floating-Point Mathematics Unit	Digital Core Design
	Floating-Point Pipelined Divider Unit	Digital Core Design
	Floating-Point-to-Integer Pipelined Converter	Digital Core Design
	Integer-to-Floating-Point Pipelined Converter	Digital Core Design
	Additional Functions	
	Advanced Encryption Standard (AES) Engine	Barco Silex
	DES/3DES	Barco Silex
	Hashing	Barco Silex
	Public Key	Barco Silex
	SHA-1	CAST, Inc.
	SHA-256	CAST, Inc.
	AES CODEC	CAST, Inc.

Altera and Partner Functions

	Product Name	Vendor Name
Embedded Processors	**32 bit/16 bit**	
	Nios II Embedded Processor[1]	Altera
	ARM Cortex-A9 MPCore Processor	Altera
	ARM Cortex-M1[1]	ARM
	C68000 and AHB Microprocessors	CAST, Inc.
	C80186EC and XL Microprocessors	CAST, Inc.
	V1 ColdFire[1]	Freescale
	8 bit	
	T8051	CAST, Inc.
	8051XC2 Microcontroller	CAST, Inc.
	DP8051 8 bit Microcontroller	Digital Core Design
	DP8051XP Pipelined, High-Performance 8 bit Microcontroller	Digital Core Design
	DF6811E 8 bit Fast Microcontroller	Digital Core Design
	DFPIC1655X 8 bit RISC Microcontroller	Digital Core Design
Interface and Protocols	**Communication**	
	POS-PHY Level 4	Altera
	Optical Transport Network (OTN) Framers/Deframers	Altera
	SFI-5.1	Altera
	SONET / Synchronous Digital Hierarchy (SDH) Framer / Deframer	Aliathon
	SONET / SDH Mapper / Demapper	Aliathon
	Synchronous Data Link Control (SDLC) Controller	CAST, Inc.
	Ethernet	
	10 Gbps Ethernet MAC[1] with 1588	Altera
	Triple-Speed Ethernet (10/100/1000 Mbps) MAC and PHY[1] with 1588	Altera
	10GBASE-R PHY	Altera
	10G Base-X (XAUI) PHY	Altera

	Product Name	Vendor Name
Interface and Protocols (Continued)	40G Ethernet MAC and PHY	Altera
	100G Ethernet MAC and PHY	Altera
	Backplane Ethernet 10GBASE-KR PHY	Altera
	1G/10Gb Ethernet PHY	Altera
	Gbps Ethernet (GbE) MAC[1]	IFI
	Advanced GbE MAC[1]	IFI
	EtherCAT (Software Stack)	IXXAT
	Ethernet Powerlink	IXXAT
	EtherNET/IP	IXXAT
	Fast XAUI	Macnica Americas
	10G MAC Lite	Macnica Americas
	40G/100G Ethernet	MorethanIP
	10GbE MAC and PCS	MorethanIP
	RXAUI PCS	MorethanIP
	SPAUI MAC	MorethanIP
	DXAUI PCS	MorethanIP
	QSGMII PCS	MorethanIP
	2.5 Gbps Ethernet MAC	MorethanIP
	EtherNET/IP	Softing AG
	EtherCAT (Software Stack)	Softing AG
	High Speed	
	Serial RapidIO®[1]	Altera
	Common Public Radio Interface (CPRI)	Altera
	Interlaken	Altera
	Interlaken Look-Aside	Altera
	SerialLite II	Altera
	SerialLite III	Altera
	SATA 1.0/SATA 2.0	Intelliprop, Inc.
	QPI	Intel Corporation
	HyperTransport™ 3.0	University of Heidelberg

[1]Qsys-compliant licensed core.

Altera and Partner Functions

	Product Name	Vendor Name
Interface and Protocols (Continued)	**PCI**	
	PCIe Gen1 x1[1], x4[1], x8 Controller (Soft IP)	Altera
	PCIe Gen1 and Gen2 x1, x4, and x8 Lane (Hard IP)	Altera
	PCI Compiler, 32 bit Master/Target	Altera
	PCI Compiler, 32 bit Target	Altera
	PCIe Controller	CAST, Inc.
	PCIe x8 Controller	CAST, Inc.
	PCI 32/64 bit PCI Master/ Target 33/66 MHz Controllers	CAST, Inc.
	PCI Multifunction Target Interface	CAST, Inc.
	PCIe Gen1 x1, x4, x8 Controller	Northwest Logic, Inc.
	PCIe Complete Core x1, x4, x8	Northwest Logic, Inc.
	PCI-X Controller	Northwest Logic, Inc.
	Integrated PCI Core	Northwest Logic, Inc.
	PCI Interface	Northwest Logic, Inc.
	PCIe, Gen1, Gen2, and Gen3	PLDA
	PCI and PCI-X Master / Target Cores 32/64 bit	PLDA
	Serial	
	Serial Peripheral Interface (SPI)[2]	Altera
	SPI/Avalon® Master Bridge[2]	Altera
	UART[2]	Altera
	JTAG UART[2]	Altera

	Product Name	Vendor Name
Interface and Protocols (Continued)	JTAG/Avalon Master Bridge[2]	Altera
	C_CAN[1]	Bosch
	I²C Bus Controller[1]	CAST, Inc.
	I²C Bus Controller Slave	CAST, Inc.
	CAN[1]	CAST, Inc.
	Local Interconnect Network (LIN) Controller	CAST, Inc.
	SPI Master/Slave	CAST, Inc.
	H16450S UART	CAST, Inc.
	H16550S UART	CAST, Inc.
	H16750S UART	CAST, Inc.
	MD5	CAST, Inc.
	Smart Card Reader	CAST, Inc.
	DI2CM I²C Bus Interface-Master	Digital Core Design
	DI2CSB I²C Bus Interface-Slave	Digital Core Design
	D16550 UART with 16-Byte FIFO	Digital Core Design
	DSPI Serial Peripheral Interface Master/Slave	Digital Core Design
	Secure Digital (SD)/MMC SPI	El Camino GmbH
	Secure Digital I/O (SDIO)/SD Memory/Slave Controller	Eureka Technology, Inc.
	UART	Eureka Technology, Inc.
	SDIO/SD Memory/ MMC Host Controller	Eureka Technology, Inc.
	Nios II Advanced CAN[1]	IFI
	MediaLB Device Interface[1]	IFI
	I²C Master/Slave/PIO Controller	Microtronix, Inc.
	USB 1.1 Host/Device	Microtronix, Inc.

[1]Qsys-compliant licensed core.
[2]Qsys component (no license required).

Altera and Partner Functions

	Product Name	Vendor Name
Interface and Protocols (Continued)	I²C Master and Slave	SLS
	PS2 Interface	SLS
	USB High-Speed Function Controller[1]	SLS
	USB Full/Low-Speed Function Controller[1]	SLS
	SD Host Controller[1]	SLS
	USB 3.0 SuperSpeed Device Controller	SLS
	Audio and Video	
	Character LCD[2]	Altera
	Pixel Converter (BGR0 -> BGR)[2]	Altera
	Video Sync Generator[2]	Altera
	Asynchronous Serial Interface (ASI)	Altera
	SD/HD/3G-HD serial digital interface (SDI)	Altera
	DisplayPort	Altera
	DisplayPort	Bitec
	V-by-One HS	Bitec
	Video LVDS Serializer/Deserializer (SERDES) Transmitter/Receiver	Microtronic, Inc
	I2S Audio CODEC[1]	SLS
Memories and Memory Controllers	**DMA**	
	Scatter Gather DMA Controller[2]	Altera
	DMA Controller[2]	Altera
	DMA for Hard PCIe (EZDMA2)	PLDA
	Flash	
	CompactFlash (True IDE)[2]	Altera
	EPCS Serial Flash Controller[2]	Altera
	Flash Memory[2]	Altera
	NFlashCtrl NAND Flash Memory Controller	CAST, Inc.
	NAND Flash Controller	Eureka Technology, Inc.
	ISA/PC Card/PCMCIA/ CompactFlash Host Adapter	Eureka Technology, Inc.
	ONFI Controller	SLS
	CompactFlash Interface[1]	SLS

[1]Qsys-compliant licensed core.
[2]Qsys component (no license required).

	Product Name	Vendor Name
Memories and Memory Controllers (Continued)	**SDRAM**	
	DDR / DDR2 and DDR3 SDRAM Controllers[1]	Altera
	LPDDR2 SDRAM Controller	Altera
	RLDRAM 2 Controller	Altera
	Streaming Multi-Port SDRAM Memory Controller	Microtronix, Inc.
	HyperDrive Multi-Port DDR2 Memory Controller	Microtronix, Inc.
	Avalon Multi-Port SDRAM Memory Controller[1]	Microtronix, Inc.
	DDR and DDR2 SDRAM Controllers	Northwest Logic, Inc.
	RLDRAM II and III Controllers	Northwest Logic, Inc.
	Mobile DDR SDRAM Controller	Northwest Logic, Inc.
	Mobile SDR SDRAM Controller	Northwest Logic, Inc.
	SDR SDRAM Controller	Northwest Logic, Inc.
	LPDDR2 / 3 Controllers	Northwest Logic, Inc.
	SRAM	
	SSRAM (Cypress CY7C1380C)[2]	Altera
	QDR II / II+ SRAM Controller	Altera

Transceiver Protocols

www.altera.com/datarates

Altera device transceivers support the protocols listed in the following table. For details about the data rates, please visit www.altera.com/datarates.

Protocols/ Interface Standards	Supported Devices												
	Stratix Series FPGAs					Arria Series FPGAs					Cyclone Series FPGAs		
	V GX/GS	V GT	IV GX	IV GT	II GX	V GX	V GT/ST	V GZ	II GX	II GZ	V GX/SX	V GT/ST	IV GX
Basic (proprietary)	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
CEI-6G-SR/LR	✓	✓	✓	✓	✓	✓	✓	✓	–	–	–	–	–
CEI-11G-SR	✓	✓	–	✓	–	–	–	–	–	–	–	–	–
CEI-28G-VSR	–	✓	–	–	–	–	–	–	–	–	–	–	–
SFP+/SFF-8431	✓	✓	–	✓	–	–	–	✓	–	–	–	–	–
XFI	✓	✓	–	✓	–	–	✓	–	–	–	–	–	–
XFP	✓	✓	–	–	–	–	–	✓	–	–	–	–	–
1000BASE-X (GbE)	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
10GBASE-R	✓	✓	–	✓	–	–	✓	✓	–	–	–	–	–
10GBASE-KR	✓	✓	–	–	–	–	–	✓	–	–	–	–	–
ASI	✓	✓	✓	✓	✓	✓	✓	–	✓	✓	–	–	–
CPRI	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
CAUI / XLAUI	✓	✓	–	✓	–	–	–	✓	–	–	–	–	–
CAUI-4	–	✓	–	–	–	–	–	–	–	–	–	–	–
DisplayPort	✓	✓	✓	✓	✓	✓	✓	✓	–	–	✓	✓	✓
Fibre Channel	✓	✓	✓	✓	✓	–	✓	✓	–	–	–	–	–
GPON	✓	✓	✓	✓	–	✓	✓	✓	✓	✓	–	–	–
G.709 OTU-2	✓	✓	–	✓	–	✓	✓	–	–	–	✓	✓	✓
OTN with FEC	✓	✓	–	✓	–	–	–	–	–	–	–	–	–
HiGig	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	–	–	–
High-Definition Multimedia Interface (HDMI)	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓

Transceiver Protocols

Protocols	Supported Devices												
	Stratix Series FPGAs					Arria Series FPGAs					Cyclone Series FPGAs		
	V GX/GS	V GT	IV GX	IV GT	II GX	V GX	V GT/ST	V GZ	II GX	II GZ	V GX/SX	V GT/ST	IV GX
JESD204 A/B	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
HMC[1]	–	–	–	–	–	–	–	–	–	–	–	–	–
HyperTransport	✓	✓	✓	✓	–	✓	✓	✓	–	–	–	–	–
InfiniBand	✓	✓	–	–	–	–	–	✓	–	–	–	–	–
Interlaken	✓	✓	✓	✓	–	✓	✓	✓	–	–	–	–	–
Interlaken Look-Aside	✓	✓	–	–	–	✓	✓	✓	–	–	–	–	–
MoSys	✓	–	–	–	–	–	–	–	–	–	–	–	–
OBSAI	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
PCI Express	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
RXAUI / DXAUI	✓	✓	✓	✓	✓	✓	✓	✓	–	–	–	–	–
SGMII / QSGMII	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
QPI	✓	✓	–	–	–	–	–	✓	–	–	–	–	–
SAS / SATA	✓	✓	✓	✓	–	✓	✓	✓	✓	✓	✓	✓	✓
SerialLite II	✓	✓	✓	✓	–	✓	✓	–	✓	✓	–	–	–
SerialLite III	✓	✓	–	–	–	–	–	✓	–	–	–	–	–
SDI	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
SFI-5.1	✓	✓	✓	✓	✓	✓	✓	✓	–	–	–	–	–
SFI-S / SFI-5.2	✓	✓	–	✓	–	–	–	✓	–	–	–	–	–
RapidIO®	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
SPAUI	✓	✓	✓	✓	✓	–	–	✓	–	–	–	–	–
SONET / SDH	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	–	–	–
XAUI (10GBASE-X)	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
V-by-One	✓	✓	✓	✓	✓	✓	✓	–	–	–	–	–	✓

[1]Contact Altera for more details on HMC support.

Altera and Partner Development Kits

The following is a list of Altera and partner development kits. To get more details about these development kits or other older development kits that are available, check out our online selector guide at www.altera.com/selector.

	Product and Vendor Name	Device	Description
DSP	DSP Development Kit, Stratix V Edition **Altera**	Stratix V 5SGSMD5K2F40C2N	The DSP Development Kit, Stratix V Edition provides a complete design environment that includes all the hardware and software you need to begin developing DSP-intensive FPGA designs immediately. The development kit is RoHS compliant. You can use this development kit to develop and test PCIe designs at data rates up to Gen3, develop and test memory subsystems for DDR3 SDRAM or QDR II SRAM memories, and use the high-speed mezzanine card (HSMC) connectors to interface to one of over 35 different HSMCs provided by Altera partners, supporting protocols such as Serial RapidIO, 10 Gbps Ethernet, SONET, CPRI, OBSAI, and others.
	Audio Video Development Kit, Stratix IV GX Edition **Altera**	Stratix IV GX EP4SGX230	This kit provides a complete video and image processing development environment for design engineers. It features the Stratix IV GX FPGA development board along with an SDI HSMC and associated reference designs.
	DSP Development Kit, Stratix III Edition **Altera**	Stratix III EP3SL150	This kit comprises a Stratix III development board with a HSMC equipped with 16 bit A/D and D/A converters (operating at up to 200 MSPS). The HSMC also has interfaces to TI DSP processors, allowing the designs that use Stratix III FPGAs to be created both as stand-alone devices and as companion devices. The kit also contains Altera's Quartus II software, DSP Builder software, and a 30-day trial of MATLAB/Simulink.
	DSP Development Kit, Cyclone III Edition[1] **Altera**	Cyclone III EP3C120N	This kit is for general DSP or wireless design engineers, regardless of whether you need pre-processing, DSP plus FPGA coprocessing, or post-processsing. This kit includes complete 16 bit high-speed analog-to-digital (A/D) and digital-to-analog (D/A) converters (operating at up to 200 MSPS), as well as interfaces to TI DSP processors (DM642 and DaVinci). Altera's DSP Builder GUI simplifies the information flow between the FPGA toolset and MATLAB/Simulink (30-day evaluation copy included).
	ProcHILs **GiDEL**	Stratix V Stratix IV	This development kit provides a state-of-the-art Hardware in the Loop acceleration tool for running Simulink designs on Altera's FPGAs. ProcHILs can automatically translate Simulink designs built using Altera's DSP Builder into FPGA code and run this code under Simulink. The generated code is compatible with the Proc board installed on the target PC and has the synchronization code needed to communicate with Simulink via PCIe.
	DE3 Stratix III High Speed Rapid Prototyping System **Terasic Technologies, Inc.**	Stratix III EP3SL150F1152C2N EP3SE260F1152C2N EP3SL340F1152C2N	This board is the perfect platform for creating your design in programmable logic. DE3 boards are available with either the EP3SL150, the EP3SL340, or the EP3SL260 (DE3-260) devices that are optimized with the extra on-chip multipliers needed for DSP research and development. All of the DE3 boards can be stacked and all feature the same connector for expanding the base functionality with daughtercards.
	OmniTek Audio Video **OmniTek**	Arria II GX EP2AGX125EF35	This Arria II GX audio and video development kit combines Altera's proven FPGA-based development hardware and associated IP with OmniTek's expertise in video algorithm IP and PCIe interface design to offer a PCIe Gen1 image processing environment.
	Cyclone III Video and Image Processing Development Kit[1] **Bitec**	Cyclone III EP3C120N	This kit is designed to help you start developing complex video applications. It supports various video I/O interfaces, allowing you to get your video data in and out of the Cyclone III FPGA. Different video interfaces are supported using the different daughtercards included in this kit: cards supporting Asynchronous Serial Interface (ASI) or SDI, composite, component, and digital video interfaces (DVIs).
	Software Programmable Reconfiguration (SPR) Development System **BittWare**	Cyclone III FPGA	This development system provides a system platform to explore software reconfiguration of waveform functionality for high-end signal processing applications such as software-defined radio. The platform provides a flexible, portable, low-cost environment for software-defined radio development in an Advanced Mezzanine Card (AdvancedMC) and Micro Telecommunications Computing Architecture (MicroTCA) environment, enabling you to quickly and cost-effectively bring your waveform designs to life.

[1] RoHS compliant.

Altera and Partner Development Kits

	Product and Vendor Name	Device	Description
DSP (Continued)	SC DVI Output Module **Bitec**	Daughtercard	This module supports all Altera development kits with Altera DVI expansion slots.
	THDB-ADA **Terasic Technologies, Inc.**	Daughtercard	This card provides dual A/D channels with 14 bit resolution with data rates up to 65 MSPS and dual D/A channels with 14 bit resolution with data rates up to 125 MSPS. It supports both Altera HSMC and Terasic DE-style connectors.
	HSMC Dual-Link DVI Board **Bitec**	Daughtercard	This daughtercard is a two-channel, dual-link DVI output board for Altera FPGA development kits with HSMC expansion port.
	SC DVI Output Module **Bitec**	Daughtercard	This module supports all Altera development kits with Altera DVI expansion slots.
I/O Interconnect	Stratix V GX FPGA Development Kit **Altera**	Stratix V GX 5SGXEA7K2F40C2N	This kit provides a full-featured hardware development platform for prototyping and testing high-speed serial interfaces to a Stratix V GX FPGA. This kit includes the PCIe x8 form factor, two HSMC connectors for expandability, and Ethernet, USB, and SDI interfaces. Memory includes one x72 DDR3 SDRAM, one x18 QDR II+ SRAM, and flash. This kit also includes two SMA connectors for a differential transceiver output. Several programmable oscillators are available and other user interfaces include three user push buttons, eight DIP switches, eight bi-color user LEDs, an LCD display, and power and temperature measurement circuitry.
	Transceiver Signal Integrity Kit, Stratix V GX Edition **Altera**	Stratix V GX 5SGXEA7N2F40C2N	This kit enables a thorough evaluation of transceiver signal integrity and device interoperability. Features include seven full-duplex transceiver channels with SMA connectors, two 14G backplane connectors (from Amphenol and Molex), four programmable clock oscillators, four user push buttons, eight DIP switches, eight user LEDs, a 7-segment LCD display, power and temperature measurement circuitry, and Ethernet, an embedded USB Blaster download cable, and JTAG interfaces.
	Transceiver Signal Integrity Development Kit, Stratix V GT Edition **Altera**	Stratix V GT 5SGTMC7K3F40C2N	The Altera Stratix V GT Transceiver Signal Integrity (SI) Development Kit provides a platform for electrical compliance testing and interoperability analysis. The accessibility to multiple channels allows for real-world analysis as implemented in the system with transceiver channels available through SMA and popular backplane connectors. This development kit can be used for evaluation of transceiver link performance up to 28 Gbps, generation and checking pseudo-random binary sequence (PRBS) patterns via a simple to use GUI (does not require the Quartus II software), access advanced equalization to fine tune link settings for optimal bit error ratio (BER), perform jitter analysis, verify physical media attachment (PMA) interoperability with Stratix V GT FPGAs for targeted protocols, such as CEI-25/28G, CEI-11G, PCIe Gen 3.0, 10GBASE-KR, 10 Gigabit Ethernet, XAUI, CEI-6G, Serial RapidIO, HD-SDI, and others. You can use the built-in high speed backplane connectors to evaluate custom backplane performance and evaluate link BER.
	100G Development Kit, Stratix V GX Edition **Altera**	Stratix V GX 5SGXEA7N2F45C2N	This kit enables a thorough evaluation of 100G designs. It supports 10G/40G line interfaces through optical modules, and applications requiring external memory interfaces through four x18 QDR II and four x32 DDR3 memory banks. With this kit, you can evaluate transceiver performance up to 11.3 Gbps, verify PMA compliance to standards, such as 10G/40G/100G Ethernet, Interlaken, CEI-6G/11G, Serial RapidIO, PCIe (Gen1, Gen2, and Gen3), and other major standards. This kit can also validate interoperability between optical modules, such as SFP, SFP+, QSFP, and CFP.
	Arria V GX FPGA Development Kit, Arria V GX Edition **Altera**	Arria V GX 5AGXFB3H6F40C6N	This kit provides a full-featured hardware development platform for prototyping and testing high-speed serial interfaces to an Arria V GX FPGA. This kit includes two Arria V 5AGXFB3H6F40C6N FPGAs, the PCIe x8 form factor, two HSMC connectors, one FPGA mezzanine card (FMC) connector, 1,152 MB 72 bit DDR3 SDRAM, 4 MB 36 bit QDR II+ SRAM, flash memory, and two additional 32 bit DDR3 SDRAM devices. This kit also includes SMA connectors and a bull's-eye connector for differential transceiver I/Os.

Altera and Partner Development Kits

	Product and Vendor Name	Device	Description
I/O Interconnect (Continued)	Arria V GX Starter Kit, Arria V GX Edition **Altera**	Arria V GX 5AGXFB3H4F35C4	This kit provides a low-cost platform for developing transceiver I/O-based Arria V GX FPGA designs. This kit includes the PCIe x8 form factor, one HSMC connector, a 32 bit DDR3 SDRAM device, one-channel high-speed transceiver input and output connected to SMAs, HDMI output, SDI input and output, 16x2 LCD display, and flash memory.
	Cyclone V E FPGA Development Kit **Altera**	Cyclone V E 5CEFA7F31C7N	The Cyclone V E Development Kit offers a comprehensive general-purpose development platform for many markets and applications, including industrial, networking, military, and medical applications. The kit features an Altera Cyclone V device and a multitude of onboard resources including multiple banks of DDR3 and LPDDR2 memory, LCD character display, LEDs, user switches, USB, and RJ-45 connectors. The Cyclone V E Development Kit gives industrial equipment designers greater flexibility in implementing real-time Ethernet communications with Industrial Ethernet IP cores.
	Cyclone V GT FPGA Development Kit **Altera**	Cyclone V GT 5CGTFD9E5F35C7N	This kit can be used to prototype Cyclone V GT FPGA or Cyclone V GX FPGA applications. It offers a quick and simple way to develop low-cost and low-power system-level designs and achieve rapid results. This kit supports a myriad of functionalities, such as FPGA prototyping, FPGA power measurement, transceiver I/O performance up to 5 Gbps, PCIe Gen2 x4 (at 5 Gbps per lane), endpoint or rootport support.
	Arria II GX FPGA Development Kit, 6G Edition **Altera**	Arria II GX EP2AGX125F1152	This kit provides a full-featured hardware development platform for prototyping and testing high-speed serial interfaces to an Arria II GX FPGA up to 6 Gbps. This kit includes the PCIe x8 form factor, one HSMC connector, 128 MB 16 bit DDR3 SDRAM device, 1 GB 64 bit DDR2 SODIMM, 2 MB SSRAM, and 64 MB flash.
	Arria II GX FPGA Development Kit **Altera**	Arria II GX EP2AGX125F1152	This kit provides a full-featured hardware development platform for prototyping and testing high-speed serial interfaces to an Arria II GX FPGA. This kit includes the PCIe x8 form factor, one HSMC connector, 128 MB 16 bit DDR3 SDRAM device, 1 GB 64 bit DDR2 SODIMM, 2 MB SSRAM, and 64 MB flash.
	Stratix IV GX FPGA Development Kit **Altera**	Stratix IV GX EP4SGX230F1517	This kit provides a full-featured hardware development platform for prototyping and testing high-speed serial interfaces to a Stratix IV GX FPGA. This kit includes the PCIe x8 form factor, two HSMC connectors for expandability, and Ethernet, USB, SDI, and HDMI interfaces. Memory includes one x64 DDR3 SDRAM, one x16 DDR3 SDRAM, two x18 QDR II+ SRAM, flash, and SSRAM. This kit also includes two SMA connectors for a differential transceiver output. Several oscillators are available at 156.25 MHz,155.52 MHz, 125 MHz, 100 MHz, and 50 MHz. Other user interfaces include six user push buttons, eight DIP switches, eight user LEDs, 7-segment LCD display, and power and temperature measurement circuitry.
	Stratix IV GX FPGA Development Kit, 530 Edition **Altera**	Stratix IV GX EP4SGX530F1517	This kit provides a full-featured hardware development platform for prototyping and testing high-speed serial interfaces to a Stratix IV GX FPGA. This kit includes the PCIe x8 form factor, two HSMC connectors for expandability, and Ethernet, USB, SDI, and HDMI interfaces. Memory includes one x64 DDR3 SDRAM, one x16 DDR3 SDRAM, two x18 QDR II+ SRAM, flash, and SSRAM. This kit also includes two SMA connectors for a differential transceiver output. Several oscillators are available at 156.25 MHz,155.52 MHz, 125 MHz, 100 MHz, and 50 MHz. Other user interfaces include six user push buttons, eight DIP switches, eight user LEDs, 7-segment LCD display, and power and temperature measurement circuitry.
	100G Development Kit, Stratix IV GT Edition **Altera**	Stratix IV GT EP4S100G5F45I1N	This kit enables a thorough evaluation of 100G designs. It supports 10G/40G line interfaces through optical modules, and applications requiring external memory interfaces through four x18 QDR II and four x32 DDR3 memory banks. With this kit, you can evaluate transceiver performance up to 11.3 Gbps, verify PMA compliance to standards, such as 10G/40G/100G Ethernet, Interlaken, CEI-6G/11G, Serial RapidIO, PCIe (Gen1, Gen2, and Gen3), and other major standards. This kit can also validate interoperability between optical modules, such as small form factor pluggable (SFP), SFP+, quad small form factor pluggable (QSFP), and CFP.

Altera and Partner Development Kits

	Product and Vendor Name	Device	Description
I/O Interconnect (Continued)	Transceiver Signal Integrity Kit, Stratix IV GX Edition **Altera**	Stratix IV GX EP4SGX230F1517	This kit features eight full-duplex transceiver channels with SMA connectors, 156.25 MHz, 155.52 MHz, 125 MHz, 100 MHz, and 50 MHz clock oscillators, six user push buttons, eight dual in-line package (DIP) switches, eight user LEDs, a 7-segment LCD display, power and temperature measurement circuitry, and Ethernet, USB, and JTAG ports.
	Transceiver Signal Integrity Development Kit, Stratix IV GT Edition **Altera**	Stratix IV EP4S100G2F40I1N	This kit enables a thorough evaluation of transceiver interoperability and SERDES signal integrity by allowing you to evaluate transceiver performance up to 11.3 Gbps. You can generate and check pseudo-random binary sequence (PRBS) patterns via a simple-to-use GUI, change differential output voltage (V_{OD}), pre-emphasis, and equalization settings to optimize transceiver performance for your channel, perform jitter analysis, verify PMA compliance to 40G/100G Ethernet, Interlaken, CEI-6G/11G, PCIe -(Gen1, Gen2, and Gen3), Serial RapidIO, and other major standards, and validate interoperability between optical modules.
	Cyclone IV GX FPGA Development Kit **Altera**	Cyclone IV GX EP4CGX150DF31C7N	This kit provides a comprehensive design environment that allows you to quickly develop low-cost and low-power FPGA system-level designs. This kit includes the PCIe short card form factor, two HSMC connectors, and a 10/100/1000 Mbps Ethernet interface. Onboard memory includes 128 MB DDR2 SDRAM, 64 MB flash, and 4 MB SSRAM. This kit also includes SMA connectors, and 50 MHz, 100 MHz, and 125 MHz clock oscillators, as well as user interfaces including push buttons, LEDs, and a 7-segment LCD display.
	Cyclone IV GX Transceiver Starter Kit **Altera**	Cyclone IV GX EP4CGX15	This kit provides a low-cost platform for developing transceiver I/O-based FPGA designs. It includes the complete hardware and software you need to develop your FPGA design for cost-sensitive applications. You can measure the FPGA's power consumption, test the signal quality of the FPGA transceiver I/Os (up to 2.5 Gbps), and develop and test PCIe Gen1 designs.
	S5-6U-VPX (S56X) **BittWare**	Stratix V GX/GS	This rugged 6U VPX card is based on Altera's Stratix V GX/GS FPGAs and when combined with BittWare's Anemone FPGA coprocessor, the ARM Cortex-A8 control processor, and the ATLANTiS FrameWork FPGA development kit, it creates a flexible and efficient solution for high-performance signal processing and data acquisition. The board provides a configurable 48-port multi-gigabit transceiver interface supporting a variety of protocols, including Serial RapidIO, PCIe, and 10GbE. Additional I/O interfaces include Ethernet, RS-232, JTAG, and LVDS. The board features up to 8 GB of DDR3 SDRAM as well as flash memory for booting the FPGAs. Two VITA 57-compliant FMC sites provide additional flexibility for enhancing the board's I/O and processing capabilities.
	S5-PCIe-HQ (S5PH-Q) **BittWare**	Stratix V GX/GS	This half-length PCIe x8 card is based on Altera's Stratix V GX or GS FPGA and is a versatile and efficient solution for high-performance network processing, signal processing, and data acquisition. Combining it with BittWare's Anemone coprocessor and ATLANTiS FrameWork enhances productivity and portability, and allows even greater processing efficiency. Over 16 GB of onboard memory includes DDR3 SDRAM and QDR II/II+ SRAM. Two front-panel QSFP+ cages provide additional flexibility for serial I/O, allowing two 40GbE interfaces (or eight 10GbE), direct to the FPGA for reduced latency, making it ideal for high-frequency trading and networking applications.
	S5-PCIe (S5PE) **BittWare**	Stratix V GX/GS	This PCIe x8 card is based on Altera's Stratix V GX or GS FPGA and is designed for high-performance network processing, signal processing, and data acquisition. Combining it with BittWare's Anemone coprocessor and ATLANTiS FrameWork enhances productivity and portability and allows even greater processing efficiency. The board provides up to 32 GB of DDR3 SDRAM with optional ECC. An optional VITA 57 FMC site provides additional flexibility for enhancing the board's I/O and processing capabilities, making it ideal for analog I/O and processing. The board also has the option of two front-panel QSFP+ cages for serial I/O, which support 10G per lane direct to the FPGA for reduced latency, making it ideal for high frequency trading and networking applications. It is also available with A/D and D/A conversion options.

Altera and Partner Development Kits

	Product and Vendor Name	Device	Description
I/O Interconnect (Continued)	PROCe V **GiDEL**	Stratix V GX/GS (Gen3 x8) 5SGXMA3K2F40C3N 5SGXMA7K2F40C2N 5SGSMD8K2F40C2N	This half-length PCIe x8 card is based on Altera's Stratix V GX or GS FPGA and is a versatile and efficient solution for high-performance network processing, signal processing, and data acquisition. Combining it with GiDEL's PROCWizard software and data management IP cores, enhances productivity and portability, and allows even greater processing efficiency. The platform features 16+ GB of onboard memory includes DDR3 SDRAM and SRAM. Typical sustain throughput of 8,000 GBps for internal memories and 25+ GBps for onboard memory. Networking capabilities include one CXP connector cage suitable for 100GbE Ethernet (100GBASE-CR10, 100GBASE-SR10), 3×40 GbE, or single Infiniband 12×QDR link, two SFP+ cage suitable for 10 GbE, and Optical Transport Network. Additional I/O interfaces, 2× high-speed inter-board connectors (up to 12×14.1Gb/s full duplex GPIO) for board to board and proprietary daughterboards connectivity.
	ProcFG **GiDEL**	Stratix V GX Stratix IV E Stratix III L/E	This kit is based on Altera's Stratix FPGA. It is used for development of vision algorithms, machine vision, and medical imaging applications. ProcFG combines high-speed acquisition, powerful FPGA processing with selective on-the-fly ROI offloading for convenient processing on standard PC. The ProcFG captures all incoming image data or dynamically targets and extracts ROIs based on real-time FPGA analysis of the incoming data, and supports acquisition from both line and area scan cameras.
	S4-3U-VPX (S43X) **BittWare**	Stratix IV GX	This commercial or rugged 3U VPX card is based on Altera's Stratix IV GX FPGA that is designed specifically for serial I/O-based applications, creating a completely flexible, reconfigurable VPX board. BittWare's ATLANTiS FrameWork and the FINe Host/Control Bridge greatly simplify application development and integration of this powerful board. The board provides a configurable 25-port SERDES interface supporting a variety of protocols, including Serial RapidIO, PCIe, and 10GbE. The board also features 10/100/1000 Ethernet, and up to 4 GB of DDR3 SDRAM. The VITA 57-compliant FMC site provides enhanced flexibility, which supports 10 SERDES, 60 LVDS pairs, and 6 clocks.
	SP/D4-AMC (D4AM) **BittWare**	Stratix IV	This board features the I/O processing power of two Altera Stratix IV FPGAs and is a mid- or full-size, single-width AdvancedMC that can be attached to AdvancedTCA carriers or other cards equipped with AMC bays, and used in MicroTCA systems. An Altera Stratix IV GX FPGA paired with a Stratix IV E FPGA makes the D4AM an extremely high-density, flexible board. The FPGAs are connected by two full-duplex 2 GB per second lanes of parallel I/O for data sharing. Each FPGA supports BittWare's ATLANTiS FrameWork to greatly simplify application development and integration. A VITA 57-compliant FMC site provides enhanced flexibility, which connects directly to the Stratix IV E FPGA for LVDS and to the Stratix IV GX FPGA for SERDES. The board also provides an IPMI system management interface and a configurable 18-port AMC SERDES interface supporting a variety of protocols. Onboard memory includes up to 1 GB of DDR3 SDRAM and 128 MB of flash memory, and Ethernet is available via the AMC front and rear panels. It is also available with A/D and D/A conversion options.
	SP/S4-AMC (S4AM) **BittWare**	Stratix IV GX	This board is based on Altera's Stratix IV FPGA and is a mid- or full-size, single-width AdvancedMC that can be attached to AdvancedTCA carriers or other cards equipped with AMC bays, and used in MicroTCA systems. The S4AM features a high-density, low-power Altera Stratix IV GX FPGA designed specifically for serial I/O-based applications, creating a completely flexible, reconfigurable AMC. Providing enhanced flexibility is the VITA 57-compliant FMC site, which features 8 SERDES, 80 LVDS pairs, and 6 clocks directly to the FPGA. BittWare's ATLANTiS FrameWork, in conjunction with the FINe III Host/Control Bridge, greatly simplifies application development and integration of this powerful board. The board also provides an IPMI system management interface, a configurable 15-port AMC SERDES interface supporting a variety of protocols, and a front panel 4x SERDES interface supporting CPRI and OBSAI. Additionally, the board features 10/100 Ethernet, GbE, two banks of DDR3 SDRAM, two banks of QDR II+ SRAM, and flash memory for booting the FPGAs and FINe. It is also available with A/D and D/A conversion options.

Altera and Partner Development Kits

	Product and Vendor Name	Device	Description
I/O Interconnect (Continued)	4S-XMC (4SXM) **BittWare**	Stratix IV GX	This is a single-width switched mezzanine card (XMC), designed to provide powerful FPGA processing and high-speed serial I/O capabilities to VME, VXS, VPX, cPCI, AdvancedTCA, or PCIe carrier boards. The 4SXM features a high-density, low-power Altera Stratix IV GX FPGA, which was designed specifically for serial I/O-based applications and is PCI-SIG® compliant for PCIe Gen1 and Gen2. Four SFP compact optical transceivers are available on the front panel. There are 8 multi-gigabit serial lanes supporting PCIe, Serial RapidIO, and 10GbE available via the board's rear panel, as well as 44 general-purpose digital I/O signals. The 4SXM also provides QDR II+ SRAM and flash memory.
	S4GX-AMC **BittWare**	Stratix IV GX EP4SGX230F1517	This board is based on Altera's Stratix IV GX FPGA and is a mid-size, single-width AdvancedMC that can be attached to AdvancedTCA carriers or other cards equipped with AdvancedMC bays, and used in MicroTCA systems. This board has two banks of DDR3 SDRAM (up to 1 GB each), and two banks of QDR II SRAM (up to 9 MB). Includes IP support for Serial RapidIO, PCIe, GbE, 10G Ethernet (XAUI), CPRI, and OBSAI interfaces.
	ProcE **GiDEL**	EP4S820E EP3S340L EP2S60F1020C4N	This Altera-based PCIe x4 platform is ideal for high-speed data acquisition, algorithmic acceleration, IP validation, and verification of small SoCs. This board has five levels of memory structure (8.5 GB+) with maximum sustain throughput of 4,693 GBps for internal memories and 12 GBps for DRAM.
	Stratix IV GX/GT 40G/100G Interlaken **HiTech Global**	Stratix IV EP4S100G5 EP4SGX530	This board integrates the most fundamental electrical and optical interfaces for building 200G subsystems. It implements CAUI and Interlaken high-speed serial interfaces, industry-leading, high-speed DDR3 SDRAM and QDR II+ SRAM interfaces, and high-speed parallel interconnect for NetLogic knowledge-based processors (KBPs). The modular design enables expansion to support legacy and emerging optical modules.
	Xpress GX4 Kit **PLDA**	Stratix IV GX EP4SGX230KF40C2N	This kit provides a complete hardware and software environment for Altera Stratix IV GX FPGAs. It is built around a PCI form factor card compliant with PCI-SIG and targets the development of designs using PCIe Gen1 or Gen2.
	Xpress AGX2 Kit **PLDA**	Arria II GX EP2AGX125EF35	This kit provides a complete hardware and software environment for Altera Arria II GX FPGAs. It is built around a PCI form factor card compliant with PCI-SIG and targets the development of designs using PCIe Gen1.
	C3 Digital Radio Kit **CEPD**	Cyclone III EP3C16	This kit aids the development and testing of algorithms and signal processing applications including digital radio, modulator/demodulator development, software-defined radio, high-speed data acquisition and signal processing, and audio data acquisition and signal processing. The acquired signals are sampled and then digitally processed by a Cyclone III FPGA. The FPGA card comes with a JTAG programming connector and a configuration PROM to retain the FPGA settings. The PCI card provides interfaces for the FPGA card to a computer PCI bus, RS232 interface, and user push buttons and includes a digital radio reference design example and full documentation.
	Cyclone III FPGA/PCI Development Board **CEPD**	Cyclone III EP3C16F484C8N	This board provides a platform for fast and easy prototyping and design verification with the Cyclone III EP3C16F484C8N FPGA. It can be accessed either through the PCI bus or powered as a stand-alone system and accessed through an RS232 port. It comes with an onboard configuration PROM to retain the FPGA settings, an RS232 level shifter, voltage monitor, oscillator, buttons, and LEDs. There is a prototyping area on the board for user circuits and all FPGA pins are accessible through connectors and clearly labeled test points. The connectors are designed to mate with other CEPD daughterboards.
	SuperUSBC3-55 **PLDA**	Cyclone III EP3C55U484C6N	This kit provides a low-cost hardware and software environment for prototyping and deploying SuperSpeed USB applications. It targets the Altera Cyclone III FPGA (EP3C55F484C6N) and includes everything you need to implement a complete USB 3.0 subsystem.

Altera and Partner Development Kits

	Product and Vendor Name	Device	Description
I/O Interconnect (Continued)	PCI-X Development Board **Terasic Technologies, Inc.**	Cyclone III FPGA	This board provides a hardware platform for developing and prototyping low-power, high-performance, logic-intensive PCI-based designs on an Altera Cyclone III FPGA. External memory is provided to facilitate the development of designs that need extra storage capacity or higher bandwidth memory. It also includes a LVDS interface using high-speed Terasic connectors (HSTCs) for high-speed interface applications.
	QuickUSB Starter Kit **Bitwise Systems**	Cyclone II EP2C20F256C7	This kit includes one QuickUSB module and one QuickUSB Cyclone II Evaluation Board. The evaluation board has a QuickUSB module site on headers that provide access to the signals. The EP2C20F256C7 FPGA connects to nearly every pin of the QuickUSB module, and extra I/O pins go to the headers so you can wire in your circuitry. The kit gets its power from the USB bus, but if you need more power, there is a power connector and a 5V 2A power supply included in the kit.
	HD FIFO Modules **Averlogic**	Daughtercard	This board is designed for evaluating the AL460A HD-FIFO. It has two embedded AL460A-7-PBF (or AL460A-13-PBF) devices operating in parallel, expanding the bus width to 32 bits. Control signals and data bus signals are available on two 50-pin connectors. A separate adaptor board (HSMC interface) is available for connecting the module directly to a Cyclone III FPGA Starter Kit.
	Broadcast Video Card **Bitec**	Daughtercard	This card is designed for professional video equipment developers. The dual ASI/SD-SDI interfaces allow access to industry-standard video transport signals. Based on the latest adaptive cable equalizers and drivers, the ASI/SDI interfaces provide excellent noise immunity up to cable lengths of 350 meters. A voltage-controlled crystal oscillator (VCXO) allows precise synchronization to incoming ASI signals. A DVB-T reference design using the Bitec BVDC daughtercard and a Cyclone III FPGA Development Kit is available.
	Quad Video Board **Bitec**	Daughtercard	This board is based on the Texas Instruments TVP5154 quad video decoder. The analog video inputs include composite video and S-video. Video output is based on the Chrontel CH7010B device, enabling single-link DVI, component analog, and composite analog outputs. The device accepts digital, parallel video data, and clocking from the host FPGA via the HSMC connector, which configures and monitors the device over an I^2C link. A DVI output connector and mini-DIN output connector are provided.
	HDMI Receiver/Transmitter **Microtronix**	Daughtercard	This daughtercard interfaces a HDMI receiver and transmitter to your Altera FPGA development kit using the HSMC expansion connector. The receiver also supports an analog component video (YCbCr) interface. The card uses the Analog Devices AD9889 HDMI Transmitter and AD9880 HDMI Receiver to support HDTV formats up to 1080p at 60 Hz. The receiver offers the flexibility of both an analog interface and an HDMI receiver integrated on a single chip.
	Quad Link LVDS Interface **Microtronix**	Daughtercard	This daughtercard supports receive and transmit LVDS links, each consisting of five data channels and one clock for a total of 48 LVDS channels. The standard configuration of 20 TX + 4 clk and 20 RX + 2 clk, is capable of supporting LCD display panels up to 1080p at 100/120 Hz. Onboard LVDS termination resistors can be removed to convert receiver channels into transmitters as required to support 12 bit or 14 bit color applications. It is used for capturing LVDS video data, connecting to a camera link interface, or for connecting to LCD panels using LVDS, mini-LVDS, RSDS, and PPDS low-voltage panel interface signaling.
	Ethernet USB Expansion Kit **Microtronix Inc.**	Daughtercard	This kit includes a wireless 802.11b CompactFlash card and a Microtronix CompactFlash board.
	I^2C Design Kit **Microtronix Inc.**	Daughtercard	This kit provides an easy way to design, develop, and test the Microtronix I^2C IP core.
	10/100/1000 Ethernet PHY Daughter Board with Marvell PHY **MorethanIP**	Daughtercard	This kit provides the ability to implement high-speed Ethernet PHY solutions for prototyping and evaluation and embedded software development.

Altera and Partner Development Kits

	Product and Vendor Name	Device	Description
I/O Interconnect (Continued)	10/100/1000 Ethernet PHY Daughter Board with Texas Instruments PHY **MorethanIP**	Daughtercard	This kit provides the ability to implement fast Ethernet solutions for prototyping and evaluation and embedded software development.
	CX4 to HSMC Adapter **MorethanIP**	Daughtercard	This passive daughtercard for 10GbE CX-4 copper interconnect prototyping features a four-lane differential 3.125 Gbps connector (CX-4) for 10GbE IEEE 802.3ak, a 160-pin HSMC to the main board, and compatibility with Stratix II GX mother boards that use HSMC connectors.
	SFP HSMC **Terasic Technologies, Inc.**	Daughtercard	This SFP HSMC is for the development of SGMII Ethernet, Fibre Channel, CPRI/ OBSAI, and SONET designs based on transceiver-based host boards with HSMC connectors.
Embedded	Arria V SoC Development Kit and SoC Embedded Design Suite **Altera**	Arria V SoC 5ASTFD5K3F40I3NES	The Altera Arria V SoC Development Kit offers a quick and simple approach to develop custom ARM processor-based SoC designs. Altera's midrange, transceiver-based Arria V FPGA fabric provides the highest bandwidth with the lowest total power for midrange applications such as remote radio units, 10G/40G line cards, medical imaging, broadcast studio equipment, and the acceleration of image- and video-processing applications. This development kit includes the SoC Embedded Design Suite software development tools. The development board has PCIe Gen2 x4 lanes (endpoint or rootport), two FMC expansion headers, dual Ethernet PHYs, and various DRAM and flash memories.
	Cyclone V SoC Development Kit **Altera**	Cyclone V SoC 5CSXFC6D6F31C8NES	The Altera Cyclone V SoC Development Kit offers a quick and simple approach to develop custom ARM processor-based SoC designs accompanied by Altera's low-power, low-cost Cyclone V FPGA fabric. This kit supports a wide range of functions, such as processor and FPGA prototyping and power measurement, industrial networking protocols, motor control applications, acceleration of image- and video-processing applications, PCIe x4 lane with ~1,000 MBps transfer rate (endpoint or rootport).
	Cyclone V GT FPGA Development Kit **Altera**	Cyclone V GT 5CGTFD9E5F35C7N	This kit can be used to prototype Cyclone V GT FPGA or Cyclone V GX FPGA applications. It offers a quick and simple way to develop low-cost and low-power system-level designs and achieve rapid results. This kit supports a myriad of functionality, such as FPGA prototyping, FPGA power measurement, transceiver I/O performance up to 5.0 Gbps, PCIe Gen2 x4 (at 5.0 Gbps per lane), endpoint or rootport support.
	Cyclone V E FPGA Development Kit **Altera**	Cyclone V E 5CEFA7F31C7N	The Cyclone V E Development Kit offers a comprehensive general-purpose development platform for many markets and applications, including industrial, networking, military, and medical applications. The kit features an Altera Cyclone V device and a multitude of onboard resources, including multiple banks of DDR3 and LPDDR2 memory, LCD character display, LEDs, user switches, USB, and RJ-45 connectors. The Cyclone V E Development Kit gives industrial equipment designers greater flexibility in implementing real-time Ethernet communications with Industrial Ethernet IP cores.
	Nios II Embedded Evaluation Kit, Cyclone III Edition[1] **Altera**	Cyclone III EP3C25N	This kit includes a complete hardware and software design environment for a 32 bit microcontroller plus FPGA evaluation. Beginners can check out the pre-built, eye-catching demos displayed on the LCD touch screen or do some lightweight development. Advanced microcontroller designers can learn about the latest techniques, multiprocessor systems, or about designing a complete system in 30 minutes.

Altera and Partner Development Kits

	Product and Vendor Name	Device	Description
Embedded (Contniued)	Cyclone III FPGA Development Kit **Altera**	Cyclone III EP3C120N	This kit contains 8 MB SSRAM, 256 MB DDR2 SDRAM, 64 MB flash, configuration via USB, 10/100/1000 Ethernet and USB ports, onboard oscillators and SMAs, graphics LCD and character LC displays, two HSMC expansion connectors, three HSMC debug cards, and onboard power measurement circuitry. Complete documentation including reference designs: *Create Your First FPGA Design in an Hour* and *Measure Cyclone III FPGA Power.* This kit also includes Quartus II Web Edition design software, an evaluation edition of Nios II processor plus related design suite, and the Altera IP library.
	Nios II Development Kit, Cyclone III Edition[1] **Altera**	Cyclone III EP3C120N	The unique combination of high-performance embedded processor power and easy-to-use integrated design software has been updated to take advantage of Cyclone III devices, the industry's lowest cost, first-to-market 65 nm FPGA family. This development kit provides an ideal environment for developing and prototyping a wide range of price-sensitive, high-performance embedded applications.
	PROC104 **GiDEL**	Stratix IV E Stratix III L Stratix III E	This is a PCIe/104 standard Altera-based platform incorporating compact, self-stacking, and rugged industrial-standard connectors. This powerful platform is ideal for high-performance FPGA development and deployment across a range of size, weight, and power-constrained (SWaP-constrained) application areas, including signal intelligence, image processing, software-defined radio, and autonomous modules, or vehicles. The PROC104 can be hosted via 4-lane PCIe and is stackable. The board's high-speed performance coupled with memory and add-on daughterboards' flexible architecture enable the system to meet almost any computational needs. In addition to 512 MB onboard memory, two SODIMM sockets provide up to 8 GB of memory.
	PROCStar IV **GiDEL**	Stratix IV EP4SE530H35C2N (1 - 4 FPGAs)	This full-length PCIe x8 card is based on Altera's Stratix IV E FPGAs. It provides a high-capacity, high-speed FPGA-based platform fortified with high throughput and massive memory resulting in a powerful and highly flexible system. The performance, memory, and add-on daughterboards' flexible architecture enable the system to meet almost any computation needs. In addition to 2 GB onboard memory, 8 SODIMM sockets provide up to 32 GB of memory or additional connectivity and logic. The largest FPGA-based supercomputer at the National Science Foundation Center for High-Performance Reconfigurable Computing (NSF CHREC) center houses 100 of these cards (400 Altera FPGAs) and is used for Bio-RC, HFT, data mining, and seismic analysis applications.
	BeMicro SDK **Arrow**	Cyclone IV E EP4CE22F17C7N	This Arrow BeMicro SDK enables a quick and easy evaluation of soft core processors for both embedded software developers and hardware engineers. The kit builds on the success of the original BeMicro evaluation kit by adding features, such as Mobile DDR memory, Ethernet, and even the option of using a file system by slotting in a micro-SD card. The BeMicro SDK connects to a PC via a USB connection, which is used for power, programming, and debug. Arrow has a number of reference designs and pre-built software templates that can be downloaded for this kit that highlight the benefits of building embedded systems in FPGAs.
	Industrial Networking Kit **Terasic Technologies, Inc.**	Cyclone IV E EP4CE115	The Industrial Networking Kit (INK) offers a comprehensive development platform for industrial automation and applications. The kit consists of the DE2-115 board featuring the Altera Cyclone IV device and dual 10/100/1000-Mbps Ethernet, 128 MB SDRAM, 8 MB flash memory, 2 MB SRAM, HSMC and GPIO connectors, USB 2.0, an SD card slot, switches and buttons, LEDs, 16x2 display, audio and video, and VGA-out. The kit also includes an Industrial Communications Board (ICB-HSMC) that supports RS-485, RS-232, CAN, and additional I/O expansion.

[1] RoHS compliant.

Altera and Partner Development Kits

	Product and Vendor Name	Device	Description
Embedded (Contniued)	ProcCamSim **GiDEL**	Stratix III EP3SE80-F1152-C2	ProcCamSim is a development kit based on Altera's Stratix III E FPGAs. It is a high-performance camera or machine simulator, that generates video and test patterns to a frame grabber supporting all the Camera Link v1.1 specification (base, medium, and full) configurations. Typical applications include vision algorithms development, image processing, application testing, machine vision integration, vision system reliability testing and debug of "rarely appearing bugs." The development kit supports Bitmap Image File (**.bmp**) and raw image files and enables video simulation via streaming of **.bmp** or raw images.
	ARM-MPS **Gleichmann Electronics**	Stratix III	This platform offers total flexibility for prototyping your ARM Cortex-M3-based designs. It allows unrestricted access to the latest ARM Cortex-M-class processors. It is delivered with a comprehensive range of tools that allow fast and easy system design—drag and drop the supplied IP components to configure the system, or implement your own system blocks. Then synthesize the design and update the board with a single mouse-click. The tool suite also includes system configuration utilities and a JTAG signal monitor together with software development tools and a JTAG debug probe.
	Low-Power Reference Platform **Arrow**	Cyclone III EP3C25 MAX IIG EPM240T100	This platform uses the low-power Altera Cyclone III FPGAs and MAX IIG CPLDs. It demonstrates how to minimize power consumption in portable and battery-powered embedded systems and gives you the flexibility to create application-specific low-power solutions.
	CMCS002M Controller FPGA Module **Dallas Logic**	Cyclone III EP3C25	This module allows you to implement general logic functions and Nios II processor operations in a compact form factor module. The module uses the Cyclone III EP3C25 FPGA, 512K x8 SRAM, EP1S16 FPGA serial loader (FPGA and Nios II processor boot), and a USB 2.0 peripheral port (low-/full-speed operation). This module also supports the Cardstac specification (master or slave standard card, 128 pins), and can interface with other modules designed to that specification.
	Lancelot VGA IP Design Kit **Microtronix Inc.**	Daughtercard	This kit includes a small hardware board with a 24 bit RAMDAC, VGA connector, stereo audio connector, and two PS/2 connectors.
	Compact Flash Expansion Kit **Microtronix Inc.**	Daughtercard	This inexpensive module allows the addition of compact flash cards to the Microtronix Product Starter Kit development board system.

Altera and Partner Development Kits

	Product and Vendor Name	Device	Description
ASIC Prototyping	Stratix IV E FPGA Development Kit **Altera**	Stratix IV E EP4SE530	This kit allows rapid and early development of designs for high-performance Stratix IV FPGAs. The development board provides general I/Os that connect to onboard switches and indicators, and to the included two-line LCD and 128 x 64 graphics display. The board also has non-volatile and volatile memories (64 MB flash, 4 MB pseudo-SRAM, 36 Mb QDR II SRAM, 128 MB DDR2 DIMM, and 16 MB DDR2 device), HSMC, and 10/100/1000 Ethernet interfaces. The kit is delivered with Quartus II software and all of the cabling required to start using the board straight out of the box.
	Stratix III FPGA Development Kit **Altera**	Stratix III EP3SL150	This kit allows rapid and early development of designs for high-performance Stratix III FPGAs. The development board provides general I/Os that connect to onboard switches and indicators, and to the included two-line LCD and 128 x 64 graphics display. The board also has non-volatile and volatile memories (64 MB flash, 4 MB pseudo-SRAM, 36 Mb QDR II SRAM, 128 MB DDR2 DIMM, and 16 MB DDR2 device), HSMC, and 10/100/1000 Ethernet interfaces. The kit is delivered with Quartus II software and all of the cabling required to start using the board straight out of the box.
	ProcSoC3-4S system **GiDEL**	Stratix IV EP4SE820F43C3	PROC_SoC Verification System provides scalability of multiple interconnected FPGA modules, enabling verification of SoC designs from 6 million to 360 million equivalent ASIC gates. Each ProcSoC module itself is a modular and scalable SoC verification system. Fast GbE connection combined with GiDEL's development tools enable it to run the target software or regression suites via remote servers connected to the SoC/ASIC design. The remote operation is performed at near actual system speed allowing for hardware-software integration and co-verification. Two chassis configurations are available, ProcSoC3 and ProcSoC10, capable of supporting up to 3 or 10 PROC12M boards, respectively. Each ProcSoC system can prototype a single SoC or be partitioned to prototype multiple designs in parallel. The ProcSoC's unique interconnectivity topology enables any FPGA to connect directly to any other FPGA in the system even in large systems.
	ProcE **GiDEL**	Stratix IV, III EP4S820E EP3S340L	This Altera-based PCIe x4 platform is ideal for high-speed data acquisition, algorithmic acceleration, IP validation, and verification of small SoCs. This board has five levels of memory structure (8.5 GB+) with maximum sustain throughput of 4,693 GBps for internal memories and 12 GBps for DRAM.
	Single-FPGA (Tile) Prototyping Solution **Polaris Design Systems**	Stratix IV	This single-FPGA prototyping board can accommodate up to 15 million gate designs. It has a single Stratix IV FPGA and 18 Mb of SRAM. The board can be used either in a rack-mountable system or as a stand-alone unit.
	Multi-FPGA (Logic) Prototyping Solution **Polaris Design Systems**	Stratix IV	This multi-FPGA prototyping board can accommodate up to 30 million gate designs. The board has three Stratix IV FPGAs, SRAM, and 2 GB of DDR3 SDRAM (expandable to 8 GB). The board can be used either in a rack-mountable system or as a stand-alone unit.
	DN7002k10MEG **The Dini Group**	Stratix IV EP4SE820F43CxN EP4SE530F43CxN	This complete logic emulation system allows you to prototype SoC logic and memory designs. It can operate as a stand-alone system, or be hosted via a USB interface. A single system, configured with two Stratix IV EP4SE820 FPGAs, can emulate up to 13 million gates. All FPGA resources are available for the target application. Each FPGA position can use any available speed grade.

Altera and Partner Development Kits

	Product and Vendor Name	Device	Description
ASIC Prototyping (Contniued)	DN7406k10PCIe-8T **The Dini Group**	Stratix IV EP4SE820F43CxN EP4SE530F43CxN	This complete logic prototyping system allows you to prototype logic and memory designs. The DN7406k10PCIe-8T is hosted in an eight-lane PCIe Gen1 bus, but can be used as a stand-alone system configured via USB or CompactFlash. A single board configured with six Altera Stratix IV EP4SE820 FPGAs can emulate up to 31 million gates. All of the FPGA resources are available for your application, and any combination of speed grades can be used.
	DN7020k10 **The Dini Group**	Stratix III Stratix IV	This complete logic prototyping system gives ASIC and IP designers a vehicle to prototype logic and memory designs using up to 20 Stratix III or Stratix IV devices.
	DN7006K10PCIe-8T **The Dini Group**	Stratix III Stratix IV	This complete logic prototyping system with a dedicated PCIe interface gives ASIC and IP designers a vehicle to prototype logic and memory designs using up to six Stratix III or Stratix IV devices.
	DIGILAB SX III **El Camino GmbH**	Stratix III	This universal FPGA prototyping platform based on Altera's largest Stratix III devices supports 2 MB flash, 2 MB SRAM, four Samtec expansion connectors, two Mictor connectors, user LEDs, and push buttons along with RS-232, SPI, and USB interfaces.
	ProcStar III **GiDEL**	Stratix III	This system provides high-capacity, high-speed, multi-FPGA-based prototyping and end system platforms.
General Purpose	Stratix V Advanced Systems Development Kit **Altera**	Stratix V 2x 5SGXEA7N-2F45C2N	This kit is a complete systems design environment that includes both the hardware and software needed to begin architecture development and system design using Stratix V FPGA designs. The PCIe-based form-factor utilizes a x16 edge connector, and includes high memory bandwidth to DDR3, QDR II+, and serial memory. Multiple high-speed protocols are accessible through FMC and HSMC connections.
	Cyclone V GT FPGA Development Kit **Altera**	Cyclone V GT 5CGTFD9E5F35C7N	This kit can be used to prototype Cyclone V GT FPGA or Cyclone V GX FPGA applications. It offers a quick and simple way to develop low-cost and low-power system-level designs and achieve rapid results. This kit supports a myriad of functionality, such as FPGA prototyping, FPGA power measurement, transceiver I/O performance up to 5 Gbps, and PCIe Gen2 x4 (at 5 Gbps per lane), endpoint or rootport support.
	Cyclone V E FPGA Development Kit **Altera**	Cyclone V E 5CEFA7F31C7N	The Cyclone V E FPGA Development Kit offers a comprehensive general-purpose development platform for many markets and applications, including industrial, networking, military, and medical applications. The kit features an Altera Cyclone V device and a multitude of onboard resources including multiple banks of DDR3 and LPDDR2 memory, LCD character display, LEDs, user switches, USB, and RJ-45 connectors. The Cyclone V E Development Kit gives industrial equipment designers greater flexibility in implementing real-time Ethernet communications with Industrial Ethernet IP cores.
	MAX V CPLD Development Kit **Altera**	MAX V 5M570Z	This low-cost platform will help you quickly begin developing low-cost, low-power CPLD designs. Use this kit as a stand-alone board or combined with a wide variety of daughtercards that are available from third parties.
	Cyclone III FPGA Starter Kit[1] **Altera**	Cyclone III EP3C25N	This kit contains 1 MB SSRAM, 16 MB DDR SDRAM, 16 MB parallel flash, configuration via USB, four user push buttons, four user LEDs, and power measurement circuitry. Complete documentation including reference designs: *Create Your First FPGA Design in a Hour*, *Measure Cyclone III FPGA Power*, and *Create Your First Nios II Design*. This kit also includes Quartus II Web Edition design software, the evaluation edition of Nios II processor plus related design suite, and Altera IP library.
	Cyclone III LS FPGA Development Kit **Altera**	Cyclone III LS EP3CLS200F780C7N	This kit combines a high-density, low-power Cyclone III LS FPGA with a complete suite of security features implemented at the silicon, software, and IP levels. These security features provide passive and active protection of your IP from tampering, reverse engineering, and counterfeiting. It uses the EP3CLS200 FPGA—200K LEs at less than 0.25 W static power.

[1] RoHS compliant.

Altera and Partner Development Kits

	Product and Vendor Name	Device	Description
General Purpose (Continued)	DE2-115 Development and Education Board **Terasic Technologies, Inc.**	Cyclone IV E EP4CE115	This board is part of the DE2 educational development board series and features the Cyclone IV E EP4CE115 FPGA. The DE2-115 offers an optimal balance of low-cost, low-power and a rich supply of logic, memory and DSP capabilities, as well as interfaces to support mainstream protocols including GbE. A HSMC connector is provided to support additional functionality and connectivity via HSMC daughtercards and cables.
	Hpe-midiv2 **Gleichmann Electronics**	Stratix III EP3SL150	This complete development environment provides a large number of onboard PHY and a range of child boards with various auxiliary functions for developing large and complex systems. It consists of a motherboard with the latest Stratix III FPGA modules and all of the latest interfaces on a single platform. It comes with a GUI for access to a set of free tools including system configuration utilities, JTAG debugger and scanner, and clock factory programmer.
	Video Development Kit **Bitec**	Cyclone III FPGA	This kit contains the Cyclone III FPGA Development Kit and two HSMC video interface cards together with a collection of IP cores and reference designs. The kit provides a variety of video interface standards including both digital and analog up to HD resolutions.
	ViClaro III HD Video Enhancement Development Platform **Microtronix**	Cyclone III FPGA	This video enhancement development platform supports 100/120-Hz HDTV that is 1080p bandwidth-capable and features 32 bit DDR2 SDRAM memory, a HDMI transmitter, an analog/HDMI receiver, and dual LVDS links.
	DE0 Development Board **Terasic Technologies, Inc.**	Cyclone III EP3C16F484C6N	This board provides all the essential tools for you to learn about digital logic and FPGAs. It is equipped with an Altera Cyclone III EP3C16 FPGA, which offers 15,408 LEs. The board provides 346 user I/O pins and is loaded with a rich set of features. It is suitable for advanced university and college courses as well as the development of sophisticated digital systems, and includes software, reference designs, and accessories.
	CoreCommander Development Kit **System Level Solutions**	Cyclone III EP3C25F256C8	This kit features the Altera Cyclone III FPGA that provides more than enough room for almost any embedded design. This flexible board comes with a suite of SLS IP Cores, drivers, and application software. Delivered as a complete package, this kit ensures quick and easy implementation of industry-leading cores with reduced risk, at a very low cost.
	ProcPAK II **GiDEL**	Cyclone II EP2C35	ProcPAK II development kit is based on Altera's Stratix II FPGA platform. The development kit greatly improves time to market. There is no need to design the board, the PCI driver, or the application driver layer, define board constraints, design memory controller, and write environment FPGA code. This kit enables designers to focus on their proprietary value-added design instead of spending their valuable effort to recreate standard design components. With ProcMultiPort innovative memory controller, the generated HDL code enables high-speed, easy-to-use parallel access to large memories.
	DE1 Development Board **Terasic Technologies, Inc.**	Cyclone II EP2C20 FPGA	This board is a smaller version of the DE2 board. It is useful for learning about digital logic and FPGAs. Featuring an Altera Cyclone II EP2C20 FPGA, it is designed for university and college laboratory use, and is suitable for a wide range of exercises in courses on digital logic and computer organization.
	DE2 Development Board **Terasic Technologies, Inc.**	Cyclone II EP2C35 FPGA	This board was designed by professors, for professors. It is an ideal vehicle for learning about digital logic and FPGAs. Featuring an Altera Cyclone II EP2C35 FPGA, the DE2 board is designed for university and college laboratory use. It is suitable for a wide range of exercises in courses on digital logic and computer organization.

Altera and Partner Development Kits

	Product and Vendor Name	Device	Description
General Purpose (Continued)	DE2-70 Digital Camera and Multimedia Development Platform **Terasic Technologies, Inc.**	Cyclone II EP2C70F896C6N	This board is a modified version of the Altera DE2 board with a larger FPGA and more memory. It is an excellent vehicle for learning about digital logic and FPGAs. Featuring an Altera Cyclone II EP2C70 FPGA, the DE2 board is designed for university and college laboratory use.
	MAX II/MAX IIZ Development Kit **System Level Solutions**	MAX II EPM240 EPM240Z	This board provides a hardware platform for designing and developing simple and low-end systems based on Altera MAX II/MAX IIZ devices. The board features a MAX II/MAX IIZ EPM240T100Cx/EPM240ZM100Cx device with 240 LEs and 8,192 bits of user flash memory (UFM). The board also supports vertical migration into EPM570T100Cx devices with 570 LEs and 8,192 bits of UFM.
	MAX II Micro **Terasic Technologies, Inc.**	MAX II CPLD EPM2210F324C3	This kit, equipped with the largest Altera Max II CPLD and an onboard USB-Blaster cable, functions as a development and education board for CPLD designs. This kit also includes reference designs with source code.
	HSMC Prototyping Board **Bitec**	Daughtercard	This board provides a solution for prototyping circuits and testing them together with the latest Altera FPGA development kits. This board provides access to the complete set of HSMC signals via a footprint of standard 0.1" pitch headers. The HSMC power pins are accessed via fuses for added security. The main prototype matrix comprises a 0.1" grid interleaved with +3.3 V and GND access points. Footprints for commonly used 25-way and 9-way D-type connectors are included on the board.
	HSMC DVI Input/Output Module **Bitec**	Daughtercard	This DVI transmitter/receiver module for the HSMC interface enables you to interface FPGA projects to real-world DVI signals.
	SC DVI Input Module **Bitec**	Daughtercard	This DVI module for the Santa Cruz interface enables you to interface FPGA projects to real-world DVI signals.
	SC DVI Output Module **Bitec**	Daughtercard	This DVI module for the Santa Cruz interface enables you to drive high-resolution displays with digital clarity.
	SC Camera **Bitec**	Daughtercard	This board features a 5.2-megapixel camera daughtercard with selectable frame rates and resolutions.
	SC Proto **Bitec**	Daughtercard	This prototyping board for the Santa Cruz interface has convenient access points to power and ground with connector break-out.
	TRDB_DC2 1.3 Megapixel Camera Module **Terasic Technologies, Inc.**	Daughtercard	This module consists of complete digital camera reference designs with source code in Verilog HDL and a user manual with live demo examples. It supports exposure, light control, and motion capture.
	TRDB_LCM Digital Panel Daughtercard **Terasic Technologies, Inc.**	Daughtercard	This 3.6" digital panel development kit consists of reference designs (TV player and color pattern generator) with source code in Verilog HDL.

Training Overview

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We offer an extensive curriculum of classes to deepen your expertise. Our classes are beneficial whether you're new to FPGA and CPLD design, or are an advanced user wanting an update on the latest tools, tips, and tricks. Choose a training path delivered in three different ways:

- Instructor-led training, typically lasting one to two days, involves in-person instruction with hands-on exercises from an Altera or Altera partner subject matter expert. Fees vary.
- Virtual classrooms, involving live instructor-taught training over the Web, allow you to benefit from the interactivity with an instructor from the comfort of your home or office. Classes are taught in 4.5-hour sessions across consecutive days.
- Online training, typically one to two hours long, features pre-recorded presentations and demonstrations. Online classes are free and can be taken at any time.

To help you decide which courses might be most useful to you, we've grouped classes into specific curricula. Curricula paths include Altera Fundamentals, I/O Interfaces, Software Developer, Embedded Hardware, DSP Designer, and more.

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Altera Instructor-Led and Virtual Classroom Courses Virtual Classroom Courses Denoted with a * (All Courses Are One Day in Length Unless Otherwise Noted)		
Course Category	**General Description**	**Course Titles**
Design languages	Attain the skills needed to design with Verilog HDL and VHDL for programmable logic	• Introduction to VHDL* • Advanced VHDL Design Techniques* • Introduction to Verilog HDL* • Advanced Verilog HDL Design Techniques*
Quartus II software	Acquire design entry, compilation, programming, verification, and optimization skills by learning how to use both basic and advanced features of Quartus II software	• The Quartus II Software Design Series: Foundation* • The Quartus II Software Debug and Analysis Tools • The Quartus II Software Design Series: Timing Analysis* • Timing Closure with the Quartus II Software* • Advanced Timing Analysis with TimeQuest* • Design Optimization Using Quartus II Incremental Compilation* • Partial Reconfiguration with Altera FPGAs
Software development	Accelerate algorithm performance with Open Computing Language (OpenCL™) by offloading to an FPGA	• Parallel Computing with OpenCL Workshop* • Optimizing OpenCL for Altera FPGAs*
System integration	Build hierarchical systems by integrating IP and custom logic	• Introduction to the Qsys System Integration Tool • Advanced Qsys System Integration Tool Methodologies
Embedded system design	Learn to design an ARM-based or Nios II processor system in an Altera FPGA	• Designing with the Nios II Processor • Developing Software for the Nios II Processor (2-day course) • Designing with an ARM-based SoC • Developing Software for an ARM-based SoC
Memory interfaces	Implement interfaces to external memory	• Implementing, Simulating, and Debugging External Memory Interfaces*
System design	Solve DSP and video system design challenges using Altera technology	• Designing with DSP Builder Advanced Blockset* • Video Design Framework Workshop
Connectivity design	Build high-speed, gigabit interfaces using embedded transceivers found in leading-edge FPGA families	• Building Gigabit Interfaces in Generation 10 Devices • Building Gigabit Interfaces in 28 nm Devices • Creating PCI Express Links Using FPGAs

Online Training

Altera Free Online Training Courses (Courses Are Approximately One Hour in Length)		
Course Category	Course Titles	Languages
Getting started	Read Me First!	English, Chinese, and Japanese
	Basics of Programmable Logic	English, Chinese, and Japanese
	How to Begin a Simple FPGA Design	English, Chinese, and Japanese
Design languages	VHDL Basics	English and Chinese
	Verilog HDL Basics	English and Chinese
	SystemVerilog with the Quartus II Software	English, Chinese, and Japanese
	Best HDL Design Practices for Timing Closure	English, Chinese, and Japanese
Software overview and design entry	Using the Quartus II Software: An Introduction	English, Chinese, and Japanese
	The Quartus II Software Interactive Tutorial	English only
	The Quartus II Software Design Series: Foundation (note: this training is equivalent to the instructor-led course of the same name)	English, Chinese, and Japanese
	What's New in the Quartus II Software	English and Japanese
	Setting Up Floating Licenses	English only
	Synplify Pro Tips and Tricks	English only
	Synplify Synthesis Techniques with the Quartus II Software	English only
	Using Quartus II Software: Schematic Design	English and Chinese
	Introduction to Incremental Compilation	English, Chinese, and Japanese
	I/O System Design	English, Chinese, and Japanese
	Advanced I/O System Design	English and Chinese
	Managing Metastability with the Quartus II Software	English only
	Partial Reconfiguration	English only
Verification and debugging	Overview of Mentor Graphics ModelSim Software	English and Japanese
	SignalTap II Embedded Logic Analyzer: Getting Started	English, Chinese, and Japanese
	Using Quartus II Software: Chip Planner	English only
	Debugging and Communicating with an FPGA Using the Virtual JTAG Megafunction	English only
	System Console	English and Chinese
	Debugging JTAG Chain Integrity	English only
	Power Analysis and Optimization	English and Chinese
	Resource Optimization	English only

Online Training

Altera Free Online Training Courses (Courses Are Approximately One Hour in Length)		
Course Category	**Course Titles**	**Languages**
Timing analysis and closure	TimeQuest Timing Analyzer	English, Chinese, and Japanese
	Timing Closure Using Quartus II Advisors and Design Space Explorer	English and Chinese
	Timing Closure Using Quartus II Physical Synthesis Optimizations	English and Chinese
	Timing Closure Using TimeQuest Custom Reporting	English only
	Design Evaluation for Timing Closure	English and Chinese
	Good High-Speed Design Practices	English only
	Constraining Source Synchronous Interfaces	English and Chinese
	Constraining Double Data Rate Source Synchronous Interfaces	English and Chinese
Memory interfaces	Using High-Performance Memory Interfaces in Altera FPGAs	English and Chinese
Connectivity design	Transceiver Basics	English, Chinese, and Japanese
	Transceiver Toolkit	English only
	Transceiver Reconfiguration in Altera 28 nm Devices	English only
	Decision Feedback Equalization and Adaptive Equalization in Stratix IV GX/GT Devices	English only
	Advanced Signal Conditioning for Stratix IV and Stratix V Receivers	English only
	Getting Started with Altera's 28 nm PCI Express Solutions	English only
	Getting Started with Altera's 40 nm PCI Express Solutions	English and Japanese
	Custom Protocol Design in Altera 28 nm Devices	English only
	Introduction to Altera's 10/100/1000 Mb Ethernet Solutions	English and Chinese
	Introduction to Altera's 10 Gb Ethernet Solutions	English only
	High-Speed Serial Protocol Design with Altera Transceiver Devices	English and Chinese
	Dynamic Reconfiguration in Altera Transceiver Devices	English and Chinese
System design	Introduction to Qsys	English and Japanese
	Advanced System Design Using Qsys	English only
	Custom IP Development Using Avalon and AXI Interfaces	English and Chinese
	Designing with DSP Builder Advanced Blockset: An Overview	English and Chinese
	DSP Builder Standard Blockset: An Overview	English only
	Variable-Precision DSP Blocks in Altera 28 nm FPGAs	English only
	Viterbi Decoder	English only
	High-Performance Floating-Point Processing with FPGAs	English only
	Building Video Systems	English only
	Implementing Video Systems	English only

Online Training

Altera Free Online Training Courses (Courses Are Approximately One Hour in Length)		
Course Category	**Course Titles**	**Languages**
System design (continued)	Creating Reusable Design Blocks	English only
	Using Cascaded-Integrator-Comb Filter in Multirate Digital Systems	English only
	FIR Compiler II	English only
	Avalon Verification Suite	English only
OpenCL	Introduction to Parallel Computing with OpenCL	English, Japanese, and Chinese
	Writing OpenCL Programs for Altera FPGAs	English, Japanese, and Chinese
	Running OpenCL on Altera FPGAs	English, Japanese, and Chinese
Embedded system design	Designing with the Nios II Processor and Qsys - Day 1	Japanese only
	Developing Software for the Nios II Processor: Tools Overview	English, Chinese, and Japanese
	Developing Software for the Nios II Processor: Design Flow	English and Chinese
	SoC Hardware Overview - (Part 1)	English, Japanese, and Chinese
	SoC Hardware Overview - (Part 2)	English, Japanese, and Chinese
	Hardware Design Flow for an ARM-Based SoC	English, Chinese, and Japanese
	Software Design Flow for an ARM-Based SoC	English, Chinese, and Japanese
	Using the Nios II Processor	English, Chinese, and Japanese
	Developing Software for the Nios II Processor: Nios II Software Build Tools for Eclipse	English and Japanese
	Nios II Software Build Tools for Eclipse and BSP Editor (Quartus II Software 10.0 Update)	English only
	Developing Software for the Nios II Processor: HAL Primer	English, Chinese, and Japanese
	Nios II Floating-Point Custom Instructions	English, Chinese, and Japanese
	Developing Software for the Nios II Processor: MMU and MPU	English and Chinese
	Lauterbach Debug Tools	English only
	Introduction to Graphics	English only
Device-specific training	Power Distribution Network Design for Stratix III and Stratix IV FPGAs	English and Chinese
	Power Distribution Network Design Using Altera PDN Design Tools	English only
	Configuring Altera FPGAs	English and Chinese
Scripting	Command-Line Scripting	English only
	Introduction to Tcl	English and Chinese
	Quartus II Software Tcl Scripting	English and Japanese

Glossary

Below is a glossary of helpful terms to bring you up to speed on Altera devices.

Term	Definition
Adaptive logic module (ALM)	Logic building block, used by some Altera devices, which provides advanced features with efficient logic utilization. Each ALM contains a variety of look-up table (LUT)-based resources that can be divided between two combinational adaptive LUTs (ALUTs).
Configuration via Protocol (CvP)	CvP is a configuration method that enables you to configure the FPGA using industry-standard protocols. Currently CvP supports the PCIe protocol.
Embedded HardCopy Blocks	These metal-programmable hard IP blocks deliver up to 14M ASIC gates or up to 700K additional LEs to harden standard or logic-intensive applications.
Equivalent LE	Device density represented as a comparable amount of LEs, which uses the 4-input LUT as a basis.
Fractional phase-locked loops (Fractional PLL)	A phase-locked loop (PLL) in the core fabric, fractional PLLs provide increased flexibility as an additional clocking source for the transceiver, replacing external VCXOs.
Global clock networks	Global clocks can drive throughout the entire device, serving as low-skew clock sources for functional blocks such as ALMs, DSP blocks, TriMatrix memory blocks, and PLLs. See regional clocks and periphery clocks for more clock network information.
Hard processor system (HPS)	This processor system is a hardened component within the SoC, which comprises a dual-core ARM Cortex-A9 MPCore processor, a rich set of peripherals, and multiport memory controllers.
Logic element (LE)	This logic building block, used by some Altera devices, includes a 4-input LUT, a programmable register, and a carry chain connection. See device handbooks for more information.
Macrocells	Similar to LEs, this is the measure of density in MAX series CPLDs.
Memory logic array blocks (MLABs)	MLABs are dual-purpose blocks, configurable as regular logic array blocks or as memory blocks.
On-chip termination (OCT)	Support for driver impedance matching and series termination, which eliminates the need for external resistors, improves signal integrity, and simplifies board design. On-chip series, parallel, and differential termination resistors are configurable via Quartus II software.
Periphery clocks (PCLKs)	PCLKs are a collection of individual clock networks driven from the periphery of the device. PCLKs can be used instead of general-purpose routing to drive signals into and out of the device.
Plug & Play Signal Integrity	This capability, consisting of Altera's adaptive dispersion engine and hot socketing, lets you change the position of backplane cards on the fly, without having to manually configure your backplane equalization settings.
Programmable Power Technology	This feature automatically optimizes logic, DSP, and memory blocks for the lowest power at the required performance. Only the blocks with critical-path logic need to be in high-performance mode; all others are in low-power mode.
Real-time in-system programming (ISP)	This capability allows you to program a MAX II device while the device is still in operation. The new design only replaces the existing design when there is a power cycle to the device, so can perform in-field updates to the MAX II device at any time without affecting the operation of the whole system.
Regional clocks	Regional clocks are device quadrant-oriented and provide the lowest clock delay and skew for logic contained within a single device quadrant.
System on a chip (SoC)	An SoC is an embedded system that consists of a processor, peripherals, and custom hardware integrated on a single device.
Variable-precision blocks	These integrated blocks provide native support for signal processing of varying precisions—for example, 9x9, 27x27, and 18x36—in a sum or independent mode.

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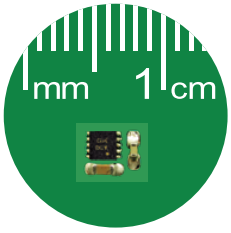

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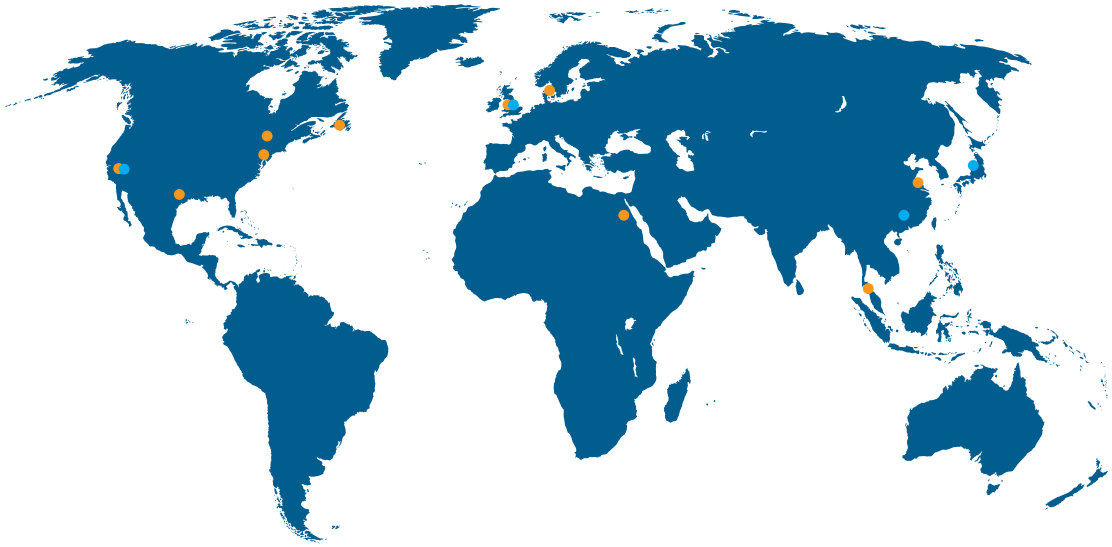
Map of Technology Centers and Main Corporate Offices



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