

Arria V FPGA Family Package and I/O Selector Guide



Arria V FPGA Features

The following features, packages, and I/O matrices give you an overview of our devices. To get the full story, check out our online selector guide: www.altera.com/selector.

| | | Arria® V GX FPGAs (1.1 V) ¹ , 6.375-Gbps Transceivers | | | | | | | |
|---|--|---|---------|---------|---------|---------|---------|---------|---------|
| | | 5AGXA1 | 5AGXA3 | 5AGXA5 | 5AGXA7 | 5AGXB1 | 5AGXB3 | 5AGXB5 | 5AGXB7 |
| Density and Speed | ALMs | 28,302 | 57,358 | 71,698 | 90,943 | 113,208 | 136,226 | 158,491 | 186,792 |
| | Equivalent LEs | 75,000 | 152,000 | 190,000 | 241,000 | 300,000 | 361,000 | 420,000 | 495,000 |
| | Registers | 113,208 | 229,434 | 286,792 | 363,774 | 452,830 | 544,906 | 633,962 | 747,170 |
| | M10K memory blocks | 488 | 1,016 | 1,153 | 1,336 | 1,377 | 1,680 | 2,006 | 2,324 |
| | MLAB memory (Kb) | 463 | 901 | 1,173 | 1,408 | 1,852 | 2,253 | 2,532 | 3,087 |
| | Embedded memory (Kb) | 5,000 | 10,400 | 11,800 | 13,680 | 14,100 | 17,280 | 20,540 | 23,800 |
| | DSP blocks | 240 | 396 | 600 | 800 | 920 | 1,045 | 1,092 | 1,139 |
| | Speed grades (fastest to slowest) | -4, -5, -6 | | | | | | | |
| Architectural Features | Global clock networks | 16 | | | | | | | |
| | PLLs/unique outputs | 10/40 | 10/40 | 12/48 | 12/48 | 12/48 | 12/48 | 16/64 | 16/64 |
| | Configuration file size (Mb) | TBD | TBD | TBD | TBD | TBD | TBD | TBD | TBD |
| | Design security | ✓ | | | | | | | |
| I/O Features | I/O voltage levels supported (V) | 1.2, 1.5, 1.8, 2.5, 3.0, 3.3 ² | | | | | | | |
| | I/O standards supported | LVTTTL, LVCMOS, PCI, PCI-X, LVDS, mini-LVDS, RSDS, LVPECL, Differential SSTL-15, Differential SSTL-18, Differential SSTL-2, Differential HSTL-12, Differential HSTL-15, Differential HSTL-18, SSTL-15 (I and II), SSTL-18 (I and II), SSTL-2 (I and II), 1.2V HSTL (I and II), 1.5V HSTL (I and II), 1.8V HSTL (I and II) | | | | | | | |
| | LVDS channels, 1,250 Mbps (receive/transmit) | 68 | 68 | 120 | 120 | 160 | 160 | 152 | 152 |
| | Embedded DPA circuitry | ✓ | | | | | | | |
| | Series and differential OCT | ✓ | | | | | | | |
| | Programmable drive strength | ✓ | | | | | | | |
| | Transceiver (SERDES) channels (6.375 Gbps) | 12 | 12 | 24 | 24 | 24 | 24 | 36 | 36 |
| | PCI Express® Gen2 x4 hard IP blocks | 1 | 1 | 2 | 2 | 2 | 2 | 2 | 2 |
| DDR3/2 hard memory controller IP blocks | 2 | 2 | 4 | 4 | 4 | 4 | 4 | 4 | |
| External Memory Interfaces | Memory devices supported | DDR3, DDR2, DDR, QDR II, QDR II+, RLD RAM II, LPDDR2, Mobile DDR, SDR | | | | | | | |

¹ Maximum LVDS channels, transceiver channels, PLLs, and PCIe hard IP blocks for the product line shown. Various packages offer a variety of options to meet your design needs.

² 3.3-V compliant, requires a 3.0-V power supply

Arria V FPGA Features Cont.

| | | Arria V GT FPGAs (1.1 V) ¹ , Up to 10.375-Gbps Transceivers | |
|----------------------------|--|---|---------|
| | | 5AGTD3 | 5AGTD5 |
| Density and Speed | ALMs | 136,226 | 186,792 |
| | Equivalent LEs | 361,000 | 495,000 |
| | Registers | 544,906 | 747,170 |
| | M10K memory blocks | 1,680 | 2,324 |
| | MLAB memory (Kb) | 2,253 | 3,087 |
| | Embedded memory (Kb) | 17,280 | 23,800 |
| | DSP blocks | 1,045 | 1,139 |
| | Speed grades (fastest to slowest) | TBD | |
| Architectural Features | Global clock networks | 16 | |
| | PLLs/unique outputs | 12/48 | 16/64 |
| | Configuration file size (Mb) | TBD | TBD |
| | Design security | ✓ | |
| I/O Features | I/O voltage levels supported (V) | 1.2, 1.5, 1.8, 2.5, 3.0, 3.3 ² | |
| | I/O standards supported | LVTTTL, LVCMOS, PCI, PCI-X, LVDS, mini-LVDS, RSDS, LVPECL, Differential SSTL-15, Differential SSTL-18, Differential SSTL-2, Differential HSTL-12, Differential HSTL-15, Differential HSTL-18, SSTL-15 (I and II), SSTL-18 (I and II), SSTL-2 (I and II), 1.2V HSTL (I and II), 1.5V HSTL (I and II), 1.8V HSTL (I and II) | |
| | LVDS channels, 1,250 Mbps (receive/transmit) | 120 | 150 |
| | Embedded DPA circuitry | ✓ | |
| | Series and differential OCT | ✓ | |
| | Programmable drive strength | ✓ | |
| | Transceiver (SERDES) channels (10.375 Gbps, 6.375 Gbps) | 4, 18 | 6, 24 |
| | PCI Express Gen2 x4 hard IP blocks | 1 | 1 |
| | DDR3/2 hard memory controller IP blocks | 1 | 4 |
| External Memory Interfaces | Memory devices supported | | |
| | DDR3, DDR2, DDR, QDR II, QDR II+, RLDRAM II, LPDDR2, Mobile DDR, SDR | | |

¹ Maximum LVDS channels, transceiver channels, PLLs, and PCIe hard IP blocks for the product line shown. Various packages offer a variety of options to meet your design needs.

² 3.3-V compliant, requires a 3.0-V power supply

Arria V Series Package and I/O Matrices

| Arria V GX and GT FPGAs (1.1 V), Up to 10.375-Gbps Transceivers | | | | |
|---|---|---|---|---|
| FBGA (F) | | | | |
| | 672 pin 27 x 27 (mm) 1.0-mm pitch | 896 pin 31 x 31 (mm) 1.0-mm pitch | 1,152 pin 35 x 35 (mm) 1.0-mm pitch | 1,517 pin 40 x 40 (mm) 1.0-mm pitch |
| 5AGXA1 | 336 9 | | | |
| 5AGXA3 | 336 9 | | | |
| 5AGXA5 | 288 9 | 384 18 | 544 24 | |
| 5AGXA7 | 288 9 | 384 18 | 544 24 | |
| 5AGXB1 | | 384 18 | 544 24 | 704 24 |
| 5AGXB3 | | 384 18 | 544 24 | 704 24 |
| 5AGXB5 | | | 528 24 | 668 36 |
| 5AGXB7 | | | 528 24 | 668 36 |
| 5AGTD3 | | 322 12+4 | 504 16+4 | 656 18+4 |
| 5AGTD5 | | | 488 18+6 | 616 24+6 |

636
8+0

Values on top indicate available user I/O pins; values at the bottom indicate the 6.375-Gbps plus 10.375-Gbps transceiver count.

Vertical migration (same V_{CC}, GND, ISP, and input pins). For vertical migration, the number of user I/Os may be less than the number stated in the table