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[www.altera.com](http://www.altera.com)**Quarterly Spotlight****[Download Easy-to-Use Video Processing Demo for NEEK](#)**

Altera's video and image processing example design demonstrates the dynamic scaling and clipping of a standard-definition video stream in NTSC format. [Download the design](#) and try it out on the Nios® II Embedded Evaluation Kit (NEEK).

**[Develop Custom HD Deinterlacing Solution With Altera VIP Cores](#)**

[Read a white paper](#) that examines sophisticated deinterlacing solutions based on Cyclone® III and Stratix® III FPGAs and Altera's Video and Image Processing Suite of IP cores. These solutions help you implement HD quality video deinterlacing in the shortest possible time.

**[Sharpen Your DSP Design Skills Through Training Courses](#)**

Digital signal processing (DSP) designers can take advantage of a specially designed curriculum of instructor-led and complimentary online classes. [Sign up today](#) for topics ranging from designing with DSP Builder to building video systems with Altera video solutions.

**[Learn How FPGAs Support Video Processing for Military Apps](#)**

[Read an article](#) that examines how FPGAs handle complex, real-time video processing within a constrained power budget. The article shows how the latest low-power, low-cost FPGAs are ideal for military electro-optical/infrared systems.

**[Take Advantage of Advances in FPGA Floating-Point Technology](#)**

Unlike digital signal processors, an FPGA can support a DSP datapath with mixed floating- and fixed-point operations, while achieving performance in excess of 100 GFLOPS. [Read this white paper](#) to learn more.

**[Get an Overview of CMOS Image Sensor Processing With FPGAs](#)**

[Read this article](#) to learn about common functions implemented in a CMOS image sensor processing pipeline. You'll also get details into a fully verified sensor processing pipeline and the implementation of such a design on a low-cost FPGA.



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