

Quarterly Spotlight**[Introducing the ARM-Based SoC FPGA for Your Embedded Designs](#)**

Altera® SoC FPGAs integrate a dual-core ARM® Cortex™-A9 MPCore™ processor, memory controllers, and peripherals with Cyclone® V and Arria® V FPGAs connected via a high-bandwidth interconnect. This combination reduces your system power, system cost, and board size while boosting your embedded system's performance. [Learn more.](#)



ARM® + Altera® =
SoC FPGAs

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Embedded Software & Tools**[Jump-Start Embedded Software Development for SoC FPGAs](#)**

Start code development earlier with Altera's new [prototyping tool for SoC FPGAs](#). Get a jump-start on developing device-specific software before hardware availability. With better control and visibility, the tool helps you work more productively and speed your time to market. [Watch our video](#) and see how to start programming today with the SoC FPGA Virtual Target.



**Jump-Start Software
Development for SoC FPGAs**

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[Download Quartus II Software v11.1 to Start Nios II Designs with Arria V and Cyclone V FPGAs](#)

With Quartus® II software v11.1, design Nios II® embedded systems with Arria V and Cyclone V FPGAs or get enhanced support for Stratix® V FPGAs. Other features include System Console and Qsys system integration tool enhancements. [Download](#) Quartus II Subscription Edition or Web Edition with the Nios II Embedded Design Suite (EDS) and [renew your Nios II IP license](#) to start designing today.



QUARTUS® II
**NEW Quartus® II
Software v11.1**

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[System Console: Debug and Monitoring Tool](#)

Available in Quartus® II software v11.1, System Console provides an easy way to build GUI elements and connect them to hardware events for monitoring performance, debugging designs, or demonstrating design functionality. Its common command set lets you maintain the same level of debug capability in the lab, during simulation, and after the product has shipped. [Watch demonstrations](#) or [attend training now](#).



**Read BDTI's Analysis of
Altera's Floating-Point
DSP Design Flow**

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New Literature

Learn more about SoC FPGAs:

- **Advanced information briefs:**
 - [SoC FPGA product overview \(PDF\)](#)
 - [SoC FPGA ARM Cortex-A9 MPCore Processor \(PDF\)](#)
 - [SoC FPGA Dedicated Peripherals \(PDF\)](#)
- **White paper:** [User-Customizable ARM-Based SoC FPGAs for Next-Generation Embedded Systems](#)
- **Brochures:**
 - [SoC FPGA overview \(PDF\)](#)
 - [SoC FPGA Virtual Target \(PDF\)](#)

Learn more about Quartus II System Console tool:

- **White paper:** [System-Level Debugging and Monitoring of FPGA Designs](#)



DSP
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Technical Design Resources

[Accelerate Your Freescale Coldfire V1 Embedded System Integration with Qsys](#)

The synthesizable 32-bit RISC Freescale® ColdFire® V1 core, the smallest and lowest-power processor in this family, is now available for your next FPGA design with full Qsys support. Qsys allows rapid system integration of processors with memory and peripherals to customize your embedded system.

[No-Hassle uClinux Development for Nios II Processor with BeMicro SDK](#)

Learn about this reference design on the low-cost [BeMicro SDK](#) from Arrow Electronics. It contains all you need to build an application based on the uClinux™ operating system for the Nios II processor. Its precompiled image eliminates set-up hassles, such as board layer settings and basic buildable driver settings for the board. Simply download the image, develop your application in it, and build the kernel.

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