Embedded Quarterly e-Newsletter

Q3 2005

Welcome to the first issue of Altera's *Embedded e-Newsletter*. This quarterly e-newsletter brings you the latest news, software tools, seminars, and technical articles on Altera's embedded processing products.

Quarterly Spotlight

Download Reference Design: Network Acceleration for Nios II Free

Altera, MorethanIP, and InterNiche have teamed up to provide Nios® II system designers with a high-performance networking solution delivering over 60 Mbits per second via TCP/IP. Download the white paper and reference design now.

Embedded Software

Jump Start Your Network Design with Complete Ethernet IP Package from Microtronix

New Partner Product

Based on the popular OpenCores.org 10/100 Ethernet MAC, this development package adds support for the Nios II processor, targeting the Microtronix µKit and Altera® Nios II Evaluation Kit. The package includes support for µClinux, MicroC/OS-II and the Nios II hardware abstraction layer (HAL) libraries.

End-Market Applications

Download Reference Design: Automotive Graphics Controller Free

This reference design shows the power and flexibility available in FPGAs for targeting low-cost applications such as those required by the automotive marketplace. A video module provides clipping, color space conversion, and scaling. The design also features a graphics library running on a Nios II processor. Download the reference design now.

CPUs, Peripherals & Interfaces

Simplify Your PCI Designs: PCI Compiler Is Now SOPC Builder-Ready

PCI Compiler provides a complete, easy-to-use solution for creating PCI interfaces with Altera FPGAs. Hardware designers can now easily integrate PCI interfaces into their systems using the SOPC Builder system integration tool.

Back to top ▲

Literature, Tutorials & Technical Resources

Article: Multi-Processor Solutions with FPGAs Free

Lower your system costs and reduce software design complexity and time by

In This Issue:

adding CPUs to your system. By breaking up large software applications into smaller, more easily designed and tested units, you can reduce development time and engineering costs with minimal tradeoffs.

Tutorial: Learn How to Create Multi-Processor Nios II Systems Free

Learn the features of Nios II processors and SOPC Builder tool that are useful for creating systems with more than one processor. The tutorial includes a step-by-step guide for assembling a three-processor system, as well as writing and debugging the software applications for each processor. Download the PDF tutorial.

Online Demonstration: Interfacing to External Memory Free

View this web-based demonstration video to learn how to design with Altera's DDR and DDR2 SDRAM controller IP functions using SOPC Builder. The video will show you how to customize the parameters for your DDR interface, automatically generate a timing analysis, and quickly and easily connect the DDR interface to the rest of your SOPC Builder system.

Development Kits & Boards

Now Shipping: Nios II Dev Kit, Cyclone II Edition - Order Today!

This kit is a full-featured development environment for the Nios II processors, featuring a Cyclone II EP2C35 device and DDR SDRAM memory. It includes everything needed to start designing low-cost embedded systems in minutes.

Reserve Your Session to Test Drive the Nios II Dev Kit Online Free

New technology allows you to take control of an actual Nios II development kit via the Internet for as many no-cost sessions as you like and up to two hours per session. The online Nios II Development Kit, Stratix® II Edition, lets you evaluate Altera hardware, processors, and intellectual property without the hassles of shipping, installation, or configuration.

Events, Net Seminars & Training

Upcoming Training Courses

San Jose, CA, July 28 - Designing with Nios II and SOPC Builder
Plano, TX, August 11 - Designing with Nios II and SOPC Builder
San Jose, CA, August 11 - Developing Software for Nios II
San Jose, CA, September 1 - Developing Software for Nios II
On-Line, Anytime - System-on-a-Programmable-Chip Design Using the Nios II Embedded Processor

Back to top ▲

From the Forum

The following topic is from www.niosforum.org. There are over 2,500 registered users and over 2,000 topics on the Nios Forum. The Forum is an excellent place to go for design tips and support, and it is also useful for

sharing embedded software and hardware designs.

The following topic discusses whether a designer should connect a custom-built peripheral using the parallel I/O (PIO) component or by creating an Avalon® switch fabric interface. Read all posts on this topic.

PIO Vs. Avalon ?!

Posted by: wesam_gobran Jun 15 2005, 02:03 PM

hi....i'm using a nios II processor and I wanna add a hardware block external to the processor and on the same FPGA that performs a general function (eg, Vector dot product). Should I interface it to the processor using the avalon bus or can i interface to a PIO block that's already interfaced to the avalon bus?
thnx

Posted by: smcnutt Jun 15 2005, 03:58 PM

Hi wesam,

> Should I interface it to the processor using the avalon bus or can I
> interface to a PIO block that's already interfaced to the avalon bus?

I started a design using a PIO for address, a PIO for control, and a PIO for data. I quickly changed my mind once I started writing the device driver code -- it was much more time-efficient (and MIPS efficient) to just write a simple avalon interface. Later, I decided I needed DMA support ... and it basically came "for free" since I already had the avalon interface.

In general, if you're doing more than just twiddling a few bits, you should consider the avalon interface. One way or another, you'll end up writing the interface logic anyway-- whether it's in an HDL or in C ... but the HDL strategy comes with some built-in "freebies" ;-)

Regards,
--Scott

Read all posts on this topic.

Back to top ▲