

Welcome to the Q4 issue of Altera's *Embedded e-Newsletter*. This quarterly e-newsletter brings you the latest news, software tools, seminars, and technical articles on Altera's embedded processing products.

With over 16,000 embedded development kits shipped, over 5,000 licensed developers, and over 3,500 registered Nios Community Forum users, the Nios[®] II processor architecture continues to grow in popularity and extend its claim as the world's most popular FPGA-targeted embedded processor. Learn more at www.altera.com/nios.

Quarterly Spotlight

[Accelerated Technology's Nucleus Products Now Support Nios II](#)

The Eclipse-powered Nucleus EDGE embedded integrated development environment (IDE) provides a complete turnkey solution that encompasses the whole development process from project management to analysis and profiling. Now Nios[®] II software developers can benefit from this seamlessly integrated IDE, compiler, debugger and system profiler. [Learn more.](#)

Embedded Software

[Hardware/software Co-Verification Support for Nios II from Adveda](#)

Adveda enables both hardware and software developers to close the system-on-chip verification gap by offering fast and fully integrated simulation and debugging tools. The Univers debugger supports simultaneous simulation and debugging of more than one Nios II CPU in multi-processor applications, including all hardware peripherals in a single simulation environment.

[Evidence RT-Druid Tool Suite & Erika Enterprise Multi-processor RTOS](#)

Evidence presents RT-Druid, a tool suite for the automatic configuration and deployment of the Erika Enterprise multi-processor RTOS. Erika Enterprise is now available for Altera's Nios II processors, and the RT-Druid environment seamlessly integrates with the Altera[®] Nios II IDE tool chain based on the Eclipse framework.

[GoFast Floating Point Library from Micro Digital Inc.](#)

GoFast is a family of fast, re-entrant floating point libraries that support Altera's Nios II processors and the GNU C compiler. They are ANSI C-compatible and are designed to directly replace a C compiler's runtime floating-point support (library or coprocessor). GoFast boosts the performance of an application's math calculations 3 to 6 times over that of the GNU floating point libraries. [Learn more about GoFast.](#)

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[Visit the Redesigned Nios Community Forum](#)

The popular Nios Community Forum, at www.niosforum.org, has been redesigned to add project hosting capabilities. Now forum users can browse other project pages, download designs, and even post their designs in their own project section. There is also a new products section where Nios II embedded partners can showcase their product offerings. Visit the [new forum](#).

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Literature, Tutorials & Technical Resources

[Download Quartus II version 5.1 Software Patch for Nios II v5.1](#)

The Quartus II Version 5.1 software patch is now available to download on www.altera.com. The software patch resolves a critical issue when compiling with Nios II v5.1 designs using Quartus II v5.1. The software patch is only required for Quartus II v5.1 and Nios II v5.1. For more information, including the software patch download, view the [Quartus II v5.1 critical issue page](#).

[Application Note: Profiling Nios II Systems](#) **Free**

This application note describes a variety of ways to measure the performance of a Nios II system using the GNU profiler, the timestamp interval timer peripheral, and the performance counter peripheral. Get [Nios II Literature](#) for the accompanying design files.

[Tutorial: Using Nios II Tightly Coupled Memory to Enhance Performance](#) **Free**

Tightly coupled memory provides guaranteed, fixed, low-latency access to on-chip memory for performance-critical applications. This tutorial describes how to use the Nios II tightly coupled memory and discusses some possible applications as well. There is a [software design file](#) that accompanies the [tutorial](#).

[Nios II Flash Programmer Now More Robust and Flexible](#)

The Nios II flash programmer has been redesigned in the 5.1 release to be more robust and more flexible. If you used the flash programmer prior to version 5.1, we recommend that you read this new user guide in its entirety to take advantage of new features. [Download Now](#)

[Online Demo: Making SOPC Builder Peripherals](#) **Free**

This online demonstration describes the design flow to develop custom SOPC Builder-ready peripherals using the SOPC Builder component editor utility. Custom logic blocks packaged as SOPC Builder peripherals can be added to a design similar to any commercially available SOPC Builder-ready component. They can also be published and shared with others, promoting design reuse and rapid product development. [View the online demonstration](#).

[Online Demo: Creating Multi-Clock Domain Systems in SOPC](#)

Builder Free

This online demonstration outlines a common scenario of a system with separate control and data paths, with different performance requirements for each. SOPC Builder allows you to specify separate clock frequencies for each component in the design, and automatically generates the necessary clock domain-crossing logic. Learn more about multi-clock domain system design with this [online demonstration](#).

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Events, Net Seminars & Training

[Embedded World 2006, Nürnberg, Germany - February 14-16, 2006](#)

Visit Altera in hall 12, booth 356 to learn about our latest embedded products and services.

[Net Seminar: Building Handheld Systems in Minutes Using FPGAs](#)

View this on-demand net seminar today and learn how to:

- Optimize your system design and speed time-to-market with SOPC Builder
- Implement an LCD/touch panel interface in an FPGA
- Benchmark system performance with hardware accelerators
- Create a custom embedded system in minutes

Upcoming Training Courses

Schaumburg, IL, December 1, 2005 - [Developing Software for Nios II](#)

San Jose, CA, December 15, 2006 - [Designing with Nios II and SOPC Builder](#)

San Jose, CA, March 2, 2006 - [Designing with Nios II and SOPC Builder](#)

San Jose, CA, February 2, 2006 - [Developing Software for Nios II](#)

San Jose, CA, February 3, 2006- [Developing Software for Nios II](#)

On-Line, Anytime - [System-on-a-Programmable-Chip Design Using the Nios II Embedded Processor](#)

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From the Forum

The following topic is from www.niosforum.org. Now with over 3,500 registered users, the Nios Community Forum is an excellent place to go for design tips and support, and is also useful for sharing embedded software and hardware designs.

The following topic discusses several users' experiences with measuring and optimizing network performance using a Nios II processor. [Read all posts on this topic](#).

[Maximum ethernet speed, nios2 and lwip - sending speed](#)

Posted by: CReal Jun 15 2005, 03:18 AM

Hello!

simple question: what are your experiences about the network speed with nios2 and lwip stack?

my scenario:

nios2 @ 75MHz

lwip stack

udp packages 1500 bytes (loop sending always the same content) in buffer

no operating system

= speed 2.0 - 2.5 MBit/s

I think this is really slow...I have to transmit 400MBit/s. So I have to implement the stack in hardware to reach this speed.

Anyone faster?

thnx

Posted by: Major Sept 14 2005, 01:01 AM

UDP speed near 5 MByte per second

TCP 1.2MByte per second (real data payload)

Posted by: revolt Sept 25 2005, 07:44 AM

400 - 600 Mbit/s. Thats a word. I think that is impossible via Ethernet.

I have a NIOS II @ 100 Mhz and the UDP checksum calculation in HW. With this configuration I reached ~62 MBit/s transfer rate. I think with more optimization 70-75 MBit/s should be possible with the 91C111.

kind regards

revolt

[Read more postings](#) on this topic on the Nios Community Form.

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