

Welcome to the December issue of the *Inside Edge*. This monthly e-Newsletter gives you the latest news about Altera's products and solutions.

Monthly Spotlight

[New Quartus II Web Edition v4.2 Is #1 in Performance](#)

Quartus® II software version 4.2 delivers the highest performance available for FPGAs and CPLDs. This release also introduces the PowerPlay power analysis and optimization technology. Design to win--download Quartus II Web Edition software today.

[Free – Download Now](#)

FPGAs, CPLDs & Structured ASICs

[Learn Why Stratix II Has 39% Performance Lead Over Xilinx Virtex-4](#)

The latest benchmark results using an industry-expert-endorsed benchmarking methodology demonstrate that Stratix II devices command an average of 39 percent performance lead over Virtex-4 FPGAs. Get the details and register for the Stratix II vs. Xilinx Virtex-4 FPGA performance net seminar.

[Place Your Orders Now for MAX II EPM240 CPLDs](#)

The EPM240 device, the smallest and lowest-cost MAX II family member, will be shipping soon. The MAX II EPM240 CPLD has 240 equivalent logic elements (LEs), 8,192 user flash memory bits, and 80 I/O pins. Contact your Altera® sales representative or distributor to place your order now.

[Stratix II EP2S130 Ships: 50% Bigger Than any Other FPGA Available](#)

Altera is now shipping the largest FPGA in the world. The EP2S130 leads the industry with 53K (130K logic elements) adaptive logic modules (ALMs), 6.7 Mbits of RAM, 252 18x18 multipliers, and embedded adders in each ALM. High-volume availability will begin in late December 2004.

[Replace Your Legacy ASICs With Cyclone Series FPGAs](#)

Lower your costs using Cyclone™ series FPGAs to replace your legacy ASICs. Start designing for Cyclone series FPGAs by using Quartus II Web Edition Software, which makes it easy to switch your existing ASIC design into an FPGA design.

Software, Intellectual Property & Development Kits

[Now Available--DDR & DDR2 SDRAM Compiler MegaCore v3.1.0](#)

Full timing and pinout support for Cyclone II FPGAs is now available in version 3.1.0 of the DDR & DDR2 SDRAM Compiler MegaCore® function. If you're designing with DDR or DDR2 SDRAM, simplify your life by downloading this core today.

[Gidel PROCStar II Development Board Features Stratix II](#)

The PROCStar II features up to four Altera Stratix II FPGAs (EP2S60, EP2S90, or EP2S180), a five-level memory structure (over 2.5 Gbytes), up to 12 TMS320C64 digital signal processors at 32 Mbytes per device and up to 695 user I/O pins, along with support for Camera Link and Machine I/O.

Events, Training & Net Seminars

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The ALTERA Zone

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Westin Santa Clara
February 4, 2005

[View Now: Stratix II vs. Virtex-4 FPGA Performance Net Seminar](#) **Free**

Learn how Altera's Stratix II FPGAs outperform Xilinx's Virtex-4 FPGAs. Explore the technology in Stratix II FPGAs that provides the industry's highest performance, using the Quartus II development tool. Enter the Altera Zone--feel the performance!

[Take Advantage of Quartus II Online Software Training](#) **Free**

A new series of in-depth online training sessions teach you to take advantage of the latest Quartus II software features. Topics include: power analysis, command line operation, tool command language (Tcl) scripting, and timing analysis.

Recent Articles about Altera

[Implementing Smart Antennas Technology in Cellular Base Stations,](#)

OpenBaseStation Newsletter

Find out how Smart Antennas technology addresses the problem of more users per base station to reduce overall network cost and make the services affordable to subscribers via advanced signal processing techniques called beamforming.

[FPGAs Help Software-Defined Radios Adapt, Wireless Systems Design](#)

Learn about future base stations and how they will house a single data rate (SDR) platform that is built upon programmable logic, software, and intellectual property (IP).

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