

Welcome to the first issue of Inside Edge. Each month you'll receive the latest news about Altera's products and solutions.

Monthly Spotlight

[HardCopy Stratix Device Wins 2003 EDN Innovation of the Year Award](#)

For the second year in a row, Altera won the prestigious EDN Innovation of the year Award. The HardCopy® Stratix® structured ASIC was selected from several hundred products submitted in the Digital ICs category.

FPGAs, CPLDs & Structured ASICs

[Stratix II FPGAs: The Industry's Biggest & Fastest FPGAs!](#)

Built with a rich set of system-level features at 40% lower cost than first-generation Stratix™ devices, Stratix™ II devices have a revolutionary logic structure that offers 500 MHz system clock performance, 180K logic elements (LEs), 9 Mbits of memory, and 384 multipliers.

[Having Delivery Issues with Competing Low-Cost FPGAs?](#)

Cyclone™ FPGAs are available for immediate volume shipments, delivering higher performance at a lower price than Spartan-3 devices. Altera can take you to volume production as fast as you can spin your board. Get started today with complimentary Cyclone samples.

[Learn about Altera's Programmable Logic Performance Leadership](#)

Recent benchmarking analysis proves that Altera is the true programmable logic performance leader. Learn about technical details, timing-analysis techniques, and exact benchmarking methods used in this analysis.

Software & Intellectual Property

[On-line Demonstrations Show You What's New in Quartus II Software](#)

Learn the latest about Quartus® II software by visiting the new Design Software On-Line Demonstration Center. Demonstrations range from a basic introduction to the Quartus II software design flow to demonstrations of advanced design-optimization features.

[Download the SerialLite Reference Design for Stratix GX FPGAs Today](#)

The SerialLite protocol is designed as a lightweight, point-to-point protocol aimed at reducing footprint, latency, and overhead compared to other serial protocols. Download the preliminary reference design today. The full Altera® MegaCore® function version will be released shortly.

Technology & System Solutions

[Visit the Updated High-Speed Serial I/O Technology Center](#)

This new section aggregates all Altera high-speed serial web content on one convenient web page. Learn more about supported protocols, intellectual property (IP), literature, development kits, training, and certified design partners.

Events, Training & Net Seminars

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[Register for the Code:DSP Video & Image Processing Seminar](#)

Complimentary Seminar Coming in June to Boston, San Jose & Toronto Attend emerging technology demonstrations and presentations by industry experts designed to update and educate engineers, system architects, and project managers on video and image processing solutions.

[View Altera's Net Seminar: Design for CPLDs in the Post-Macrocell Era](#)

This on-line net seminar highlights the differences and benefits of the world's first "post-macrocell" CPLD family, MAX[®] II devices, and will show you how to successfully develop designs that leverage this new architecture.

[Attend New Stratix II & MAX II Courses](#)

New classes are available to teach you how to design for the new and innovative Stratix II FPGAs and MAX II CPLDs. Courses are also available that will show you how to get the most from Quartus II software version 4.0 and related EDA tools. Register for a class today!

Technical Support

[Updated Signal Integrity Center Provides Comprehensive Support](#)

Altera offers resources beyond the basics to help designers develop high-speed interfaces using programmable logic. This information helps customers to develop, lay out, and verify their high-speed designs. Characterization and interoperability information are also available.

Recent Articles about Altera

[A Wolf in Sheep's Clothing, FPGA Journal](#)

Are MAX II devices really CPLDs? This article addresses the question by taking a close look at the new MAX II CPLD family and its look-up table (LUT) -based architecture.

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