

Welcome to the September issue of the *Inside Edge*. This monthly e-Newsletter gives you the latest news about Altera's products and solutions.

Monthly Spotlight

[Get New DSP Builder Version 2.2 & Accelerate Your DSP Design](#)

New release of Altera's DSP Builder software accelerates Stratix® II and Cyclone™ II FPGA-based DSP designs. DSP Builder version 2.2 expands access to Altera's DSP IP and fully supports the latest release of The Mathworks MATLAB/Simulink software. [Download Now](#)

FPGAs, CPLDs & Structured ASICs

[Stratix II FPGAs Have Industry's Fastest DDR2 SDRAM Interface](#)

Shipping since June, Stratix II FPGAs have the fastest DDR2 interfaces in the industry. As the only FPGAs with 533 Mbps DDR2 interfaces, Stratix II devices are performing above the 533 Mbps specification and offer customers significant guard band.

[Altera Achieves Industry's Highest FPGA Performance Using Quartus II](#)

Learn about the advanced technology in Quartus® II software that enables Altera customers to achieve the highest available performance for high-density FPGA designs, low-cost FPGA designs, and CPLD designs.

Software, Intellectual Property & Development Kits

[Download Service Pack 1 to Program MAX II & Stratix II Devices](#)

Service pack 1 for Quartus II software version 4.1 is now available for download. This release adds programming support for the first available members of the MAX® II CPLD and Stratix II FPGA device families and adds pin-out support for the new Cyclone II FPGA family.

[Order a Stratix II High-Speed Development Kit Today](#)

Altera designed the High-Speed Development Kit, Stratix II Edition for the development and rapid prototyping of applications that incorporate high-performance source-synchronous interfaces (such as SFI-4, XSBI, SPI-4.2, RapidIO™, and HyperTransport™ interfaces), PCI-X, and DDR2 SDRAM.

[Speed DSP Implementation--Get a Stratix II DSP Development Kit](#)

The Stratix II edition of the DSP development kit delivers a complete DSP development environment with a development board, DSP Builder version 2.2, Quartus II software, MATLAB/Simulink evaluation software, and IP. The board features analog interfaces targeting wireless, video, and audio applications.

Technology & System Solutions

[Learn about Altera's Newest Memory Solutions for Your Designs](#)

Altera's complete DDR, DDR2, and QDR II interface solutions help designers easily resolve issues through the design process, thereby lowering risks, maximizing performance, reducing design time, and accelerating time-to-market.

[Get Exclusive Pricing on Denali Memory Models](#) [Free Trial](#)

Altera and Denali have teamed up to provide a high-quality, low-cost solution for simulating

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and verifying DDR memory interfaces for Altera devices. Denali's memory models are the de facto standard for ASIC designs, and now they are available for Altera's FPGA and HardCopy® products.

[Find Answers Fast with the New Altera Toolbar--Download Now](#) **Free**

Download the new Altera Toolbar to get instant access to the Altera Support Center from your web browser.

Events, Training & Net Seminars

[Register Now: DDR2 Interface Design Net Seminar](#) **Free**

DDR2 SDRAM is the next evolutionary step for DRAMs. Attend this net seminar to learn how to implement high-speed DDR2-533 interfaces: hardware design and verification, timing and clock management, skew and noise reduction, and signal integrity management.

[Visit Altera at GSPx & Learn How to Optimize DSP Designs](#)

Attend a wide range of technical presentations on DSP solutions hosted by Altera and its partners in booth #205 at GSPx, September 27-30 in Santa Clara, California.

[Altera to Exhibit at IBC 2004 in Amsterdam September 9-14](#)

IBC is the leading event for broadcast professionals, with over 40,000 attendees and over 1,000 of the industry's leading companies participating. Altera and its partners will demonstrate integrated, cost-effective, performance-intensive video standard protocols implemented with Altera FPGAs.

[Learn to Optimize DSP Algorithms in Altera FPGAs](#)

Learn to map the mathematical operations of signal and image processing algorithms into Altera® FPGAs with this Altera training class. Implementation details, including performance/device resource tradeoffs through serialization, parallelization, and hardware acceleration for processors, are also discussed.

Recent Articles about Altera

[Stratix II FPGAs: A Case Study in Successful 90-nm Development and Rollout, Yahoo](#)

With the smooth rollout of the new 90-nm Stratix II devices, Altera has proven, once again, that a well-thought-out design methodology and choice of a mainstream process technology pays off. These high-density FPGAs are exceeding initial expectations for power and performance. [Read Article](#)

[Advantages of FPGA design methodologies, EE Design](#)

Discover some of the advantages of FPGA design methodologies over ASICs, including early time-to-market, easy transition to structured ASICs, and reduced NRE costs. [Read Article](#)

[FPGA Use in Software-Defined Radios, EE Times](#)

Read about the advantages of using FPGAs as co-processors in software-defined radio (SDR). [Read Article](#)

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