

December 2006 *Inside Edge*

Bringing you the latest Altera product and solution news.

## Monthly Spotlight

### [SI Prescription with Dr. Bogatin: "So, What Do You Do for a Living?"](#)

What do signal integrity engineers say when asked what they do—without getting blank stares? In his latest SI Prescription, Dr. Eric Bogatin lists entertaining answers SI engineers give. Read the SI Doc's column. If you have a question on SI, remember, the doctor is always in for you.

## FPGAs, CPLDs & Structured ASICs

### [Stratix III—The World's Fastest FPGAs](#)

With its fracturable LUT and high performance I/Os, Stratix III devices are the fastest FPGAs in the industry. Delivering a 25% performance boost over Stratix II devices, Stratix III FPGAs are the only ones that support DDR3/QDR2+ at 400 MHz with margin to spare.

### [Beat SONET Jitter with Stratix II GX Production FPGAs](#)

With the lowest power and highest number of functional transceivers, and the only FPGA with performance margins exceeding stringent OC48/STM16 jitter specs, Stratix II GX FPGAs are now available in production with a full complement of characterization reports and errata-free transceivers.

### [All Stratix II GX Family Members Shipping](#)

Shipments of the EP2SGX60 and EP2SGX30 complete the Stratix II GX family's initial rollout. Offering a complete solution for key protocols including PCI Express, SDH/SONET Serial RapidIO™, SDI, Gigabit Ethernet and XAUI Stratix II GX FPGAs are the right choice for line card and custom PCI Express endpoint applications.

### [Take Our Structured ASIC Survey—Enter to Win \\$50 on Amazon.com](#)

Altera invested in structured ASICs, because compared to standard-cell ASICs, they offer fast turn-around, high density and high performance. Tell us if you intend using structured ASICs in future projects. Take our survey for a chance to win one of three \$50 Amazon.com gift certificates.

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Literature Updates

## On the Edge



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See the world's first-ever comic devoted to the programmable logic industry.

## Inside Edge Poll

What would you do if you could start your career over?

[Take the Poll. See the results.](#)

## Did You Know...

Why was Bluetooth named "Bluetooth?"

[Find out.](#)

## Most Popular News from Last Issue

### [Introducing Stratix III—The Lowest Power High-performance FPGAs](#)

With 25% higher performance, 50% lower power and 2x the density of Stratix II FPGAs, Stratix III is the latest high-end FPGA family from Altera. Combined with Quartus II Software, Stratix III FPGAs provide the most productive high-end FPGA solution available anywhere.

## Software, Intellectual Property & Development Kits

### [Download Quartus II Software v6.1 Today—Free 30-Day Trial!](#)

Available today, you can download the Quartus® II Subscription Edition and Web Edition software v6.1. The Subscription Edition supports the Stratix® III device family and includes a 30-day trial.

### [Quartus II Software: #1 in Performance for 65-nm Devices](#)

Quartus II software v6.1 offers industry-leading performance for the new 65-nm Stratix III FPGA family and delivers a full speed grade advantage over competing high-end 65-nm FPGA designs. Go to the Website and discover all Quartus II v6.1 advantages for yourself.

### [Limited Time Offer: Big Discounts on PCI Express Solutions](#)

Take advantage of Altera's discount on PCI Express IP Cores. Now through the end of March, 2007, these items are hugely discounted from their normal prices. Also, ask about the PCI Express Development Kit, Stratix® II GX Edition available at no additional cost!

## Events, Training & Net Seminars

### [View the Stratix III FPGA Seminar and QuickCast. View the Future.](#)

In a 15-minute QuickCast, senior executives offer a high-level overview of Altera's new Stratix III FPGAs. Or view the 60-minute net seminar to learn how Stratix III FPGAs, with Programmable Power Technology, can help you achieve a 50% power savings and 25% performance improvement.

### [See Dr. Bogatin's High-Speed Board PDN Best-Design Practices](#)

Watch on-demand the net seminar, "Power Delivery Network (PDN) Best Design Practices for High-Speed Boards" presented by the Signal Integrity Doctor, Dr. Eric Bogatin. Learn how to establish PDN target impedance, select the right VRM and design a proper decoupling network for your system.

## Support & Literature

## [Design Example: C2H Compiler Accelerates FIR Filter](#)

Find out how the Nios® II C2H Compiler can be used to create a system that computes a symmetrical FIR filter algorithm 52 times faster than a software-only implementation. Download now.

### Altera in the News

#### [Far-flung teams craft 65-nm FPGA, EE Times](#)

Discover how this “third generation of the Stratix family grapples with the thorny downsides of 65-nm processes--specifically, leakage problems.”

#### [Altera unveils 65 nm Stratix III FPGA families and design tools, Programmable Logic Design Line](#)

Read about how “Stratix III devices address the '4Ps' of customer requirements: Power, Performance, Productivity, and Price.”

#### [Structured ASICs Are Alive and Well, Chip Design](#)

Structured ASICs offer the best of both worlds—fast turnaround like FPGAs with significantly lower cost and higher performance like standard-cell ASICs. This article discusses the path to the silicon portion of the solution and addresses design flow to offer real value.

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