

December 2007 *Inside Edge*

Bringing you the latest Altera® product and solution news.

Monthly Spotlight

[New MAX IIZ CPLDs Minimize Power, Space & Cost](#)

Maximize your advantage with Altera's new zero-power MAX® IIZ CPLDs. These non-volatile, instant-on CPLDs address the power, space, and cost constraints of today's portable applications, with the industry's lowest power consumption, ultra-small packages, and an affordable price.

FPGAs, CPLDs & Structured ASICs

[Video: Plug & Play Signal Integrity with Stratix II GX FPGAs](#)

With Altera's Plug & Play Signal Integrity, you can design systems with universal cards that plug into multiple positions in a system's backplane. You'll achieve optimal signal integrity automatically for each backplane position, without manual reconfiguration. See it in action now!

[Choose From Dozens of Cyclone III FPGA Die/Package Combinations](#)

Looking for a particular die/pin/package combination in a low-cost FPGA? Cyclone® III FPGAs are now available on the Altera eStore in sizes from 5K to 120K logic elements, from 144 to 780 pins, and in 5 different packages. Order your devices online now!

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Software, Intellectual Property & Development Kits

[New \\$399 Nios II Embedded Evaluation Kit, Cyclone III Edition](#)

Add remote configuration, LCD control, and Ethernet to your FPGA design while using the industry-leading hardware acceleration tool in this new evaluation kit. The included design examples help you get your system up and running fast. Buy your kit online today!

[Download Quartus II Software v7.2 SP1 for MAX IIZ Support & More](#)

Download service pack 1 for Quartus® II Software v7.2 for additional programming support for Cyclone III FPGAs, support for MAX IIZ CPLDs, and additional Windows Vista support for SOPC Builder and the Nios® II Embedded Design Suite. Download SP1 for the Quartus II software today!

[Save \\$495: Purchase Quartus II Software Before December 31](#)

Quartus II Subscription Edition software's fixed licenses and renewals are increasing in price—from \$2,000 to \$2,495—on January 1, 2008. Subscription



See New Device Availability

[Arria GX](#)

[Cyclone III](#)

[Stratix III](#)

Did You Know...

...How many worldwide holidays are celebrated in December?

[Find out.](#)



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Edition includes the IP Base Suite and much more. Buy Quartus II software online now or contact your local sales office.

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Technology & End Markets

[SI Prescription with Dr. Bogatin: A Midlife Kick for Copper](#)

Learn about the connector technologies that are breathing new life into copper cables and interconnects for high bandwidth, short-haul apps. Server farms' wiring harnesses and backplanes may benefit from new copper connectors with embedded signal processing. See how!

[Webcast: Addressing Size, Weight, and Power Constraints](#)

In today's military platforms, reducing systems' size, weight, and power (SWaP) is critical for operational life and budgetary constraints. Learn how FPGA advances are driving market expansion by extending mission life while reducing form factor and weight for better mobility and logistics.

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Events, Training & Net Seminars

[Essential Principles of Signal Integrity Class by Dr. Eric Bogatin](#)

Jan 17-18, 2008, High Wycombe, UK: Register for this two-day class to learn the foundations of signal integrity, taught by SI evangelist Dr. Eric Bogatin. This introductory class removes the math to reveal the underlying truth of how interconnects affect signal integrity.

[Webcast: Implementing High-Speed DDR3 Interfaces](#)

This 30-minute webcast discusses the challenges of implementing DDR3 and available solutions. View the webcast today to learn how to address read/write leveling in your DDR3 system, how to reduce power consumption on your board, and the JEDEC requirements for DDR3.

[New Training: Timing Analysis](#)

Starting Dec 12, various US locations: In this hands-on training, you'll learn how to constrain and analyze a design for timing, to write and manipulate SDC files for analysis, and to apply timing constraints to the design to guide placement and routing. Register today!

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Support & Literature

[White Paper: FPGA Power Challenges & Modeling Techniques \(PDF\)](#)

This white paper describes the major challenges associated with accurately predicting power consumption in FPGAs, while describing how you can overcome these challenges with the PowerPlay early power estimator and Quartus II PowerPlay power analyzer.

[White Paper: An SPR Framework for Development of SDR \(PDF\)](#)

Learn about a new FPGA development framework that leverages concepts found in software applications. Using software methodologies, this framework supports software-programmable reconfiguration (SPR) for FPGAs and is applicable to developing software-defined radio (SDR) applications.

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Altera in the News

[Interfacing FPGAs to DDR3 SDRAM Memories, EDN.com](#)

Without the leveling feature designed directly into FPGA I/O structures, interfacing anything to a DDR3 SDRAM DIMM can be complicated and costly. Learn about read/write leveling and how it works.

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Most Popular News from Last Issue

[Reference Design: Protect FPGA Designs from Theft](#)

Protect your low-cost, high-volume FPGA design! Using the "identification, friend or foe" design security approach, you can keep your design secure even if the configuration data bitstream is captured.

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