

July 2007 *Inside Edge*

Bringing you the latest Altera® product and solution news.

## Monthly Spotlight

### [Inspiration for embedded designs: Award-winning white papers](#)

Check out the top 18 white papers of the 2006 Nios® II Embedded Processor Design Contest, with finalists selected from over 500 entries. See how you can use Nios II processors in applications such as: encryption, image and audio processing, networking, security, and signal processing.

## FPGAs, CPLDs & Structured ASICs

### [Order the highest-density low-cost FPGA today](#)

Fit bigger designs on a low-cost FPGA with the Cyclone® III EP3C120 device. With its low power, low cost, and high functionality, these 120,000 LE FPGAs with 4 Mbits of memory are ready for your next cost-sensitive system.

[Back to Top](#)

## Software, Intellectual Property & Development Kits

### [Download the PCI Express High-Performance Reference Design](#) **Free**

View the extensive benchmarking results of the PCI Express x1, x4, and x8 IP core to see the extremely high sustained bandwidth achieved across multiple platforms. The reference design includes a chaining DMA for seamless high-speed transfers from system memory over a PCI Express link.

### [Order Nios II kits with triple-speed Ethernet solution](#)

Add triple-speed Ethernet to your application quickly and easily with Nios II development kits. These [Cyclone II](#) and [Stratix® II](#) kits now include Altera's Triple-Speed Ethernet IP core, TCP/IP network stack, PHY daughter board, and supporting design examples. Order today!

### [Download now—new Quartus II software v7.1 service pack 1](#)

When you download SP1 for Quartus® II software v7.1, you'll get pinout support for all Stratix III and Arria™ GX devices, POF support for Arria GX devices, and new BGA package support for Cyclone III devices. Download service pack 1 today!

[Back to Top](#)



## Did You Know...

...Which nation's employees get the most holidays?

[Find out.](#)



[Click to enlarge](#)

## Technology & End Markets

### [SI Prescription with Dr. Bogatin: House-changing flatwire cables](#)

No one wants unsightly cables routing around the living room. Wireless can't solve all problems, and small or thin cables haven't had the needed signal integrity over long distances. Check out this new cable--thin and flat enough to be painted over, with attenuation <0.6 dB/foot at 1 GHz.

[Back to Top](#)

## Events, Training & Net Seminars

### [QuickCast: Future proof with triple-rate SDI](#) **Free**

Ready to upgrade to the 1080p video standard? Learn how Altera's triple-rate SDI solutions, with support for SDI, HD-SDI, and 3G SDI, make upgrading easier. You'll also see how to future-proof your design so that moving to future video standards will be simple.

### [Net Seminar: Gigabit channel design guidelines](#) **Free**

Before you design another high-speed channel, be sure to watch this seminar. It reviews a channel model case study that addresses the challenges in designing for high data rates. You'll see detailed techniques to model an end-to-end channel simulation.

### [Training: Designing with Stratix III Devices](#)

August 15, Chelmsford, MA; August 22, San Jose, CA: This one-day training shows you how to use Stratix III architectural features, IP, and new power optimization innovations to build Stratix III systems. You'll also learn to implement high-speed external memory interfaces.

[Back to Top](#)

## Support & Literature

### [Constraining & Analyzing Source Synchronous Interfaces \(PDF\)](#)

If your timing margins are tight, Quartus II software has the tools you need to close timing with as few iterations as possible. Learn how to use the SDC format and TimeQuest timing analyzer to constrain and analyze high-speed interfaces quickly and efficiently.

### [From the Forum: How do I use a FIFO megafunction?](#)

Altera Forum user **uri** posted a question about simulating VHDL code in ModelSim® software while using a FIFO megafunction. See what other Forum users suggested that he try, then post your own questions, tips, and tricks today!

[Back to Top](#)

## Altera in the News

## [Time stamp your communications](#), Control Engineering

Hey, buddy, have you got the time? "Yes!" now that the IEEE 1588 standard PTP is available to industrial automation applications for precise time synchronization on Ethernet networks. See how to support the IEEE 1588 standard by implementing a triple-speed Ethernet MAC in an FPGA.

[Back to Top](#)

### Most Popular News from Last Issue

#### [Try Arria GX FPGAs with \\$995 development kit](#)

With the \$995 Arria GX development kit, you can design for PCIe, GbE & SRIO protocols, using proven Arria GX transceiver technology. The kit includes an Arria GX FPGA on a PCIe board, Quartus II design software, reference designs, and demos. Order yours from the Altera eStore today!

---

To ensure that you receive future issues of Inside Edge, please add [announcements@altera.com](mailto:announcements@altera.com) to your address book.

As a subscriber to the Inside Edge e-Newsletter, you will receive a monthly email newsletter. Altera respects your privacy. If you no longer wish to receive this e-Newsletter, please [unsubscribe](#).

[Subscribe](#) to additional Altera e-mail updates and e-Newsletters, or view/edit all of your Altera e-mail subscriptions. Altera e-mail communications include:

- Product Announcements & Updates
- Code:DSP e-Newsletter
- Embedded e-Newsletter
- Net Seminar e-Newsletter