

Monthly Spotlight

[New Signal & Power Integrity Tools for Stratix FPGAs](#)

Download the latest signal and power integrity tools for your high-speed board from the signal integrity center. These tools let you calculate SSN (with the Stratix® III early SSN estimator) and optimize your board-level power distribution network (with the updated PDN design tool.)



FPGAs, CPLDs & ASICs

[Webcast: New Gen2 PCI Express Hard IP for 40-nm Devices](#)

System architects need to weigh performance, capabilities, costs, reliability, and power consumption when implementing PCI Express. Learn how implementing PCIe on 40-nm Stratix IV FPGAs and HardCopy® IV ASICs helps balance these considerations, with special emphasis on Gen2 PCIe.



[Webcast: Cut Months and Millions from ASIC Design](#)

Complete your ASIC designs faster and at lower cost, while gaining unparalleled productivity, with Altera's unique system development method. In this 20-minute webcast, you'll see how HardCopy ASICs, Quartus® II software, and Stratix FPGAs can speed your time to market and cut costs.

See New Device Availability

[Arria® GX](#)
[MAX IIZ](#)
[Stratix III](#)

[Low-Power EPM570Z CPLDs for Portable Applications: Now Shipping!](#)

Now is a great time to buy low-standby power (32uA) MAX® IIZ CPLDs. Choose from three package options to fit your board: M100 (6x6 mm², 76 I/O), M144 (7x7 mm², 116 I/O), and M256 (11x11 mm², 160 I/O). Download no-cost Quartus II Web Edition software and design examples as well!

Did You Know...

What a fish, panda, flame, Tibetan antelope, and swallow have in common?
[Find out.](#)

Software, Intellectual Property & Development Kits

[Update to Service Pack 1 for Quartus II Software v8.0](#)

Download service pack 1 for Quartus II software v8.0 for additional programming support for the low-voltage Stratix III C4L (commercial) and I4L (industrial) FPGAs.

[PowerPlay Power Analysis and Optimization FAQ](#)

Are you taking full advantage of the Quartus II PowerPlay power analysis and optimization tools? Check out these frequently asked questions (and their answers!) to see what push-button PowerPlay technology can do for your design.



[Click to enlarge](#)

Technology & End Markets

[10-Gbps Ethernet Reference Design Now Available](#)

Need to design a system with 10-Gbps Ethernet connectivity? Altera's 10-Gbps Ethernet Reference Design is now available. It includes an IEEE 802.3ae standard-compliant 10-Gbps Ethernet MAC, 10GBASE-X PCS and

XAUI PMA. Contact Altera to get this reference design now!

[White Paper: DO-254 Support for FPGA Design Flows](#)

The DO-254 Design Assurance Guidance for avionics safety has a large impact on FPGA designs. Learn how to simplify your DO-254 certification burden in this white paper, then check out these other white papers for more information on FPGAs in military applications.

- [Military Benefits of the Managed Risk at 40 nm](#)
- [40-nm FPGAs and Defense Electronic Design Organizations](#)
- [Anti-Tamper Capabilities in FPGA Designs](#)
- [Military Productivity Factors in Large FPGA Designs](#)

Support & Literature

[Get Organized with the Quartus II Design Checklist](#)

Use the new Quartus II design checklist during design planning and implementation to ensure that you're using the methodology and settings you need to meet your design requirements. Print out a copy today!

[From the Forum: Timing Constraints for Serial Interface](#)

Altera Forum user **Ardni** asked about adjusting timing constraints for a serial interface, using Stratix II GX FPGAs. Read the comments and suggestions from other Forum users that helped answer his question, then post your own advice to gain Forum reputation today!

[White Paper: HW/SW Co-Verification with FPGA Prototyping](#)

Requirements for lower power, higher levels of integration, and greater SoC functionality present challenges for ASIC and ASSP development. This white paper explains how you can use FPGA prototyping systems to reduce time-to-market and development risk.

Events & Training

[Discover Altera's Complete Broadcast Solutions IBC2008](#)

Sept 12-16, Amsterdam, Holland: Visit Altera at the RAI Congress Centre, Hall 10, Booth A10, to learn about Altera's broadcast solutions. You'll see how Altera's technology helps you get broadcast equipment to market faster, at lower cost, and without compromising reliability.

[Training: Basics of Programmable Logic](#) **Free**

New to FPGAs? In this 1-hour online course, you'll learn:

- How programmable logic devices are programmed
- The differences between and advantages of CPLDs and FPGAs
- How to choose the right device technology for a design

[Register for One-Day PROFINET Training in North America](#) **Free**

PTO, the home of PROFINET and PROFIBUS, invites you to their

complimentary PROFINET training, where you can find out more about using FPGAs in industrial Ethernet systems. Selected cities also offer hands-on workshops to help you choose industrial Ethernet development tools. Register today!

Altera in the News

[Winning the Pinewood Derby—Using a CPLD to Get the Most from Your Cellular Handset](#), **Mobile Handset DesignLine**: CPLDs fit within the power and BOM budget of handset designs. Here's an example of how CPLDs are increasingly being used for QWERTY keyboard functionality.

Most Popular News from Last Issue

[Training: FPGA Designer Curriculum](#)

Looking for the basics of FPGA design? Altera's new FPGA Designer Curriculum will take you from an introduction to VHDL/Verilog, through Quartus II design software tutorials, interfacing with external memory, I/O pin assignments and timing analysis, to design optimization and more.

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