

January 2008 *Inside Edge*

Bringing you the latest Altera® product and solution news.

Monthly Spotlight

[Buy New Arria GX Development Kit Online](#)

Get started on your next PCIe, GbE, or SRIO design with a new Arria™ GX Development Kit. Only \$995, the kit includes everything you need to design transceiver-based Arria GX FPGAs: a full-featured board, design software, complete documentation, and reference designs.

FPGAs, CPLDs & Structured ASICs

[Webcast: Cut Power 100X Using CPLD Coprocessors in Portable Apps](#)

This 30-minute webcast gives examples of how to use the new MAX® IIZ zero-power CPLDs as power reduction coprocessors. Tune in to learn nine standard system functions where MAX IIZ CPLDs can be used to reduce power consumption in portable applications.

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Software, Intellectual Property & Development Kits

[New Cyclone® III Embedded USB 2.0 Development Board](#)

This new board from SLS is a ready-to-use, low-cost development platform with SLS IP cores, drivers, application software, and two reference designs to ensure easy implementation of USB 2.0 with reduced risk. Order your board from SLS online today!

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Technology & End Markets

[Webcast: Implementing Flexible Industrial Ethernet Solutions](#)

In this webcast, you'll learn how you can use low-cost FPGAs and the Nios® II processor to create a single, flexible hardware design that supports all industrial Ethernet standards, which protects your design from obsolescence. View the webcast today!

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Events, Training & Webcasts



See New Device Availability

[Arria GX](#)

[Cyclone III](#)

[MAX IIZ](#)

[Stratix III](#)

Did You Know...

...Which country's people enjoy the longest life expectancy?
[Find out.](#)



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[New Quartus II Software Interactive Tutorial](#) **Free**

This interactive tutorial teaches you how to use the basic components of the Quartus® II design software, including best-practice design flows, project management, and design tools, as well as programming a device with your thoroughly tested design.

[Advanced Digital Design & Test](#)

This online, three-course program from Worcester Polytechnic Institute focuses on complex digital systems and the design methods, tools, and languages required for modeling, simulation, and synthesis. Register today to learn about the evolving methodologies for design and test.

[DesignCon 2008: See the Only FPGA Built for DDR3 at 1,067 Mbps](#)

At DesignCon 2008, see how Altera's architectural innovations enable the highest I/O performance, best-in-class signal integrity, and low power consumption. View Altera's technical presentations & check out the booth to see DDR3 at 1,067 Mbps & a test chip showing 10G operation with margin!

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Support & Literature

[Design Example: Polyphase Modulation for Data Up-Conversion](#)

Download this DSP Builder design example to learn how to build a polyphase up-converter using Altera's FIR Compiler, NCO, and CIC IP cores. This example generates a carrier frequency that exceeds the NCO sampling frequency, easing requirements for analog modulation.

[Partitioning Your Design? Best Practices Ensure Best Results! \(PDF\)](#)

Partitioning for incremental compilation helps reduce compilation times and improve timing closure (see the [Resource Center](#) for more information). This app note provides best practices for setting up your design and creating good design partitions for the best results.

[Manage Skew at the I/O Elements in Your Stratix III Design \(PDF\)](#)

Manually configuring the I/O delay elements in Stratix® III FPGAs can help in some applications, such as memory interfaces. This app note explains the various programmable delays in Stratix III I/O pins and shows options for configuring them using the Quartus II software.

[Alternative Nios II Boot Methods \(PDF\)](#)

Many boot up configurations are possible when using the Nios II embedded processor. A boot copier locates application software in non-volatile memory, copies it to RAM, and initializes the system. This app note shows how to implement custom boot software with the Nios II processor.

[Performing Equivalent FPGA Timing Analysis Accurately \(PDF\)](#)

This white paper is a "must-read" before you start your next FPGA benchmark comparison! You'll learn how to configure the available timing analyzer tools (Altera TimeQuest and Xilinx Trace) to perform equivalent timing analysis and to accurately interpret the benchmarking results.

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Altera in the News

["Oooohhh, shiny...what is it...and where can I get one?", Programmable Logic DesignLine](#)

"I am rather impressed," wrote Clive Maxfield of *Programmable Logic DesignLine*, about the new Nios II Embedded Evaluation Kit. See what he liked about the "cool" touch-screen interface, demo applications, and drop-in design examples, then [order one for yourself!](#)

[Stratix III FPGAs Achieve 533-MHz DDR3 Spec, EETimes](#)

Stratix III FPGAs recently achieved DDR3 memory interface speeds in excess of 1,067 Mbps. This higher memory bandwidth enables new computing, communications, and video processing applications that were previously impossible or required twice the memory banks. Read more in EETimes.

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Most Popular News from Last Issue

[New MAX IIZ CPLDs Minimize Power, Space & Cost](#)

Maximize your advantage with Altera's new zero-power MAX IIZ CPLDs. These non-volatile, instant-on CPLDs address the power, space, and cost constraints of today's portable applications, with the industry's lowest power consumption, ultra-small packages, and an affordable price.

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