

Monthly Spotlight

[White Paper: Increase Productivity With Incremental Compilation](#)

See how incremental compilation can significantly reduce compile time and preserve performance in your designs. Through four design scenarios, this white paper shows how incremental compilation increases your productivity.



FPGAs, CPLDs & ASICs

[Stratix IV FPGAs: Think AND, not OR](#)

Don't think high density, high performance, OR low power with your FPGA; think high density, high performance, AND low power! With 680K logic elements, 8.5-Gbps transceivers, and Programmable Power Technology, you don't need to compromise. With Stratix® IV FPGAs, think AND, not OR.

[Stratix III LVDS Now Runs at 1.6 Gbps](#)

Now you can design for even higher speed LVDS data rates--Stratix III FPGA True-LVDS is now specified for 1.6-Gbps operation. Take advantage of these higher rates in your next design!

[Webcast: Reach New Levels of SoC Integration](#)

FPGAs are an ideal platform for SoC integration due to their inherent flexibility and time-to-market advantages. View this webcast to learn the 3 most important high-end digital system requirements, how transceiver quality affect system bandwidth, and more.

Software, Intellectual Property & Development Kits

[Purchase Quartus II Subscription Edition & Get DSP Builder Free](#)

Purchase Quartus® II Subscription Edition online and get DSP Builder at no cost. That's a \$4,490 value for only \$2,495! Quartus II Subscription Edition software offers up to 70% faster compilation times and 2X faster simulation than Web Edition. Offer expires August 3, so purchase today!

Events & Training

[Training: DSP Designer Curriculum](#)

Need to design a DSP electronic system with an FPGA? Learn how with Altera's DSP Designer Curriculum. You'll use DSP Builder to create DSP designs and perform system simulations, and then work with FIR, NCO, and FFT MegaCore® functions to get your system running. Start today!

[Training: 3 Protocol Solutions Courses for Stratix IV GX FPGAs](#)

Learn to design high-speed protocols with these new online courses:

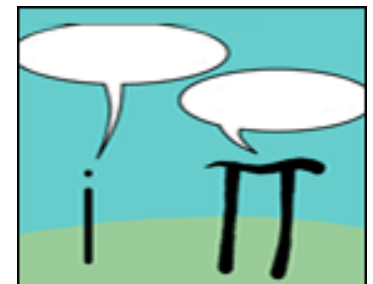


See New Device Availability

[Arria® GX](#)

[MAX IIZ](#)

[Stratix III](#)



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- [PCI Express Design with Stratix IV GX FPGAs](#)
- [Ethernet Design with Stratix IV GX FPGAs](#)
- [Serial RapidIO® Design with Stratix IV GX FPGAs](#)

[Register for the Asia Pacific Technology Roadshow 2008](#)

July 2-29: Altera's annual technology-focused seminars are coming to 12 cities around the Asia Pacific. Come learn about the latest 40-nm technology, and see how Altera facilitates your DSP and embedded designs. Join us for a chance to win a Nios® II Embedded Evaluation Kit!

Support & Literature

[App Note: Implementing an LCD Controller \(PDF\)](#)

This new application note shows how to create an LCD module for your embedded design. The example used is based off the Nios II Embedded Evaluation Kit and includes background information on the LCD subsystem and porting guidelines. Download today.

[Quartus II Documentation is Now Easier to Navigate!](#)

Check out this one-stop shop for technical documentation on design, synthesis, implementation, optimization, and verification using the Quartus II software, including SOPC Builder. You'll find this new handbook web page is better-organized and easier to navigate than ever!

[From the Forum: How should I use LVDS?](#)

Altera Forum user **stephenzhou** asked about LVDS pin connections in Cyclone® family. Read the comments and suggestions from other Forum users that helped answer his question, then post your own advice to gain Forum reputation today!

Altera in the News

[MAX IIZ CPLDs go to Beijing Olympics, Mobile Handset DesignLine](#)

For the 2008 summer Olympics, MAX® IIZ CPLDs were chosen for use in portable handsets for identification, logistics, and more. Huayu Communications chose MAX IIZ CPLDs for their security, power, and cost advantages. Read more about MAX IIZ CPLDs in portable devices.

Most Popular News from Last Issue

[Training: FPGA Designer Curriculum](#)

Looking for the basics of FPGA design? Altera's new FPGA Designer Curriculum will take you from an introduction to VHDL/Verilog, through Quartus II design software tutorials, interfacing with external memory, I/O pin assignments and timing analysis, to design optimization and more.

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