

Monthly Spotlight

[New 40nm Portfolio with Stratix IV FPGAs and HardCopy IV ASICs](#)

With Altera's new 40nm portfolio, you don't have to settle for one benefit over another—you can think AND, not OR. Get high density AND performance with the lowest power, the benefits of both FPGAs and ASICs, AND high-performance design software optimized for compile times.

Introducing 40 nm

Stratix IV

HardCopy IV

think **AND** not OR

FPGAs, CPLDs & ASICs

[Video Demo: 40nm FPGA and 8.5 Gbps Transceiver](#)

Watch this 4-minute video to see Altera's new 40nm FPGA demos showcasing 1.5-Gbps LVDS performance and an 8.5-Gbps transceiver operating with excellent signal integrity. You'll see how pre-emphasis and equalization improve signal integrity.

[Webcast: Introducing Altera's 40nm Portfolio](#)

Challenges for today's high-end digital systems include increasing performance, reducing power consumption, and increasing system bandwidth and integration. Learn how to overcome these challenges with the 40nm portfolio, including Stratix® IV FPGAs and HardCopy® IV ASICs.

[Partner Webcast: Transceiver-Based Channel Modeling with Agilent](#)

Thursday, June 26, at 10 AM Pacific Time: This live webcast demonstrates real-world circuit boards using S-parameters to predict eye-opening performance before a system is physically prototyped. Stratix II GX transceiver models in Agilent ADS will show 6.375-Gbps performance.

Software, Intellectual Property & Development Kits

[New Quartus II Software v8.0 Available - Download Now](#)

Download the newest version of Quartus® II software. Version 8.0 includes an average 3X faster compile times when compared to the nearest competitor, a 2-speed grade advantage, and the highest logic utilization in the industry for high-end FPGAs. Download today!



See New Device Availability

[Arria® GX](#)

[MAX IIZ](#)

[Stratix III](#)



Technology & End Markets

[Increase Performance in Video & Image Processing Apps \(PDF\)](#)

Learn how an FPGA-based JPEG2000 implementation addresses the needs of the JPEG2000 standard, and demonstrates significant performance, cost, and integration benefits over ASSP- or digital signal processor-based options.

Events & Training

[Training: FPGA Designer Curriculum](#)

Looking for the basics of FPGA design? Altera's new FPGA Designer



[Click to enlarge](#)

Curriculum will take you from an introduction to VHDL/Verilog, through Quartus II design software tutorials, interfacing with external memory, I/O pin assignments and timing analysis, to design optimization and more.

[Partner Course: Advanced Digital Design and Test from WPI](#)

This 10-week online graduate course on Digital Systems Testing and Testable Design discusses faults and fault modeling, test equipment, sequential circuits, fault simulation, memory testing, design for testability, boundary scan, and more. Starts in June, so sign up today!

Support & Literature

[From the Forum: Cyclone III Starter Kit Compilation Error](#)

Altera Forum user **Saider72** asked about a compilation error he receives when designing for a Cyclone® III starter kit and Terasic NEEK upgrade kit. Read the detailed suggestions from other Forum users that helped answer his question, then post your own advice on the Forum today!

Altera in the News

[Analysis of 40nm Stratix IV & HardCopy IV Products](#)

Altera's May 19 announcement of the industry's first 40nm FPGAs and ASICs generated a lot of excitement in the press:

- ["Give me strength! New FPGA has 2.5 billion transistors!"](#)
EETimes.com
- ["40nm FPGA video,"](#) Embedded.com
- ["Analyst comments on Altera's 40nm FPGAs,"](#) EETimes.com
- ["40nm Altera Stratix IV,"](#) FPGA Journal

[Under the Hood: Inside Sony's OLED TV, EETimes](#)

Check out a recent video teardown of the Sony XEL-1 TV to see which devices the consumer giant selected to speed the world's first organic LED (OLED) TV to market. When rapid innovation at the lowest cost is required, there's no substitute for Cyclone FPGAs and MAX® CPLDs.

Most Popular News from Last Issue

[Video Demo: Compare Stratix III & Virtex-5 Core Power Consumption](#)

Watch a side-by-side comparison of Stratix III FPGAs and Virtex-5 to see how, with Programmable Power Technology, the Stratix III logic fabric consumes less core power. You'll also see how Stratix III FPGAs consume the lowest possible power without compromising performance.

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