

Monthly Spotlight

[Design Example: Say Goodbye to Your Configuration Controller](#)

Configure your FPGA design without a configuration device. Download the Application Selector Design Example to learn how, using your Nios® II Embedded Evaluation Kit. The "[Configuring Cyclone® III Devices](#)" chapter of the Cyclone III Handbook provides helpful details.



FPGAs, CPLDs & ASICs

[Industrial-Temperature Cyclone III FPGAs Now Shipping](#)

Ready to roll out your design, using industrial-temperature Cyclone III FPGAs? Over 50 industrial-grade and 100 commercial-grade Cyclone III devices are now available for shipment. Get yours today!

[Zero-Power MAX IIZ CPLDs Now Shipping](#)

MAX® IIZ EPM240Z CPLDs are now available to buy online. You can reduce power consumption and save space on your next board with these devices that come in ultra-small packages.

Software, Intellectual Property & Development Kits

[Buy Quartus II Software Online & Save Up To \\$500 on Training](#)

Buy a Quartus® II software subscription by March 31, 2008, and save up to \$500 on Altera software training courses. Quartus II software is #1 in productivity and performance, so you'll hit the ground running and get your design out the door in no time.

[See RapidIO IP Interoperate with TI DSP](#)

Check out this example of a serial interface between a Stratix® II GX FPGA and Texas Instruments 6482 digital signal processor, using Altera's RapidIO® MegaCore® function. Download the complete design files, as well as a step-by-step application note, today!

[Evaluate the New Triple Speed Ethernet \(TSE\) Reference Design](#)

Create this SOPC Builder system that demonstrates Ethernet network traffic using two IP cores and Stratix II GX transceivers. The reference design showcases maximum wire speed operation with packet generators and checkers that send, receive, and check Ethernet packets through hardware.

Technology & End Markets

[Webcast: Accelerating OFDMA-MIMO Wireless System Design](#)

Learn how to accelerate OFDMA-MIMO wireless system design in this new webcast. You'll learn about the latest channel card and RF card IP, reference designs, and development boards useful for WiMAX and LTE basestation development. View now!



See New Device Availability

[Arria GX](#)
[Cyclone III](#)
[MAX IIZ](#)
[Stratix III](#)

Inside Edge Poll

How do you read your work email?

[Take the Poll. See the results.](#)



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[Webcast: FPGAs in Ultra Low Power Applications](#)

Join Altera, Arrow, and Linear Technology as they examine the Low Power Reference Platform and prove that FPGAs really can run on batteries.

Events & Training

[New ASIC-to-FPGA Designer Training Curriculum](#)

Are you a hardware engineer with experience designing ASICs? Would you like to use your VHDL or Verilog HDL skills to design for FPGAs? Check out this course-by-course curriculum that lists every class you need to become an expert FPGA designer.

[Visit Altera at the 2008 ESC Silicon Valley](#)

April 14-18, San Jose, CA: Visit the Altera booth at this year's Silicon Valley Embedded Systems Conference for tips on improving your embedded designs. You'll have the opportunity to check out our kits, participate in technical training, and test drive our latest software.

[Visit Altera at NAB'08 to Accelerate 1080p Video Development](#)

April 14-17, Las Vegas, NV: As the broadcast industry adopts 1080p video, OEMs aim at delivering the best quality video on time. See how Altera's 1080p solutions enable rapid development from concept to product so you can focus on your core expertise.

Support & Literature

[On-Chip Debug Using SignalTap II State-Based Triggering](#)

The state-based triggering flow allows you to define a custom triggering flow to organize your triggering conditions. These 15 design examples provide templates for common triggering flow scenarios. Use them to improve productivity in your chip debug and verification cycle.

From the Forum: [How to Implement a Histogram in an FPGA](#)

Altera Forum user **bertronicom** needs to create a histogram for a 2D image. Read the comments and suggestions from other Forum users that helped answer his question, then post your own advice to gain Forum reputation today!

[Download New Stratix II GX SPICE Design Kits](#)

New multi-gigabit transceiver SPICE kits are now available on the web for Stratix II GX FPGAs. Each easy-to-download kit includes a set of encrypted models, sample decks, and user guides. Start simulating with Agilent, Cadence, Mentor Graphics, and Synopsys tools today!

Altera in the News

[IEC Announces Winners of DesignVision Awards](#), EDA Café

Stratix III FPGAs received the International Engineering Consortium's DesignVision award in the Semiconductor and IC category. Stratix III FPGAs were recognized for their unique and innovative architecture and

DDR3 memory interface.

Most Popular News from Last Issue

[Download Seven Winning White Papers \(PDF\)](#)

Chosen from hundreds of entries to the 2007 "Innovate Nordic Design Contest," these winning white papers show how engineers use Altera's IP, tools, and development kits to build market-specific applications.

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