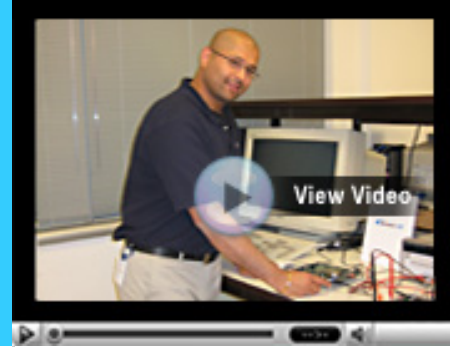


## Monthly Spotlight

### [Video Demo: Compare Stratix III & Virtex-5 Core Power Consumption](#)

Watch a side-by-side comparison of Stratix<sup>®</sup> III FPGAs and Virtex-5 to see how, with Programmable Power Technology, the Stratix III logic fabric consumes less core power. You'll also see how Stratix III FPGAs consume the lowest possible power without compromising performance.

[Read more...](#)



## FPGAs, CPLDs & ASICs

### [New Enhancements to Arria GX FPGAs with Transceivers](#)

Arria<sup>™</sup> GX FPGAs now offer 3.125-Gbps transceivers, support for 6 new protocols, and channel equalization settings. In addition to PCIe, GigE, and SRIO, Arria GX FPGAs support SDI, XAUI, CPRI, OBSAI, and SerialLite protocols, and Basic mode. See what Arria GX FPGAs can do for you now!

[Read More...](#)



## Software, Intellectual Property & Development Kits

### [New Cyclone III FPGA-based 1080p Video IP Development Kit](#)

The new ViClaro III Development Kit from Microtronix accelerates your development of next-generation HD 1080p HDTV sets or flat panel display systems. The EP3C120 Cyclone<sup>®</sup> III FPGA, featured in the kit, provides logic and interface resources for advanced video processing IP algorithms.

[Read More...](#)

See New Device Availability

- [Arria GX](#)
- [MAX IIZ](#)
- [Stratix III](#)

## Technology & End Markets

### [Video Demo: Build up to 96-Port SGMII GigE with Stratix III FPGAs](#)

View this video to see how, with Stratix III FPGAs, you can quickly build communications systems with up to 96 Ethernet links, while meeting jitter and tolerance requirements. Stratix III FPGAs support SGMII GigE operation on LVDS I/O pins at 1.25 Gbps. Watch it work!

[Read More...](#)

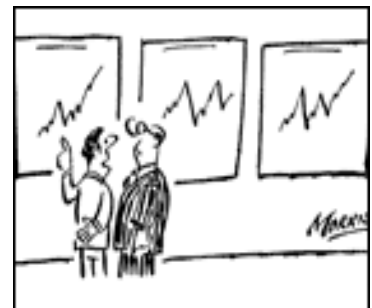


## Events & Training

### [Dr. Eric Bogatin Teaches "Taming Signal Integrity"](#)

May 20, Winnersh, UK: Join this practical class to learn the best way to design systems with clock frequencies over 100 MHz. Dr. Bogatin will show how to accelerate the interconnect design process and create design rules that balance performance with cost, risk, and schedule.

[Read More...](#)



[Click to enlarge](#)

### [Training: High-Speed I/O Designer Curriculum](#)

Need to design a board with multi-gigabit transceivers on an FPGA? Learn

how with the High-Speed I/O Designer Curriculum. The curriculum's classes step you through signal integrity issues, implementing RapidIO™ and other IP cores, dynamic reconfiguration, and more!

[Read More...](#)

## Support & Literature

### [From the Forum: Quartus II Internal Memory Initialization](#)

Altera Forum user hapyang asked about implementing and initializing internal memory in the Quartus® II design software. Read the comments and suggestions from other Forum users that helped answer his question, then post your own advice to gain Forum reputation today!

[Read More...](#)

## Altera in the News

### [Reduce Power by Adding Hardware Accelerators, Embedded.com](#)

The rule of thumb in embedded system design has been that adding hardware increases power demands. The careful use of hardware accelerators, however, inverts the rule: adding hardware can reduce power. Read the article to see for yourself.

[Read More...](#)

## Most Popular News from Last Issue

### [OpenCore Designs Show Increased Stratix III Advantage vs Virtex-5](#)

See for yourself! Benchmarks on 7 large, popular OpenCore designs show that as design sizes increase, Stratix III FPGAs are up to 65% faster, can fit an average 46% more logic, and compile up to 9x faster than Virtex-5. Learn more, download the design files, and run the benchmarks yourself!

[Read More...](#)

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