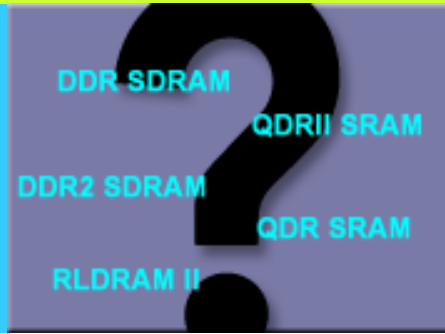


Monthly Spotlight

[White Paper: Selecting the Right High-Speed Memory Technology](#)

Learn about high-speed memory selection criteria, the options available, and applications where each option is used. In addition, you'll see the strengths and weaknesses of each option, the functions they perform in high-end systems, and which Altera FPGAs to use with each one.



FPGAs, CPLDs & ASICs

[Webcast: Manage Performance & Power Using 40-nm FPGAs](#)

In this 30-minute webcast, get a behind-the-scenes look at new technologies such as strained silicon and triple-gate oxide, new transceiver technology for the highest system bandwidth, and power optimization via the FPGA architecture and design software. View now!

[Webcast: Building High-Speed FPGA Memory Interfaces](#)

View this 15-minute webcast to explore new 40-nm FPGA architectures built for reliable high-speed memory interface operation. You'll learn how to use IP to quickly and easily build memory interfaces, and how soft IP buys back timing margin by reducing timing variations. View now!

Software, Intellectual Property & Development Kits

[Hardware Debugging of SOPC Builder Systems with System Console](#)

The new System Console tool, introduced in Quartus® II software v8.0, provides access to hardware modules instantiated on your FPGA. This user guide shows how and why to use the System Console, along with quick-start design examples. Check it out today!

[Webcast: Improve Productivity with the Right FPGA Software](#)

As FPGA compile times get longer and timing closure becomes more difficult, the key to a product's success is in choosing the right design software. In this webcast, you'll learn about software technologies that maximize performance and productivity throughout the design process.

Technology & End Markets

[New Industrial Ethernet Online Training](#) Free

Interested in industrial Ethernet? In this 30-minute online course, learn how to implement industrial Ethernet in FPGAs. You'll see what new resources are available today to help you implement your own flexible industrial Ethernet solution.

[Webcast: Understand & Control Costs in Military FPGA Designs](#)

Designers of military electronics are faced with unique technical and cost

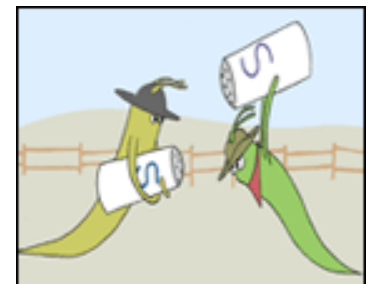


Featured Development Kits

[Arria® GX Dev Kit](#)

[Cyclone® III FPGA Kit](#)

[Nios® II Evaluation Kit](#)



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design risks. This webcast looks at ways to mitigate these risks using high-end software tools, the impact of software productivity on defense program costs, and how an efficient software flow saves money.

Events & Training

[Design Partition Planner in the Quartus II Software Training](#)

Learn to make informed design partition choices for better results. You'll

- Know when to use the design partition planner
- Use the partition planner with other advanced software tools
- Manage design partitions effectively for optimum design results

[October, Asia-Pacific: Register for SOPC World 2008](#)

Power down and speed up at this year's SOPC World conference and exhibition. These one-day events, hosted in five cities across the Asia/Pacific region, will focus on power-efficient semiconductor solutions. Register today to reserve your spot!

Support & Literature

[From the Forum: Instantiation Components Compile Error](#)

Altera Forum user **chmosiii** was getting a confusing Quartus II component instantiation compilation error. Read the comments and suggestions from other Forum users that helped answer his questions, then post your own advice to gain Forum reputation today!

[Multicycle Timing Exceptions Made Simple \(PDF\)](#)

Multicycle exceptions can help relax timing constraints, improve the quality of results, and decrease design compile times by allowing the Quartus II fitter to optimally place and route an FPGA design. Learn how to easily implement multicycle exceptions with TimeQuest in this app note.

[Attention Xilinx Users: Migrate Easily to Altera \(PDF\)](#)

Would you like to convert your Xilinx ISE design to Altera's Quartus II software? This app note shows the equivalent tool flows between the two software tools, and provides design conversion guidelines with device and design constraints. Start your design conversion today!

[TimeQuest Cookbook: SDC Examples and Recipes \(PDF\)](#)

This "cookbook" provides quick and easy-to-use Synopsys Design Constraint (SDC) files for various FPGA design scenarios. Constraint example topics include clocks, I/O constraints, system synchronous outputs, exceptions, and JTAG signals. Try them today!

Altera in the News

[Altera Receives Rockwell Collins' Supplier of the Year Award](#)

Rockwell Collins named Altera its #1 supplier over 10,000 others in their supply chain when it awarded Altera the 2008 President's Award. The award

is based on quality, product excellence, supplier performance, and teamwork to meet Rockwell Collins' specific needs.

Most Popular News from Last Issue

[New Signal & Power Integrity Tools for Stratix FPGAs](#)

Download the latest signal and power integrity tools for your high-speed board from the signal integrity center. These tools let you calculate SSN (with the Stratix® III early SSN estimator) and optimize your board-level power distribution network (with the updated PDN design tool.)

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- Embedded newsletter
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