

Monthly Spotlight

[40nm Dev Kit Shows 8.5Gbps XCVR With Optimized Signal Integrity](#)

Evaluate transceiver performance up to 8.5 Gbps with our new Transceiver Signal Integrity Development Kit, Stratix® IV GX Edition. The kit enables a thorough assessment of transceiver interoperability and serializer/deserializer (SERDES) signal integrity. Pre-order today!



FPGAs, CPLDs & ASICs

[Webcast: 40-nm FPGA Transceiver & Clocking Architecture](#)

This 40-minute webcast, presented by Dr. Mike Peng Li, discusses transceiver architecture and clocking in 40-nm Stratix IV GX FPGAs and HardCopy® IV ASICs. Learn about clock generation and recovery, jitter reduction with advanced oscillators, and powering analog circuits.

[Watch Stratix IV GT Transceivers Running at 11.3 Gbps](#)

This 5-minute video shows six lanes of a Stratix IV GT FPGA's transceivers running at an industry-leading 11.3 Gbps. You'll see clear results from the eye diagram and jitter performance analysis.

[White Paper: Avoid PCB Design Mistakes \(PDF\)](#)

In FPGA-based systems, managing the multitude of PCB-related design issues is compounded by the size, complexity, and programmable nature of the FPGAs themselves. This paper discusses the factors that must be considered in order to achieve a high-quality FPGA-based PCB design.

Software, Intellectual Property & Development Kits

[Download Quartus II Software Faster with Altera Installer](#)

Speed up software downloads when you cut the size of download files by up to 50% with the new Altera Installer. With the Altera Installer, you can download and install only the Quartus® II software and related files that you need for your design's device family. Try it today!

[Manage Metastability Using Quartus II Software \(PDF\)](#)

The Quartus II software provides industry-leading features that analyze potential metastability issues in your designs' asynchronous signal transfers. Identify synchronizers to see the mean time between failures (MTBF) and optimize your design for better metastability MTBF.

Technology & End Markets

[White Paper: Multi-Rate Video Interfaces for Broadcast \(PDF\)](#)

As high-definition video is established as the standard for video broadcast, new production equipment must cope with the 1080p video interface while also handling the legacy of standard definition and 1080i interfaces. See how it can be done in this white paper.

[White Paper: Video Processing for Military Infrared Apps \(PDF\)](#)

This white paper explores Altera's low-power FPGA platform with video design solutions that address the military's complex, power-budget-constrained EO/IR design challenges and significantly increase designer productivity.

Events & Training



Popular Literature

[Altera Product Catalog](#)

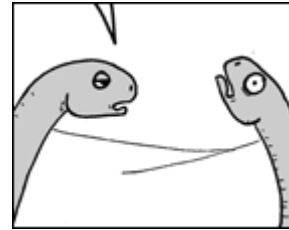
[Embedded Processor Portfolio](#)

[HardCopy ASICs: Technology for Business](#)



[High-Speed Serial Protocol Design with 40-nm FPGAs](#) **Free**

View this 2.5 hour online course to learn serial design techniques for data rates over 10 Gbps. You'll learn to configure high-speed serial transceivers for a customized protocol, use Altera's manual transceiver tool, and interface custom serial protocols to embedded transceivers.



[Click to enlarge](#)

Support & Literature

[White Paper: Remote Radio Heads and the Evolution to 4G Networks](#)

This white paper demonstrates design techniques for digital IF signal-processing functions such as DUC/DDC, CFR, and DPD. Using this methodology and IP blocks minimizes FPGA resources while keeping the flexibility required for simultaneous multi-standard operation.

[High-Speed Board Design Resource Center](#)

Visit Altera's improved board design guidelines resource center! This single-site information source will help you implement successful high-speed PCBs. Visit today for information about board stack-up, routing guidelines, models, tools and more.

[Quartus II Installation & Licensing for Windows & Linux \(PDF\)](#)

Read all the requirements and instructions related to downloading, installing, and licensing the Quartus II software for Windows and Linux in one handy manual.

[From the Forum: Linking Two FPGAs](#)

Altera Forum user **studtlc** asked how to connect a single block of the first FPGA with a block of the second one. Read the comments and suggestions from other Forum users that helped answer his question, then post your own advice to gain Forum reputation today!

[White Paper: Assessing FPGA DSP Benchmarks at 40 nm \(PDF\)](#)

Understanding and using reliable device benchmarks for system decisions is essential for scientific and military applications. This white paper examines these benchmarks to help designers decide which conditions or benchmark figures are most important for their design.

Altera in the News

[How to Control Analog Output from a CPLD Using a Pulse Width Modulator](#), [pldesignline.com](#)

This article shows how a CPLD can replace a digital-to-analog converter, allowing it to drive an audio speaker or control things like LED intensity, motor speed, and servo position.

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