

May 2009

www.altera.com

Monthly Spotlight

[White Paper: Using FPGAs to Render Graphics and Drive LCDs](#)

Learn to use FPGAs to add a LCD and GUI display to any embedded system. This approach is scalable and graphics can be generated by any external processor, embedded processor, or hardware graphics acceleration engine in the same FPGA.



FPGAs, CPLDs & ASICs

[Migrate Your Stratix III FPGA Designs to Stratix IV E FPGAs](#)

Future-proof your Stratix[®] III FPGA designs to take advantage of the higher performance, higher density, and lower power consumption of Stratix IV E FPGAs

[Video: Analyze Transceiver Interoperability & Signal Integrity](#)

In this new 8-minute video, see how to evaluate the Stratix IV GX transceiver's interoperability and SERDES signal integrity. You'll view performance differences between 3- and 40-inch board traces, learn about bit-error ratios, and see how to monitor power consumption.

[Stratix IV GX FPGAs Achieve PCI Express Version 2.0 Compliance](#)

Stratix IV GX FPGAs successfully completed PCI-SIG testing procedures and achieved compliance for Gen1 and Gen2 x1, x4, and x8 lane configurations. Stratix IV GX FPGAs have up to four PCIe hard IP blocks, supporting both PCIe Gen1 and Gen2 endpoint and root port functions.

Software, Intellectual Property & Development Kits

[Download Quartus II Software v9.0 Service Pack 1 Now!](#)

Download Quartus[®] II v9.0, service pack 1 for:

- Programming support for the Stratix IV GX EP4SGX530 ES FPGAs
- Advanced support for the new Stratix IV package options
- Compilation support for HardCopy[®] III and HardCopy IV E ASICs

[Order New PCI-SIG Compliant Stratix IV GX FPGA Development Kit](#)

Altera's Stratix IV GX FPGA Development Kit delivers a rapid prototyping environment for serial protocols such as PCI Express 2.0, 10 Gigabit Ethernet, CPRI/OBSAI, Serial RapidIO, and HD/SD SDI. Order your kit today!

Technology & End Markets

[Learn About MotionFire Motor Control Platform](#)

View this video from National Semiconductor's PowerWise Design TV series that features the MotionFire FPGA-based motor control development platform. The platform demonstrates Cyclone[®] III FPGAs' design flexibility and addresses energy efficiency. View today!

Events & Training

[Attend Hands-On Transceiver Portfolio Workshops](#) Free

Starting June 9, throughout Europe: Learn about silicon, board, and system solutions to help you achieve optimal signal integrity in your high-speed serial applications. Take part in hands-on labs and see product demos featuring the latest 40-nm FPGAs. Register today!

Poll

[Do you use Facebook, LinkedIn, Twitter...?](#)

Purchase
Quartus[®] II Software
and Get Nios[®] II
Processor for Free
Limited Time Offer
Buy Now! ▶

Popular Videos

[Developing Software for Embedded Systems on FPGAs](#)

[Plug & Play Signal Integrity for FPGAs with Transceivers](#)

[40-nm FPGA and 8.5-Gbps Transceiver Demo](#)

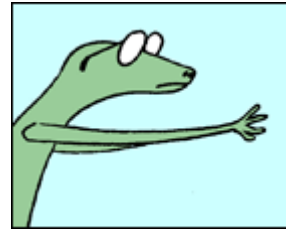
[Quartus II Software Design Training: Foundation](#)

Learn to use new features in Quartus II software version 9.0:

- Plan and develop an FPGA or CPLD, including device I/O assignments

- Create and compile projects with clock and I/O constraints

- Analyze clock and input/output timing using TimeQuest Analyzer



[Click to enlarge](#)

Support & Literature

[From the Forum: SystemVerilog Supported by Quartus II Software?](#)

Altera Forum user **Learner_08** asked how to run SystemVerilog design files in Quartus II software. Read the comments and suggestions from Forum users that answer his question, then post your own questions and advice to gain Forum reputation today!

[Analyze and Optimize SSN in the Quartus II Software \(PDF\)](#)

To compute SSN on each pin of your design, the Quartus II SSN Analyzer uses circuit simulation on your design's I/O placements. The integrated Pin Planner tool helps correct pins with SSN issues. SSN optimization tools within the Quartus II software also improve SSN levels.

[White Paper: Automating DSP Simulation and Implementation \(PDF\)](#)

Military sensor-driven systems normally use FPGAs to interface to the analog-to-digital converters (ADCs) used to digitize sensor inputs. Since ADCs require up to 3 MSPS, they need high-performance DSP circuitry. See how to automate optimal implementation of DSP algorithms in an FPGA.

[White Paper: Ethernet-Over-NG-SONET/SDH for MSPP Linecard \(PDF\)](#)

Use the combination of Arria[®] II GX FPGAs with TPACK's 2.5-Gbps/10-Gbps Ethernet-over-SONET/SDH and 10-Gbps/20-Gbps Switch/NPU solutions to meet the requirements of next-generation MSPP linecards and maintain your existing infrastructure.

Altera in the News

[Flexibility in the Palm of Your Hand, Portable Design News](#)

Bring handheld products to market first and with the most desirable feature set. In this article, see how you can use low-power FPGAs and zero-power CPLDs to meet power consumption requirements and keep the highest level of flexibility without time-to-market tradeoffs.

[Building 'Image Format Conversion' Designs, FPGA Journal](#)

Image format conversion (IFC) can be implemented in broadcast systems such as servers, switchers, head-end encoders, and specialty studio displays. This article details key components of new design frameworks that make it easier to develop custom IFC signal chains.

Most Popular News from Last Issue

[White Paper: Avoid PCB Design Mistakes \(PDF\)](#)

In FPGA-based systems, managing the multitude of PCB-related design issues is compounded by the size, complexity, and programmable nature of the FPGAs themselves. This paper discusses the factors that must be considered to achieve a high-quality FPGA-based PCB design.

To ensure that you receive future issues of Inside Edge, please add announcements@altera.com to your address book.

As a subscriber to the Inside Edge, you will receive a monthly email newsletter. To unsubscribe from this newsletter or subscribe to additional Altera email updates and newsletters, please visit our [Email Subscription Center](#).



Altera email communications include:

- Product Announcements & Updates
- Webcast & Video newsletter
- Embedded newsletter
- DSP newsletter

Copyright © 1995-2009 Altera Corporation, 101 Innovation Drive, San Jose, California 95134, USA

ALTERA, ARRIA, CYCLONE, HARDCOPY, MAX, MEGACORE, NIOS, QUARTUS & STRATIX are Reg. U.S. Pat. & Tm. Off. and Altera marks in and outside the U.S.