

October 2009

www.altera.com

Monthly Spotlight

[New Stratix IV E Device—the Industry's Highest Density 40-nm FPGA](#)

Simplify your design partitioning and accelerate your verification cycle with the newest member of the Stratix® IV family. The EP4SE820 device has 820K logic elements, 23.1 Mbits of memory and 1,120 I/O pins, making it the logical choice for ASIC prototyping and design emulation.



FPGAs, CPLDs & ASICs

[Video: See 100G Interlaken Solution on 40-nm High-Density FPGA](#)

See an Altera® Interlaken solution running on our 100G demo board and learn about the design advantages of 40-nm Stratix IV GT FPGAs.

[Video: See PCIe, XAUI, & 3G-SDI on an Arria II GX Transceiver FPGA](#)

See how implementing various protocols on Arria® II GX devices can lower cost and power. Also, view the transceiver's eye diagram.



Software, Intellectual Property & Development Kits

[Buy Quartus II Software & Get a Nios II Evaluation Kit for \\$99](#)

Available to the first 300 Customers—purchase Quartus® II Software at full price and get a Nios® II Embedded Evaluation Kit for \$99 (\$449 value).

[Embedded Linux for the Nios II Processor](#)

You can now choose from a wide range of embedded providers, including free open-source distributions to full commercial support.

Technology & End Markets

[Webcast: Designing with Multiple Industrial Ethernet Standards](#)

See how to design with a flexible FPGA platform that supports any Ethernet protocol, saving time and lowering your cost of ownership.

[Webcast: Upgrade Your Broadcast System to PCIe Gen2](#)

PCIe Gen2 offers interfaces with increased bandwidth for 1080p video. Learn techniques for bridging 3G Triple-Rate SDI to PCIe Gen2.

[App Note: DPRIO and Multiple Instances SDI Application](#)

Learn how to control multiple SDI cores across several transceiver blocks using the Dynamic Reconfiguration Controller.

[White Paper: Cost-Optimized FPGAs Deliver OTN Mapper Solutions](#)

Read how telecommunications carriers plan to transition their existing infrastructure to a more cost-per-bit effective transport technology.



Support & Literature

[App Note: Timing Closure Methodology for FPGA Designs](#)

Achieve quick timing closure using the practical tips and design examples provided in the application note.



[Click to enlarge](#)

[From the Altera Forum: DMA Transfer Issue](#)

Forum user **Bhupesh** has a problem transferring data between memory interfaces using DMA. Read comments and post your advice.

Events & Training

[Free Online Class: Serial RapidIO Design with Altera 40nm Devices](#)

Learn to design Serial RapidIO® transceivers for your device—develop and verify a custom protocol Serial RapidIO solution in an FPGA.

[BeMicro "Lab on a Stick" Embedded Processor Workshops](#)

Ever wondered what it's really like to use a soft core processor? Find out by building and running your own system on the BeMicro board.

[Intel® Atom™ and Altera I/O Hub Hands-On Europe Workshops](#)

Find out how PCI Express delivers high-performance I/O expansion and co-processing support on the Gleichmann Industrial Reference Platform.

Altera In the News

[FPGAs Enable Energy-Efficient Motor Control, Industrial Embedded.com](#)

Learn how FPGAs can integrate processor, Industrial Ethernet/fieldbus standards, custom motor interfaces, and DSP functions in one device.

[Building High-Speed FPGA Memory Interfaces, PLD DesignLine](#)

To build reliable memory interfaces, target FPGA I/O structures, as well as IP used in design software, for rapid configuration and extra timing margin.

Most Popular News from Last Issue

[White Paper: The Energy-Aware Approach to Home Energy Control](#)

Learn how to develop cost-effective, energy-aware solutions that allow homeowners to monitor appliance energy use via a home area network, appliance manufacturers to provide improved service to customers, and utility companies to lower energy consumption via the Internet.

To ensure that you receive future issues of Inside Edge, please add announcements@altera.com to your address book.



As a subscriber to the Inside Edge, you will receive a monthly email newsletter. To unsubscribe from this newsletter or subscribe to additional Altera email updates and enewsletters, please visit our [Email Subscription Center](#).

Altera email communications include:

- Product Announcements & Updates
- Webcast & Video enewsletter
- Embedded enewsletter
- DSP enewsletter

Copyright © 1995-2009 Altera Corporation, 101 Innovation Drive, San Jose, California 95134, USA

ALTERA, ARRIA, CYCLONE, HARDCOPY, MAX, MEGACORE, NIOS, QUARTUS & STRATIX are Reg. U.S. Pat. & Tm. Off. and Altera marks in and outside the U.S.