

Monthly Spotlight

[White Paper: The Energy-Aware Approach to Home Energy Control](#)

Learn how to develop cost-effective, energy-aware solutions that allow homeowners to monitor appliance energy use via a home area network, appliance manufacturers to provide improved service to customers, and utility companies to lower energy consumption via the Internet.



FPGAs, CPLDs & ASICs

[Buy Today: Cyclone® III LS-Lowest Power FPGAs with Security](#)

The lowest-power 200K LE FPGAs for under 0.25W of static power are shipping. They're ideal for design security and design separation.

[MAX IIZ CPLDs: Lower Static Power & Available in Industrial Grade](#)

The MAX® IIZ static power spec was cut by 40-55%, and standby ICC is down to 25uA. New industrial-grade MAX IIZ CPLDs support -40°C to 100°C.

Software, Intellectual Property & Development Kits

[Altera CPRI IP for Wireless Basestation Design Now Available](#)

Speed development of LTE wireless basestations and remote radio heads using Altera's complete, easy-to-use intellectual property core.

[Download Open Source Embedded Linux for the Nios II Processor](#)

In addition to commercial Linux support from Wind River, now you can get a community-supported open-source Linux distribution from the Nios® Wiki.

Technology & End Markets

[Video: Support Multiple Industrial Ethernet Protocols with 1 FPGA](#)

See demos integrating motor control and industrial Ethernet in a single FPGA, and how you can change protocols on the same FPGA platform.

[White Paper: Cost-Effective HMIs for Home Appliances](#)

Learn how low-cost, high-performance human-machine interfaces with interactive GUIs replace mechanical HMIs found on most home appliances.

[White Paper: A Flexible Solution for Industrial Ethernet](#)

Use Altera FPGAs to deliver multistandard Industrial Ethernet capability to create a universal but easy-to-maintain solution on a single board.

Support & Literature

[New Interface Protocol IP Support Centers](#)

Find answers to interface protocol questions on six new support pages on PCIe, RapidIO, SDI, Triple Speed Ethernet, and POS-PHY L4 protocols.

[From the Forum: Minimum Pulse Width \(dcfifo\) for Cyclone III FPGA](#)

Forum user **Hua** needs to fix dcfifo timing violations. Read the comments and post your advice to gain Forum reputation today!

Altera In the News

[Deinterlacing with FPGA for HDTVs, Video/Imaging DesignLine](#)



[Click to enlarge](#)

Explore how different deinterlacing video processing techniques in FPGAs are used for HDTV applications.

Most Popular News from Last Issue

[Order New Arria® II GX Development Kits Today](#)

Cut development time for cost-sensitive applications requiring high-performance 3-Gbps transceivers. With this kit, you can develop and test designs for PCIe, Gigabit Ethernet, and other transceiver protocols. Add one of 20+ available HSMC daughter cards for even more functionality.

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